Integral Cycle Controller

Check for Samples: UCC29900

FEATURES

- **Integral Cycle Control for High Efficiency Burst Mode Operation at all Load Levels**
- **Allows Easy Use of Low Cost Self-Driven Secondary-Side Synchronous Rectifiers (SRs)**
- **Advanced Drive Signal Timing Control for Volt-Sec Balance**
- **Light-Load Mode for Reduced Power Consumption at No Load and Light Load**
- **Integrated Soft-Start Function**
- **Frequency Dithering for Improved EMI Reduction**
- **Bus Voltage UVLO and OVP Sensing**
- **Current Sense Input for Overcurrent Protection**
- **SCP Input Pin to Flag Short-Circuit Condition**
- **Selectable Latching or Hiccup Mode OCP/SCP**
- **START Output – Ease Startup Bias Design, (allow improved PFC stage startup transient)**
- **FAULT Output to Indicate Latched Fault State**

APPLICATIONS

- **High Efficiency AC-DC Converters**
- **Low Profile & High Density AC-DC Adapters**

DESCRIPTION

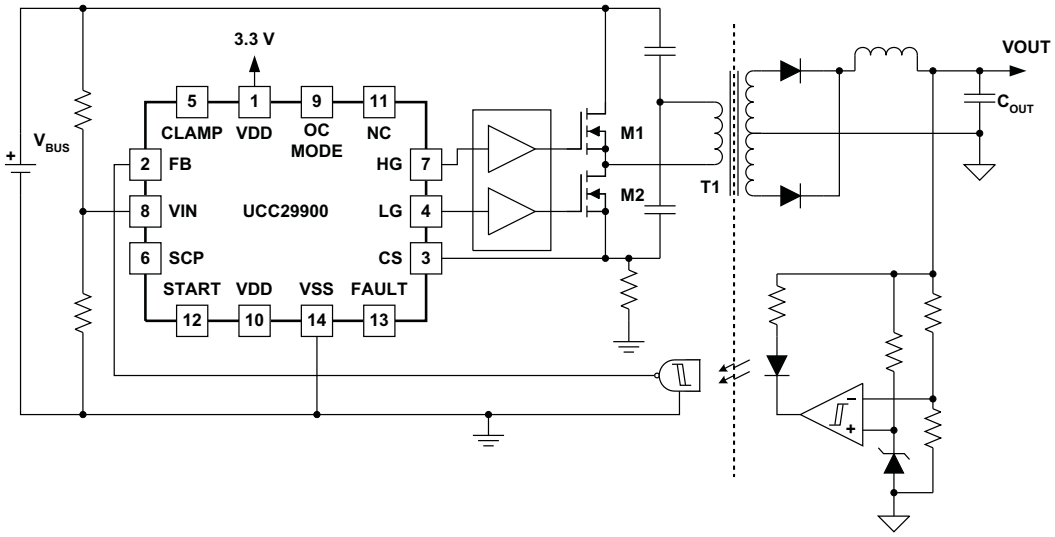
The UCC29900 is a new class of Integral Cycle Control (ICC) controller designed to implement ultra-high efficiency isolated switching power stages. ICC can be employed to achieve ultra-high conversion efficiency over a wide range of load current. The hysteretic mode output voltage control employed exhibits fast transient response, with almost zero output overshoot. Isolation stage efficiencies of >96% have been demonstrated in reference designs.

ICC controllers operate the switching power stage in high efficiency burst mode at all load levels, rather than the more conventional PWM mode.

The UCC29900 is a highly integrated ICC controller, incorporating all the features necessary to implement a wide range of high efficiency designs. The UCC29900 has been designed for ease of use, and incorporates many useful features, including over-current and short-circuit protection, bus under- & over-voltage detection, soft-start and light load management.

PRODUCT PREVIEW

SIMPLIFIED APPLICATION DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING
UCC29900PW	Plastic, 14-pin TSSOP (PW)	90-pc. per Tube
UCC29900PWR	Plastic, 14-pin TSSOP (PW)	2000-pc. Tape and Reel

ABSOLUTE MAXIMUM RATINGS(1) (2) (3)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	LIMIT	UNIT
Supply voltage: VDD	4.1	V
	-0.3	
Voltage: all pins	−0.3 to VDD + 0.3	
Diode current: all pins	+/- 2	mA
Operating free air temperature, T_A (4)	−40 to +105	°C
Operational junction temperature, T_J (4)	−40 to +105	
Storage temperature, T_{STG} (4)	−40 to +105	
Lead temperature (10 seconds)	260	

(1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
Operating free air temperature, T_A	−40	105	°C
VDD input voltage	3.23	3.37	V
VIN, FB, & SCP input voltage range	0	VDD	

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) VDD = 3.23 - 3.37 V, VSS = 0 V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Biasing						
I_{VDD}	VDD current			5		mA
Voltage Monitoring						
	VIN UVLO threshold	Measured at VIN (rising)	2.32	2.38	2.44	V
	VIN UVLO hysteresis	Measured at VIN (falling)		0.6		
	Startup delay	VIN = 3.3 V, Measured as start of HG switching after removal of UVLO fault		64		ms
V_{OVP}	Input over voltage threshold	Measured at VIN rising	2.76	2.83	2.9	V
	OVP delay	Measured between VIN and FAULT rising edges		20		µs
Feedback						
	FB rising threshold		1.45		2.53	V
	FB falling threshold		0.8		1.85	
	Hysteresis		0.3		1	
	FB rising response time			2		µs
Soft Start						
$t_{SS(max)}$	Max soft start period	Total duration of SS Operation, FB = 3.3 V		20		ms
$t_{SS(int)}$	Initial SS interval	Initial time delay between HG bursts in SS mode, FB = 0 V		160		µs
Oscillator						
	Switching frequency	Measured at LG & HG, FB = 3.3 V	-6%	126.5	6%	kHz
	LG period	First LG pulse after FB rising		2		µs
		Subsequent LG pulses, FB = 3.3 V		4		
		Last LG pulse after FB falling		2		
	HG period	FB = 3.3V		4		
	LG period – light load	First LG during light load		4		
		Last LG during light load		4		
	HG period – light load	HG pulse during light load		8		
Frequency Dithering						
	Dithering magnitude	Max frequency – min frequency		12		kHz
	Dithering rate	Time to sweep from max to min and back to max frequencies		6		ms
	Min dithering frequency	Measured at LG, FB = 3.3 V		121		kHz
	Max dithering frequency	Measured at LG, FB = 3.3 V		133		

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted) VDD = 3.23 - 3.37 V, VSS = 0 V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Light Load Detect						
	Light load enable timeout	Measured between FB rising edges to enable Light Load Mode		40		µs
	Light load disable timeout	Measured between FB rising edges to disable Light Load Mode		135		
Over Current Protection						
V_{OCP1}	Over current, lower threshold	Measured at CS during LG pulse	61	75	88	mV
	Over current, V_{OCP1} delay	Measured as the duration of LG pulses with CS > V_{OCP1}		16		ms
V_{OCP2}	Over current, upper threshold	Measured at CS during LG pulse	185	200	215	mV
	Short circuit, V_{OCP2} delay	Measured as the duration of LG pulses with CS > V_{OCP2}		11		ms
Short-Circuit Protection						
	SCP internal pull up		20	35	50	kΩ
	SCP falling threshold		0.8		1.85	V
	SCP rising threshold		1.45		2.53	
	Hysteresis		0.3		1	
	Restart delay	Measured between restart attempts - latch-off mode		1		ms
	Max restart attempts	Latch-off mode		9		
	Hiccup delay	Measured between restart attempts – Hiccup mode		480		ms
Power On Reset (POR)						
V_{POR}	Falling threshold	Measure at VDD falling			1.71	V
	Hysteresis		70	130	210	mV
	POR delay	Duration of VDD < V_{POR}		2		µs
Start & Fault Outputs						
	START & FAULT output voltages – high	I_{START} & I_{FAULT} = -1.5 mA	VDD – 0.25		VDD	V
	START & FAULT output voltages – low	I_{START} & I_{FAULT} = 1.5 mA	0		0.25	
Gate Outputs						
	LG, HG, & CLAMP output voltages -- high	I_{LG}, I_{HG}, & I_{CLAMP} = -1.5 mA	VDD – 0.25		VDD	V
	LG, HG, & CLAMP output voltages – low	I_{LG}, I_{HG}, I_{CLAMP} = 1.5 mA	0		0.25	
	LG, HG, & CLAMP rise times	C_{LOAD} = 0.2 nF		15		ns
	LG, HG, & CLAMP fall times	C_{LOAD} = 0.2 nF		22		

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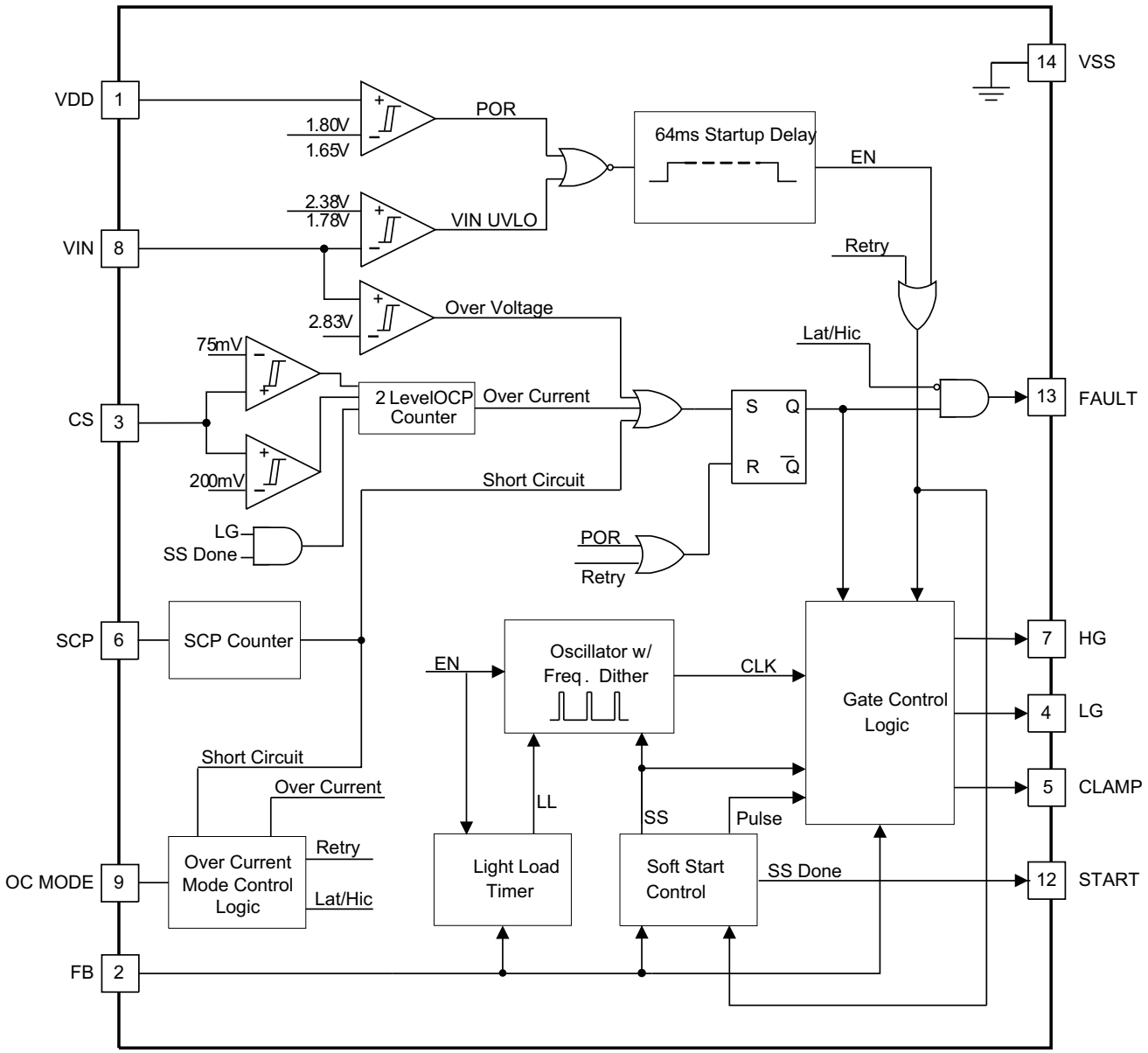
DEVICE INFORMATION

Functional Bllock Diagram



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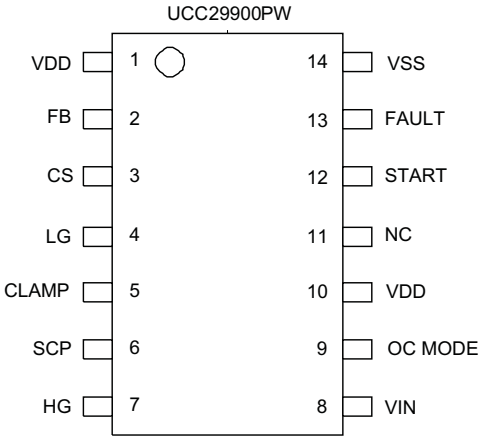
TERMINAL FUNCTIONS

TERMINAL	PIN NUMBER	I/O	DESCRIPTION
VDD	1	I	Provides power to the device; should be decoupled with ceramic capacitor 0.1 μF to 1 μF, connected directly across pins 1-14.
FB	2	I	Feedback or control input from the secondary side opto-coupler; used to enable (FB High) or inhibit (FB Low) switching to effect hysteretic mode output voltage regulation .
CS	3	I	Current sense input for over-current and short circuit protection; usually derived from a current sense resistor.
LG	4	O	Low-side drive signal output. Connect to MOSFETS driver device.
CLAMP	5	O	Transformer clamp MOSFETS drive signal.
SCP	6	I	Short-Circuit-Mode flag input, active low with internal pull-up to V_{DD}.
HG	7	O	High-side drive signal output. Connect to MOSFETS driver device.
VIN	8	I	Voltage sense input for input bus voltage UVLO and OVP.
OC MODE	9	I	Connect to V_{SS} for latching or V_{DD} for Hiccup protection mode.
VDD	10	I	This pin must be connected to V_{DD}, and must not be left floating .
NC	11	-	No connection should be made to this pin, this pin should be left floating.
START	12	O	START is held low at start-up, during power-on delay, and during the ramp-up sequence. Once the UCC29900 enters NORMAL operation , START is driven high. START is driven low also during latched fault mode.
FAULT	13	O	Logic level fault output – output HIGH indicates internally latched fault state.
VSS	14	-	Ground for internal circuitry.



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APPLICATION INFORMATION

Theory of Operation

TI has developed a fully functioning reference design using the UCC29900 ICC controller, full details of which are available on request. This design is for a universal input, single output, 90-W PSU intended for laptop adapter applications. It comprises a buck PFC stage converting the incoming line power to a nominal 84 V. A half-bridge power stage is used to convert this intermediate voltage to an isolated 19.25-V nominal output. In addition to the UCC29900 ICC controller the design uses synchronous rectifiers to give maximum efficiency levels. The following paragraphs give some details on how the features of the UCC29900 are used to maximum effect in this reference design. Additional application guidelines for the UCC29900 are available on request.

Supply Rail and Start-up

The recommended minimum rate of rise of V_{DD} in the target system is 1 V/ms. This requires attention to system design, to ensure that V_{DD} rail total capacitance is not excessive and that start-up linear regulators to generate V_{DD} are not too restrictively current limited. Issues may be observed during start-up with the UCC29900 due to an excessively slow rate of rise of the supply rail V_{DD}. If the supply rail rate of rise is insufficient, especially with respect to the rate of rise of the input bus sense signal VIN, then a FAULT mode latch-off can occur.

For the 90WLP Notebook Adapter Reference Design, the 3.3-V V_{DD} rail is derived via two series linear regulators from the main PFC bus voltage (nominally 84 V), as shown in Figure 1. In this case the 100-V start-up linear regulator NPN transistor is chosen as a Darlington type to ensure adequate emitter current capability to rapidly charge the V_{DD} load capacitance. For this system, the expected V_{DD} rate of rise is typically 10 V/ms as shown in Figure 2.

Since the V_{DD} rail is internally used to generate reference levels for OVP, UVP and OCP, good rail decoupling is highly recommended. A local ceramic capacitor of at least 100 nF (1 µF recommended) should be placed directly from pin 1 (V_{DD}) to pin 14 (V_{SS}). In addition, the tolerance of the V_{DD} rail should be limited (recommended to +/-2%) to limit the tolerances of the OVP, UVP and OCP levels.

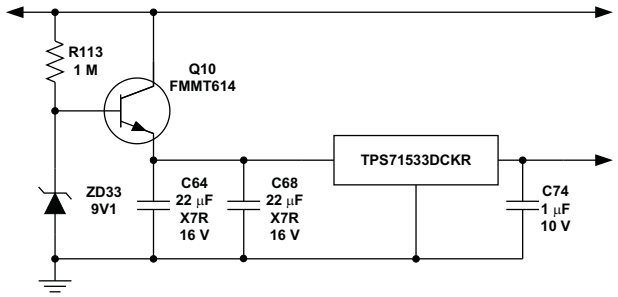

Figure 1. Typical V_{DD} Startup Linear Regulators

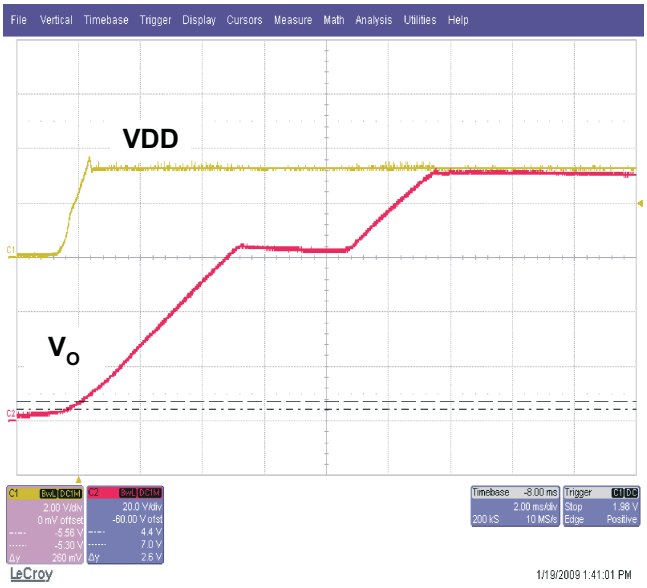

Figure 2. Typical V_{DD} Risetime for CCT in Figure 1

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Bus UV Sense, Start-up Delay

The VIN pin of the controller is internally compared to a reference of 2.38 V to enable the output switching signals. A resistor divider across the bus voltage from the PFC stage is used to scale the bus voltage to achieve the desired enable level. The Thevenin equivalent source resistance of the divider chain is recommended to not exceed 10 kΩ. A small local filter capacitor can be connected from the VIN pin to V_{SS} (Pin 14) to prevent noise from affecting the bus voltage sensing. However, this filter cap value should not exceed 1 nF, so that VIN pin response time is not degraded.

This pin incorporates 600 mV of hysteresis to the bus under-voltage disable level. This hysteresis is to help prevent unwanted ICC stage restart under ac removal or sag conditions due to the typically low loop bandwidth and bus dynamics for PFC stages. When the VIN level has dropped below the lower under-voltage falling threshold, the current switching cycle is completed, and the controller then ceases switching until VIN is increased above the upper under-voltage rising threshold. The PFC bus VIN UV levels are illustrated in Figure 3.

For the 90WLP Notebook Adapter Reference Design, the expected rate of rise of VIN is dependent on the ac line voltage, PFC stage power components and control circuit & values. Typically, rise time from 0 V to regulation level will be about 10 ms.

Once the bus voltage exceeds the rising UV enable level, the controller implements a fixed start-up delay time. This start-up delay is implemented to allow the PFC stage error amplifier to settle closer to its final value, to ease start-up bus voltage transients and hence improve output start-up dynamics.

Bus OVP Sense

The VIN pin of the controller is also compared to a higher over-voltage protection (OVP) reference level of 2.83 V. This sets the bus OVP level at approximately 120% of the UV enable level. In normal operation, the PFC stage should regulate the bus voltage, typically with an upper level of bus over-voltage clamping to keep the bus voltage from reaching excessive levels during heavy-load to light-load transients. If however, due a system fault, the over-voltage clamp does not operate, the UCC29900 incorporates latching OVP shutdown to minimise the risk of system damage. In this case the FAULT pin can be used to trigger latch-off of the PFC stage also. The PFC bus VIN OVP level is illustrated in Figure 3.

A small local filter capacitor should be connected from the VIN pin to V_{SS} to prevent noise from affecting the bus voltage sensing. However, this filter cap value should not exceed 1 nF so that OVP response time is not degraded.

As with all faults detected, if OVP occurs during a switching cycle, then the cycle is completed, and the controller goes into a latched fault state at the end of the cycle. If OVP occurs outside a switching cycle, then the controller immediately enters latched fault mode.

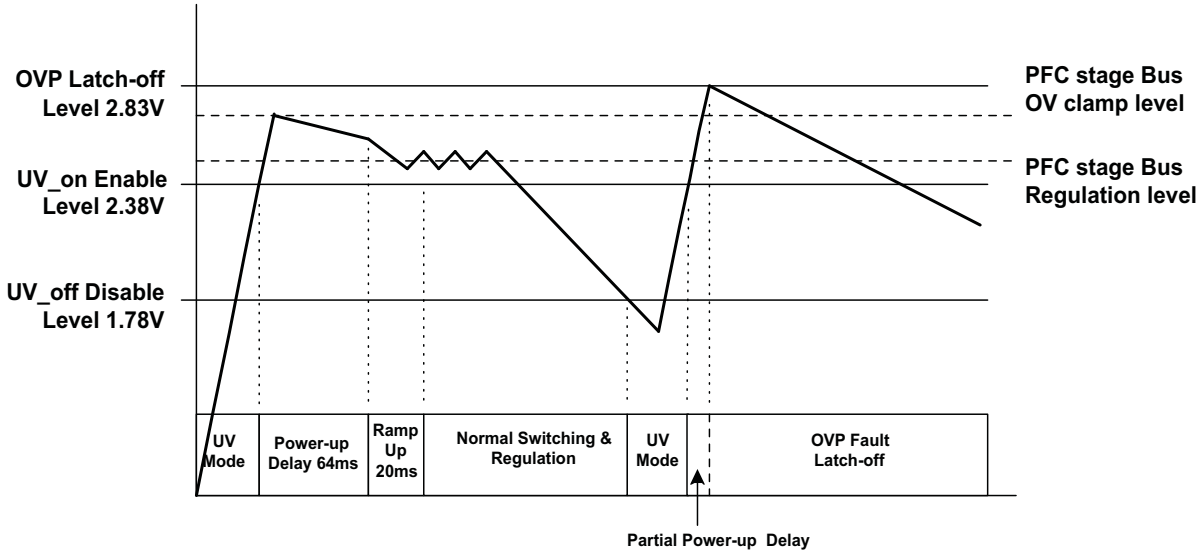

Figure 3. PFC Bus Voltage Sense UV & OV Levels

Ramp-Up Mode

Once the start-up delay period has elapsed, the controller begins ramp-up mode. This mode delivers a single switching cycle, followed by a defined off-time, i.e. an off-interval with no switching cycles. After this defined off-time, another single switching cycle is delivered, followed by another defined off-time. The off-time between switching cycles is gradually reduced, i.e. the single switching cycles are delivered progressively closer together. By gradually advancing the single switch cycles closer together, the output voltage is slowly increased.

Ramp “duty cycle” is defined as the ratio of switching cycle duration to incremental period, i.e. the sum of switching cycle duration and subsequent off-time duration. A gradual duty cycle increase is implemented to ensure an approximately linear monotonic ramp up of the output capacitor voltage. There is minimum fixed off-time, which in turn results in a fixed max ramp duty cycle of nominally 95% at the end of the ramp.

Depending on load demand, the output should normally reach regulation before the end of the nominal 20ms ramp interval. As soon as the output feedback signal FB goes low, indicating that the output has reached nominal regulation level, then the ramp is terminated, and normal output voltage regulation commences.

Depending on load demand and the timing of the start-up ramp relative to ac line crossovers, under some circumstances, the output voltage may not reach regulation by the end of the ramp interval. This is due to the inherent buck PFC “dead-time” during which the buck PFC stage is reverse biased, and no power can be drawn from the ac line. In this case, since the bus voltage will effectively decrease, while the integrator duty is increasing, the net output voltage may slow down in rate of rise, or even plateau. For this reason, regulation may not always occur within the ramp interval. In such cases, operation still advances to normal switching mode at the end of the nominal 20-ms ramp. In this mode, full 100% effective duty cycle can be delivered, so that the output voltage is quickly brought to regulation level.

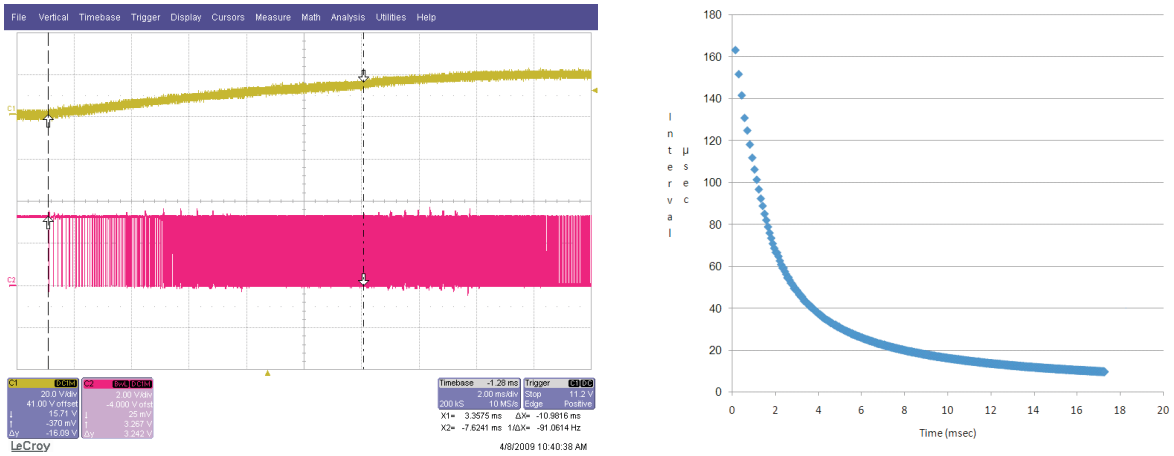

Figure 4. Typical Ramp-Up Pulse Set Timing

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Feedback Input (FB)

The FB (feedback) input pin is used to regulate the output voltage in a hysteretic control mode. The output voltage is sensed and compared to a reference value by a comparator on the secondary side, and the comparator output drives a digital Schmitt-input opto-coupler. When the output voltage is below the regulation level, the comparator output is high and the opto-coupler is not driven; when the output voltage exceeds the regulation level, the comparator output goes low and turns on the opto. In this way, the output comparator acts like a simple 1-bit A/D converter. The opto-coupler feeds the digital feedback information to the primary side across the isolation barrier. The opto-coupler output signal to FB is high when Vout is below regulation level, and low when Vout is below the regulation level.

In normal mode, the controller monitors the FB pin to determine the switching cycle mark/space ratio. When FB is found to be high, a switching cycle is commenced. Every time a switching cycle is commenced, it is completed fully, regardless of the FB pin level. During each current switching cycle, FB is monitored to determine whether or not a subsequent switching cycle should be delivered. If FB stays high, then another switching cycle is delivered contiguously. If FB goes low, then switching ceases or “drops out” at the end of the current cycle. While delivering switching cycles, FB is polled once every switching cycle, or approximately every 8 μs. Once switching ceases at the end of the cycle, FB is monitored while the controller waits for the next FB high transition to indicate that switching should recommence.

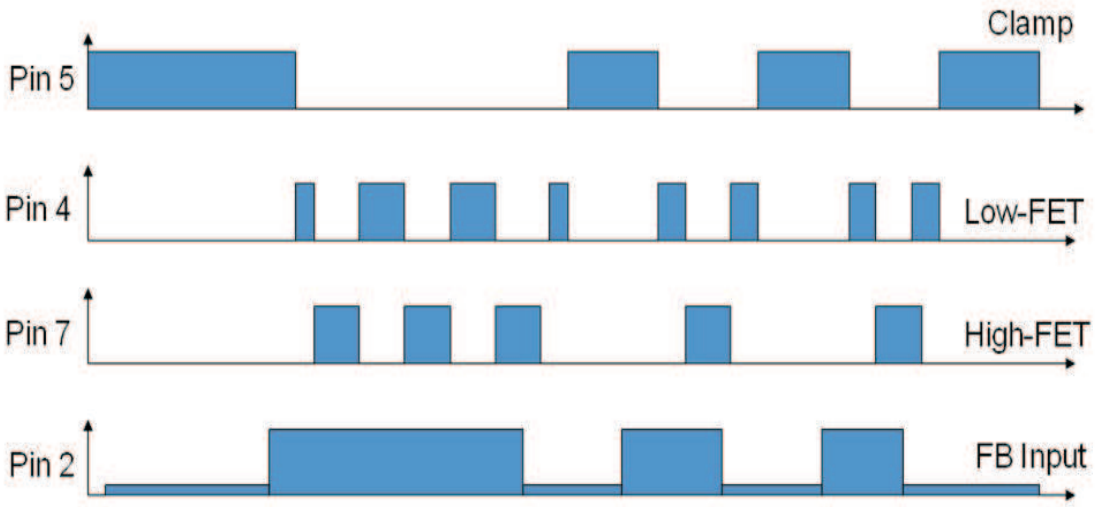

Figure 5. Typical FB Response

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Gate Drive Volt-Sec Balance

The drive signals LG & HG are designed to deliver balanced on-time to both low side and high-side half-bridge MOSFETS. This is necessary to ensure power transformer volt-sec balance.

Figure 6. HB Drive Signal "Manchester Encoding"

In addition, the signals are "Manchester-encoded" as shown in Figure 6. This proprietary (to TI) mode of operation means that the LG on time is divided into two intervals, each half the duration of the HG on time, with the drive signals sequenced LG-HG-LG. This encoding additionally ensures that the half-bridge capacitor midpoint remains balanced. If a gate drive transformer is to be used, then this encoding also ensures balanced drive signals for this transformer.

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Gate Drive Dead-time

The LG & HG drive signals are recommended to be connected to the driver inputs through RCD delay networks as shown below. This allows the dead-time or non-overlap time of the drive signals to be adjusted by suitable choice of resistor and capacitor values. Fixed internal dead-times are not implemented to allow more user flexibility. Use of external RCD delay gives more system design flexibility to cater for different system power levels, MOSFET choices, transformer design, etc.

Importantly, the system can be designed to make use of these dead-times to achieve zero-voltage-switching (ZVS) or soft-switching. In this case, the energy stored in the transformer leakage inductance (due to the flow of transformer magnetising current plus reflected load current) can be used to charge/discharge the MOSFET output capacitances during the dead-time, such that the voltage across each MOSFET has discharged to zero or close to zero before that MOSFET is turned on. Soft-switching reduces switching losses and increases system efficiency.

Drive signal dead-time management is critical to ensure that the system does not suffer from cross-conduction between the primary half-bridge MOSFETS, and also between the primary MOSFETS and complementary secondary side synchronous rectifier (SR) MOSFETS. Such cross-conduction would result in excessive device power dissipation, poor system efficiency, possible EMC issues, internal system noise issues, and in some cases MOSFETS device destruction due to thermal runaway.

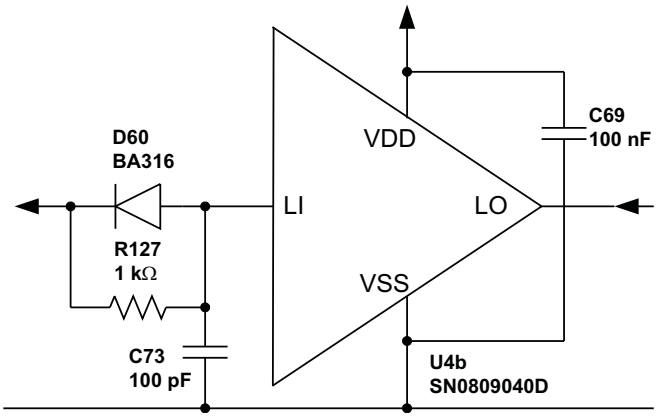

Figure 7. Typical RCD Dead-Time Implementation

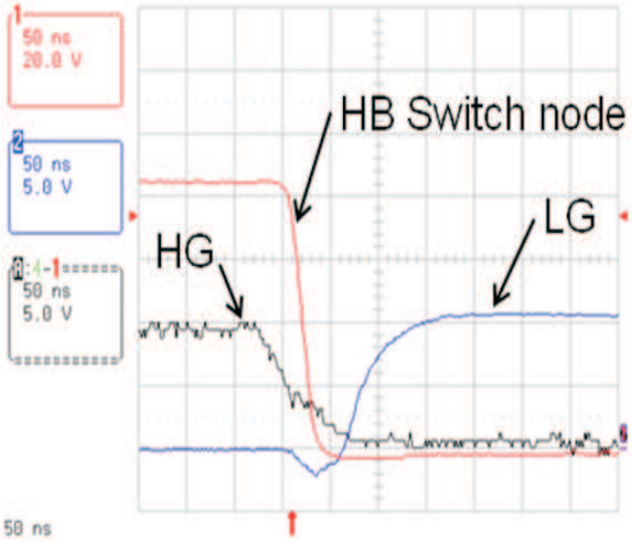

Figure 8. Typical ZVS Waveforms HG OFF, LG ON

Gate Drive Frequency Dithering

The gate drive signals are frequency dithered to improve EMC performance. This is implemented by varying the switch period in discrete steps, as outlined in the table below. The maximum dither frequency is chosen to limit the maximum switching frequency to be no higher than 135 kHz, to avoid possible issues with sidebands of the max switching frequency "spilling over" above the 150-kHz starting frequency per EN55022.

Table 1. Frequency Dithering

FREQUENCY STEP	TOTAL SWITCHING PERIOD	SWITCHING FREQUENCY
1	7.50 μs	133 kHz
2	7.75 μs	129 kHz
3	8.00 μs	125 kHz
4	8.25 μs	121 kHz

The controller sets a nominal time of 1 ms at each distinct switching frequency. The frequency is dithered sequentially from the minimum value to the maximum value, then back down to the minimum value, and so on, spending equal time at each frequency step.

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Light-Load Mode

When the system load current drops below approximately 3% of full load, the controller enters “Light-Load” Mode. In this mode, the controller extends the MOSFETS on-times to approximately double that used in normal mode, i.e. 16-µs nominal switching period, or 62.5-kHz effective switching frequency. At this half-frequency, output inductor current will build to twice the level, so that four times the energy is stored in the inductor and delivered to the output capacitor. This causes the burst rate of the switching cycles to reduce approximately four-fold in Light-Load mode. This reduction in the repetition rate of switching cycles greatly improves the power stage efficiency.

Because of the low level amplitude of the current sense signal available, it is not possible to get enough resolution to detect very low current levels in light-load mode. For this reason, the light-load transitions are performed based on measuring the time separation of switching cycles, i.e. using the pulse-set separation as a proxy for the load current level – this is very valid at light load current levels, since operation will be heavily discontinuous, and the rate of pulse set delivery will vary almost linearly with load level.

To ensure clean transitions, hysteresis is employed in the timing decision values for the transition into and out of light-load mode. In addition, due to the hysteretic mode control, there will always be a degree of jitter in the time interval between successive pulse sets due to noise in the output comparator. To make the mode transitions robust to this jitter, a counter is employed to ensure that a there are a small number of successive or almost successive timing events that satisfy the transition criterion before the transition is made.

In order to speed up response to sudden load demands, if the FB input remains high even after delivery of a light-load mode switching cycle, then an immediate transition to normal mode occurs, regardless of the timing between pulse sets or the value of the mode transition counter.

Frequency dithering is not employed during light-load mode.

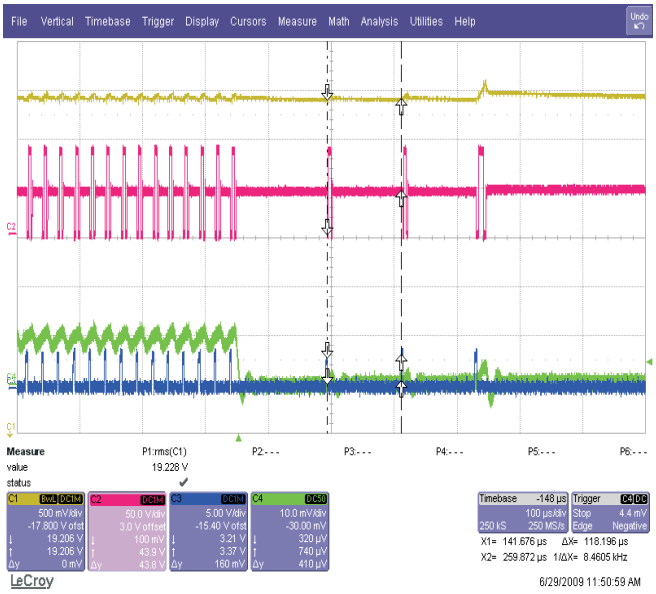


Figure 9. Typical Pulse Set Timing for Transition Into Light Load Mode

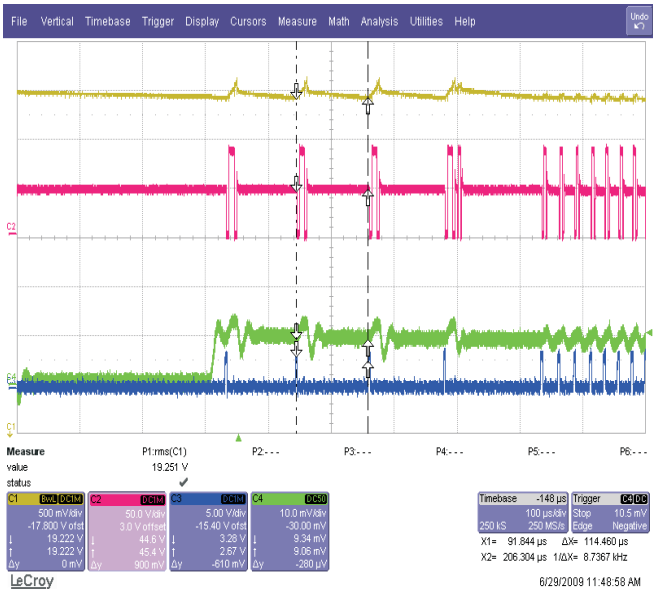


Figure 10. Typical Pulse Set Timing for Transition Out of Light Load Mode

CLAMP Function

As already outlined the “Feedback Input” section, in normal mode, the controller monitors the FB pin to determine the switching cycle mark/space ratio. When FB is found to be low, then switching ceases or “drops out” at the end of the current cycle. By dropping out at the end of a cycle, the half-bridge transformer magnetising current will be approximately zero, and the half-bridge capacitor mid-point voltage will also be balanced. However, the reflected load current will still flow in the leakage inductance, so the transformer must be clamped in order to prevent spurious turn-on of the secondary side self-driven synchronous rectifiers (SRs). Without such clamping, then during dropouts, the leakage inductance energy can cause the voltage on the self-driven SR gate windings to ring to a level sufficient to turn on one of the SR’s. This can then kick start a Royer-type self-oscillation within the transformer windings during the dropout intervals – this can lead to high audible noise, high dissipation within the transformer and MOSFETS, and possible damage to the power devices.

This clamping is most easily done by simply using a winding on the transformer, and shorting this winding to GND during the drop-outs by turning on a mosfet. The CLAMP signal from the UCC29900 is designed to be high during dropouts, when both LG & HG are inactive, so can be used to drive an external clamp mosfet. The clamp winding can be implemented in many ways, but ideally should have reasonably good coupling to the main primary winding. If rectifying diodes are added, and the clamp is decoupled by another diode, then the clamp winding can conveniently serve a dual purpose as a bias supply winding, as shown in Figure 11.

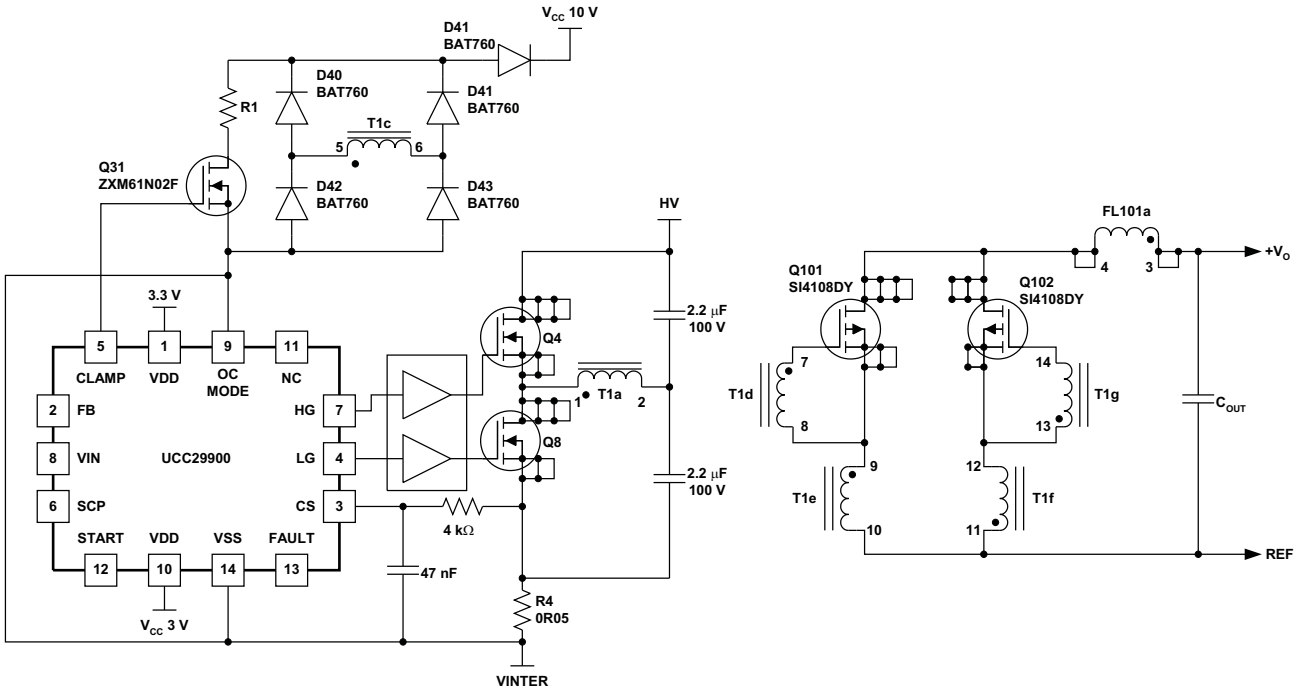


Figure 11. Typical CLAMP Function Implementation (simplified)

Over Current and Short Circuit Protection MODE Selection

The Over Current and Short Circuit protection mode depends on whether the OC MODE pin is tied high or low. If this pin is low, then all FAULT conditions cause the FAULT output to go high and the controller enters a latched fault state, recovery from this state is achieved by power cycling the system.

If this pin is tied high then the controller enters a Hiccup mode if the Over-current or Short circuit trip levels are exceeded. In Hiccup mode, the FAULT line remains low, switching is stopped for the Hiccup delay time of approx 480 ms. Once this interval has elapsed and both FB & SCP pins have gone high, then switching operation is resumed in soft-start Ramp-Up mode. The system will restart if the fault has cleared or it will wait a further 480 ms before re-trying again. The system will continue re-trying every 480 ms until a successful restart has been achieved.

Over-Current Protection (OCP)

The over-current function is implemented by measuring the current flowing on the primary side of the power stage, because the secondary side load current cannot be directly sensed due to the primary-secondary isolation barrier. This primary current sense is an accurate replica of the load current flowing on the secondary side, with the exception that it will also exhibit a large ripple component at twice the ac line frequency.

The sensed current at the CS pin should be filtered through an R-C network to help filter out switching ripple. The recommended filter network is 4.7 kΩ/47 nF. The CS pin source feeding resistance is recommended to be kept below 5.3 kΩ. For slowly changing load currents, this filtering delay is not significant. However, for very fast changing overloads and output short circuits, there is a necessity for a separate parallel protection scheme (outlined later), so the CS pin filter delay is still not significant.

The CS signal is internally compared to a 2-level over-current trip level. The use of a 2-level over-current threshold allows more rapid response to more severe overloads. The lower trip level is set to 75 mV, with a delay time of nominally 15 ms. The upper level is set to 200 mV with a minimum delay time of 10 ms, this ensures that the system "rides through" all types of overloads and short-circuits of duration <10 ms. If either trip level is exceeded for the appropriate delay time, then an OCP state is entered. The OC MODE pin may be used to select either a Latch-off or Hiccup response.

Short-Circuit Protection (SCP)

Due to the deliberate internal delay times to ensure “ride-through” capability to short-term (<10 ms) overloads, the CS pin internal response is not sufficiently fast to ensure adequate protection for the power stage, in the case of severe overloads, such as output short circuit. For this reason, a separate external fast comparator is recommended. For ease of implementation and cost minimisation, this can be adequately implemented as a simple low cost NPN transistor, Q11 in Figure 12 below. The base of the transistor connects to the same shunt resistor used to generate the CS signal for the CS pin. In the case of severe over-current due a short-circuit, this NPN transistor will turn on. The collector of this transistor should be connected via diodes to both FB and SCP input pins of the controller (diodes need to be used to prevent the SCP pin from being pulled low by normal regulation feedback).

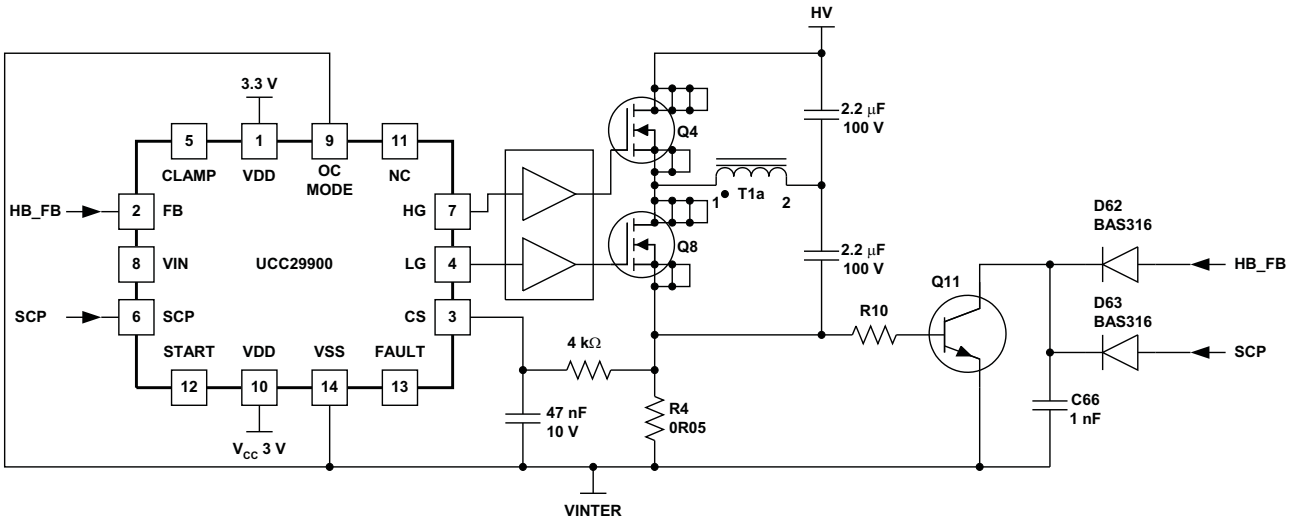


Figure 12. Typical SCP Function Implementation (simplified)

PRODUCT PREVIEW

Once the SCP pull-down has been internally latched, the controller temporarily inhibits all switching for a defined “SCP blanking interval”. This interval is 1ms if the OC MODE pin is Lo and 480ms if it is HI. During this interval, the VIN level is still monitored against OVP and UV levels. At the end of the blanking interval, if either the FB or SCP pin levels are low, then the blanking interval is extended until such time that both FB and SCP pins are both high again.

Once the blanking interval has elapsed and both FB & SCP pins have gone high, then switching operation is resumed in soft-start Ramp-Up mode. This ensures that the current is built up slowly again into the short circuit. It also ensures that the system can restart normally into full load if the short-circuit has been cleared (i.e. momentary accidental short).

However, if the short-circuit is persistent, then at a point in the ramp-up phase, the current will have built to a level where the external NPN transistor will again turn on and pull down the FB and SCP pins. The FB & SCP pull-downs will terminate ramp-up and force the controller into SCP mode once again.

In Latch-off OC MODE only, each time SCP mode is entered, an SCP mode counter is incremented. Once the SCP mode counter reaches a limit of 10 events, then the controller enters a latch-off state, and the FAULT pin is driven high. However, if a successful ramp up is completed without the SCP pin being pulled low, then this SCP mode counter is decremented over a short time interval.

In Hiccup OC Mode, the presence of a persistent short circuit will force the controller to repeatedly enter the SCP mode and wait for the Hiccup delay time before trying to re-start the output.

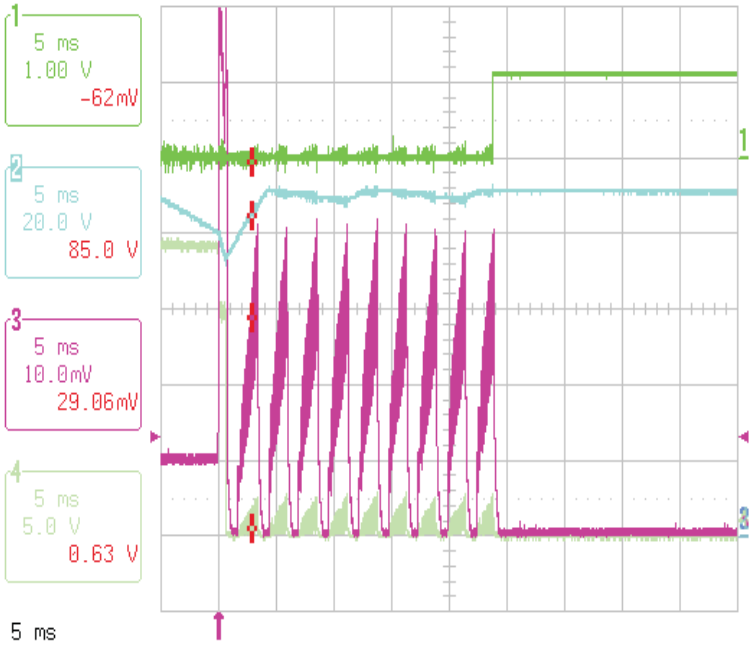


Figure 13. Typical SCP Restart Timing Before Latch-Off

Start Function

The START pin is used to flag when the controller has completed the ramp-up phase. This can be used for many possible features such as:

- Gate-off a start-up linear regulator, once start-up is complete, to save power.
- Gate-off a start-up linear regulator, once start-up is complete, to ease back-bias tolerance issues.
- Flag to the PFC stage that the isolation stage is powering up, possibly into full load, to allow the PFC stage to operate in some type of fast-transient response mode to improve start-up transients.

The START pin is designed to be active low at initial power on and during ramp-up phase. It should then be driven high when the ramp-up phase ends and normal mode begins. The START pin should remain high during all subsequent operation, except for the following:

- During the latched fault state due to any faults, the START pin is cleared low in order to turn on the external startup linear regulator. This ensures continuity of bias supply to the controller, to ensure that the latched state does not get released until ac mains power is removed, and also to ensure that the bus voltage is discharged as rapidly as possible once ac mains power is removed, so that the latched fault is then reset as quickly as possible.
- During SCP mode blanking interval and the Hiccup delay time, START pin is also cleared low to turn on the start-up linear regulator, again to ensure continuity of bias voltage during intervals of no switching.

Fault Mode

In response to some fault conditions, the controller enters a latched fault state. In this state, no switching cycles are delivered, the FAULT pin is driven high in order to flag the fault condition to the PFC stage, and the START pin is driven low to allow the bias start-up linear regulator to turn back on. The controller waits until ac mains power is removed to allow the latched fault state to be reset. Bus under-voltage does not cause a latched fault shutdown, to ensure auto-recovery to as voltage dips, sags, brownouts, etc.

The following faults can cause the controller to enter a latch-off fault state:

- OCP – over-current as sensed on the CS pin and OC MODE pin is LOW.
- SCP – persistent short-circuit as detected by the SCP pin and OC MODE pin is LOW.
- OVP – bus over-voltage as sensed by the VIN pin. OC MODE pin is don’t care.

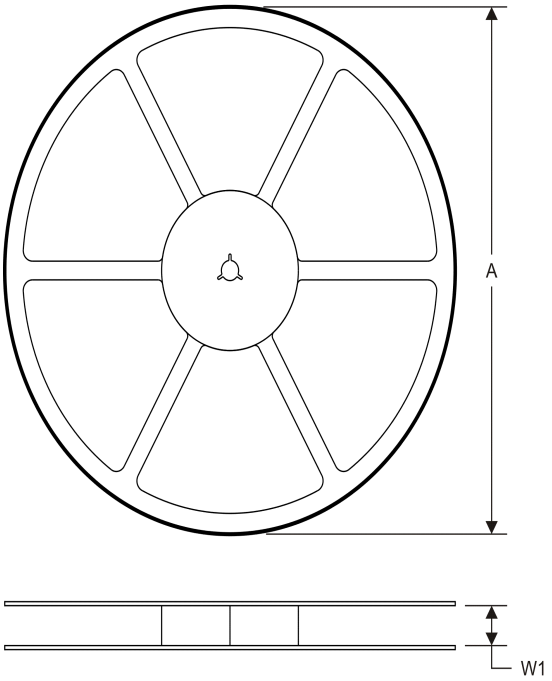
PRODUCT PREVIEW

REVISION HISTORY

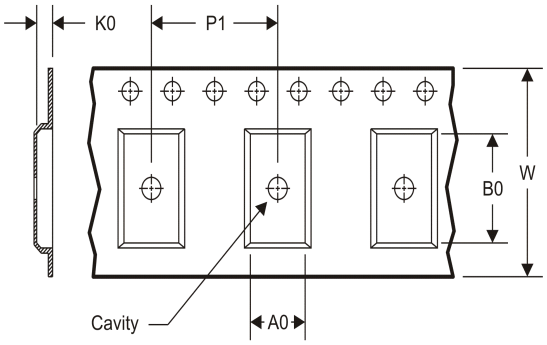
Changes from Revision A (August 2009) to Revision B	Page
• Added FB = 3.3 V	3

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



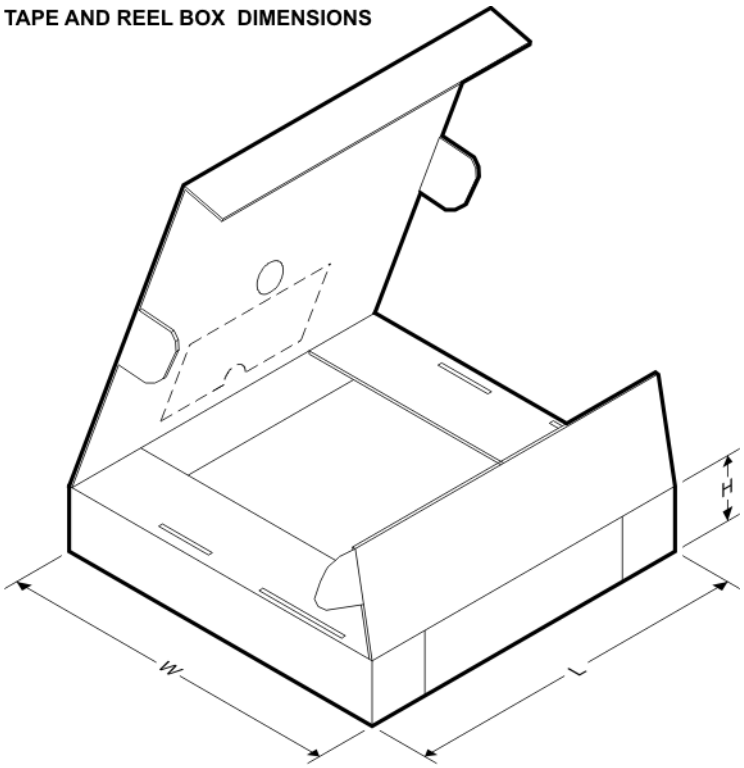
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC29900PWR	TSSOP	PW	14	0	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

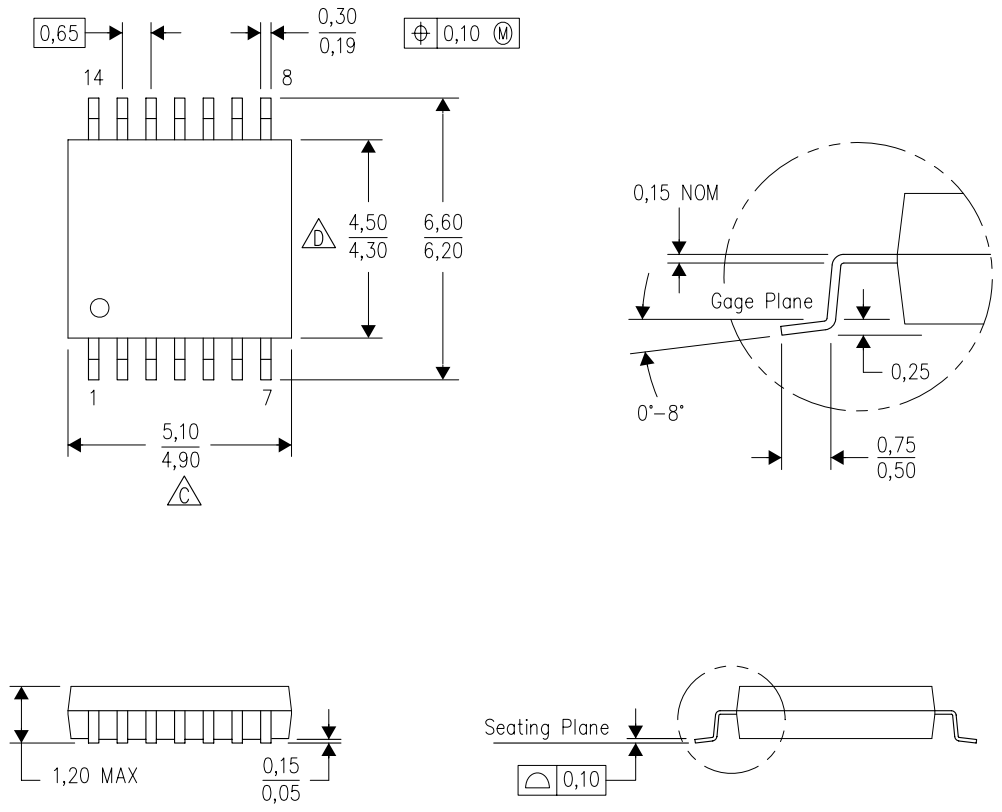
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC29900PWR	TSSOP	PW	14	0	367.0	367.0	35.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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