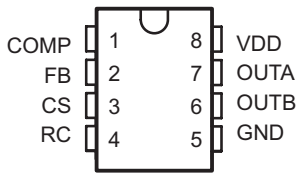
Low Power Current Mode Push-Pull PWM

Check for Samples: UCC2808A-1Q1 , UCC2808A-2Q1

FEATURES

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Dual Output Drive Stages in Push-Pull Configuration**
- **Current Sense Discharge Transistor to Improve Dynamic Response**
- **130-µA Typical Starting Current**
- **1-mA Typical Run Current**
- **Operation to 1 MHz**
- **Internal Soft Start**
- **On-Chip Error Amplifier With 2-MHz Gain Bandwidth Product**
- **On Chip V_{DD} Clamping**
- **Output Drive Stages Capable of 500-mA Peak-Source Current, 1-A Peak-Sink Current**

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

DESCRIPTION

The UCC2808A-xQ1 is a family of BiCMOS push-pull, high-speed, low-power, pulse-width modulators. The UCC2808A-xQ1 contains all of the control and drive circuitry required for off-line or DC-to-DC fixed frequency current-mode switching power supplies with minimal external parts count.

The UCC2808A-xQ1 dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60 ns to 200 ns depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

The UCC2808A-xQ1 family offers a variety of package options and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery powered systems. Thresholds are shown in the ordering information table.

The UCC2808A-xQ1 is an enhanced version of the UCC2808 family. The significant difference is that the A versions feature an internal discharge transistor from the CS pin to ground, which is activated each clock cycle during the oscillator dead time. The feature discharges any filter capacitance on the CS pin during each cycle and helps minimize filter capacitor values and current sense delay.

ORDERING INFORMATION[1]

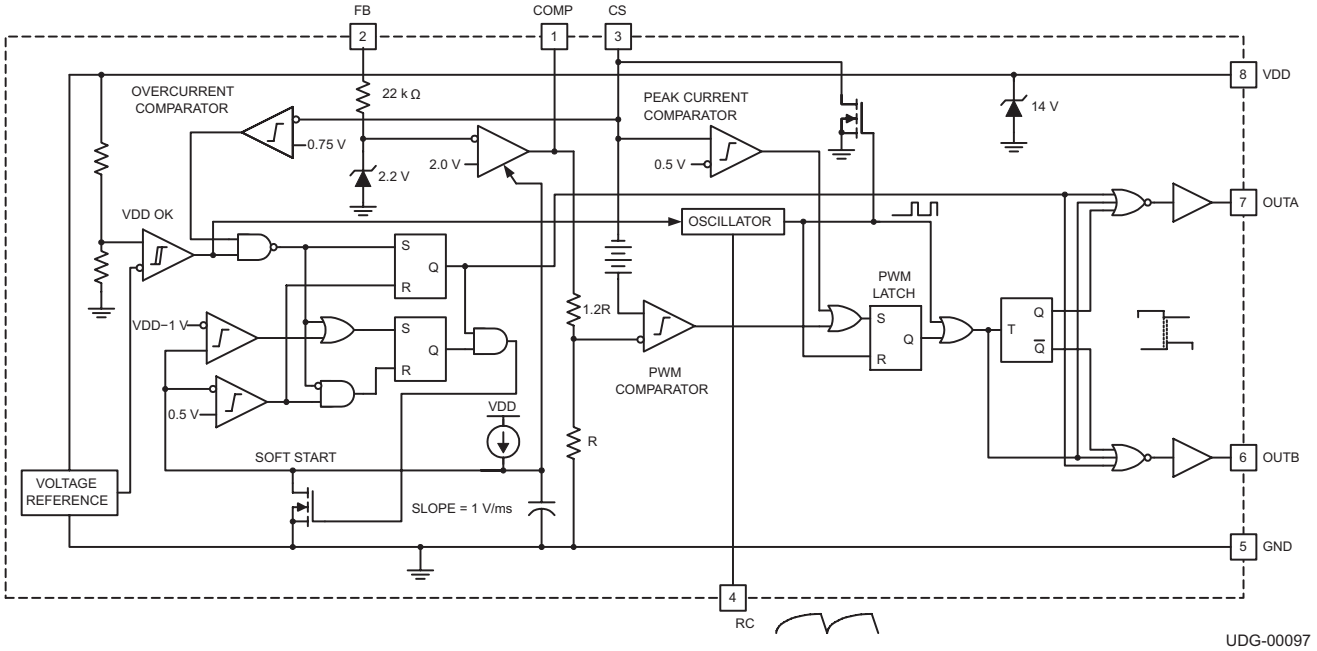
T_A	UVLO OPTION	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	12.5 V/8.3 V	SOIC (D)	Tape and reel	UCC2808AQDR-1Q1	2D08-1
		TSSOP (PW)	Tape and reel	UCC2808AQPWR−1Q1[3]	2808A1
–40°C to 125°C	4.3 V/4.1 V	SOIC (D)	Tape and reel	UCC2808AQDR-2Q1	2D08-2
		TSSOP (PW)	Tape and reel	UCC2808AQPWR−2Q1[3]	2808A2

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Product Preview.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Block Diagram



A. Pinout shown is for SOIC package. TSSOP pinout is different.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Supply voltage (I_{DD} ≤ 10 mA)	15	V
	Supply current	20	mA
	OUTA/OUTB source current (peak)	–0.5	A
	OUTA/OUTB sink current (peak)	1	A
	Analog inputs (FB, CS)	–0.3 to V_{DD} 0.3, not to exceed 6	V
	Power dissipation at T_A = 25°C (D package)	650	mW
	Power dissipation at T_A = 25°C (PW package)	400	mW
T_{stg}	Storage temperature	–65 to 150	°C
T_J	Junction temperature	–55 to 150	°C
	Lead temperature (soldering, 10 sec.)	300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Currents are positive into, negative out of the specified terminal. Consult the Packaging Section of the *Power Supply Control Data Book (TI Literature Number SLUD003)* for thermal limitations and considerations of packages.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 125°C for the UCC2808A-xQ1, V_{DD} = 10 V(1), 1-µF capacitor from V_{DD} to GND, R = 22 kΩ, C = 330 pF $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator Section					
Oscillator frequency		175	194	213	kHz
Oscillator amplitude/V_{DD}		(2)0.44	0.5	0.56	V/V
Error Amplifier Section					
Input voltage	COMP = 2 V	1.95	2	2.05	V
Input bias current		–1		1	µA
Open loop voltage gain		60	80		dB
COMP sink current	FB = 2.2 V, COMP = 1 V	0.3	2.5		mA
COMP source current	FB = 1.3 V, COMP = 3.5 V	–0.2	–0.5		mA
PWM Section					
Maximum duty cycle	Measured at OUTA or OUTB	48	49	50	%
Minimum duty cycle	COMP = 0 V			0	%
Current Sense Section					
Gain		(3)1.9	2.2	2.5	V/V
Maximum input signal	COMP = 5 V(4)	0.45	0.5	0.55	V
CS to output delay	COMP = 3.5 V, CS from 0 mV to 600 mV		100	200	ns
CS source current		–200			nA
CS sink current	CS = 0.5 V, RC = 5.5 V(5)	4	10		mA
Over current threshold		0.65	0.75	0.85	V
COMP to CS offset	CS = 0 V	0.35	0.8	1.2	V
Output Section					
OUT low level	I = 100 mA		0.5	1.1	V

(1) For UCC2808A−1Q1, set V_{DD} above the start threshold before setting at 10 V.
(2) Measured at RC. Signal amplitude tracks V_{DD}.
(3) Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$, 0 ≤ V_{CS} ≤ 0.4 V.
(4) Parameter measured at trip point of latch with FB at 0 V.
(5) The internal current sink on the CS pin is designed to discharge an external filter capacitor. It is not intended to be a DC sink path.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 125°C for the UCC2808A-xQ1, V_{DD} = 10 V(1), 1-µF capacitor from V_{DD} to GND, R = 22 kΩ, C = 330 pF $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT high level	I = −50 mA, V_{DD} – OUT		0.5	1	V
Rise time	C_L = 1 nF		25	60	ns
Fall time	C_L = 1 nF		25	60	ns
Undervoltage Lockout Section					
Start threshold	UCCx808A−1(1)	11.5	12.5	13.5	V
	UCCx808A−2	4.1	4.3	4.5	V
Minimum operating voltage after start	UCCx808A−1	7.6	8.3	9	V
	UCCx808A−2	3.9	4.1	4.3	V
Hysteresis	UCCx808A−1	3.5	4.2	5.1	V
	UCCx808A−2	0.1	0.2	0.3	V
Soft Start Section					
COMP rise time	FB = 1.8 V, rise from 0.5 V to 4 V		3.5	20	ms
Overall Section					
Startup current	V_{DD} < start threshold		130	260	µA
Operating supply current	FB = 0 V, CS = 0 V(6)(1)		1	2	mA
V_{DD} zener shunt voltage	I_{DD} = 10 mA(7)	13	14	15	V

(6) Does not include current in the external oscillator network.
(7) Start threshold and zener shunt threshold track one another.

PIN ASSIGNMENTS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC2808A-xQ1 is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC2808A-xQ1 family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.

FB: The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: Reference ground and power ground for all functions. Due to high currents, and high frequency operation of the UCC2808A-xQ1, a low impedance circuit board ground plane is highly recommended.

OUTA and OUTB: Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current.

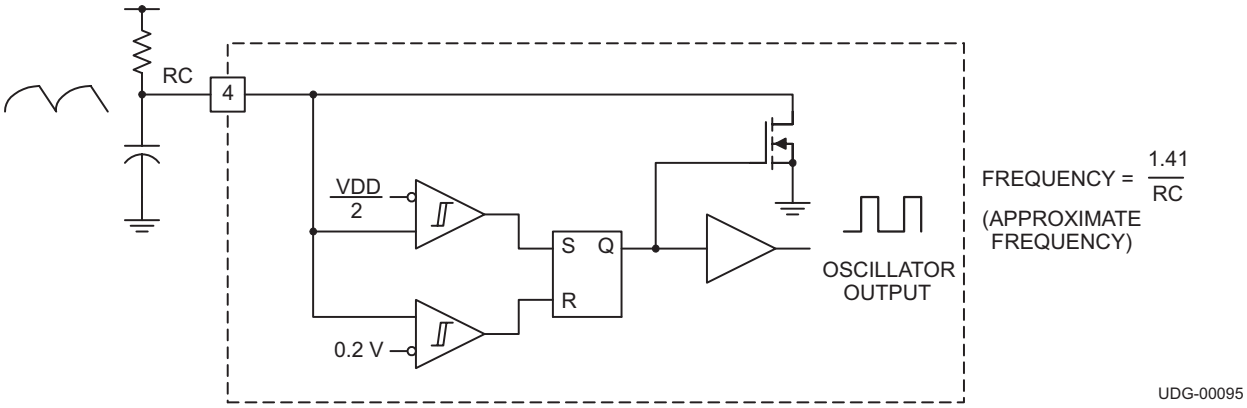
The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from V_{DD} to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky-clamp diodes are not required.

RC: The oscillator programming pin. The oscillator of the UCC2808Ax-Q1 tracks V_{DD} and GND internally, so that variations in power supply rails minimally affect frequency stability. shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the V_{DD} and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula: $f_{OSCILLATOR} = \frac{1.41}{RC}$, where frequency is in Hz, resistance in Ohms, and capacitance in Farads. The recommended range of timing resistors is between 10 kΩ and 200 kΩ and range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 10 kΩ should be avoided.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from V_{DD} as short as possible, and the leads between timing components and RC as short as possible. Separate ground and V_{DD} traces to the external timing network are encouraged.



A. The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a 1/2 the oscillator frequency, with ensured duty cycle of < 50% for both outputs.

Figure 1. Block Diagram for Oscillator

VDD: The power input connection for this device. Although quiescent V_{DD} current is very low, total supply current will be higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from: $I_{OUT} = Q_g \times F$, where F is frequency.

To prevent noise problems, bypass V_{DD} to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1-µF decoupling capacitor is recommended.

APPLICATION INFORMATION

A 200-kHz push-pull application circuit with a full-wave rectifier is shown in Figure 2. The output, V_O, provides 5 V at 50-W maximum and is electrically isolated from the input. Since the UCC2808A-xQ1 is a peak-current-mode controller the 2N2907 emitter following amplifier (buffers the CT waveform) provides slope compensation which is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single ground IC controller, and 1 µF is suggested as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 adjustable precision shunt regulator. Small signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanical strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown here. The main power transformer has a Magnetics Inc. ER28 size core made of P material for efficient operation at this frequency and temperature. The input voltage may range from 36-V DC to 72-V DC.

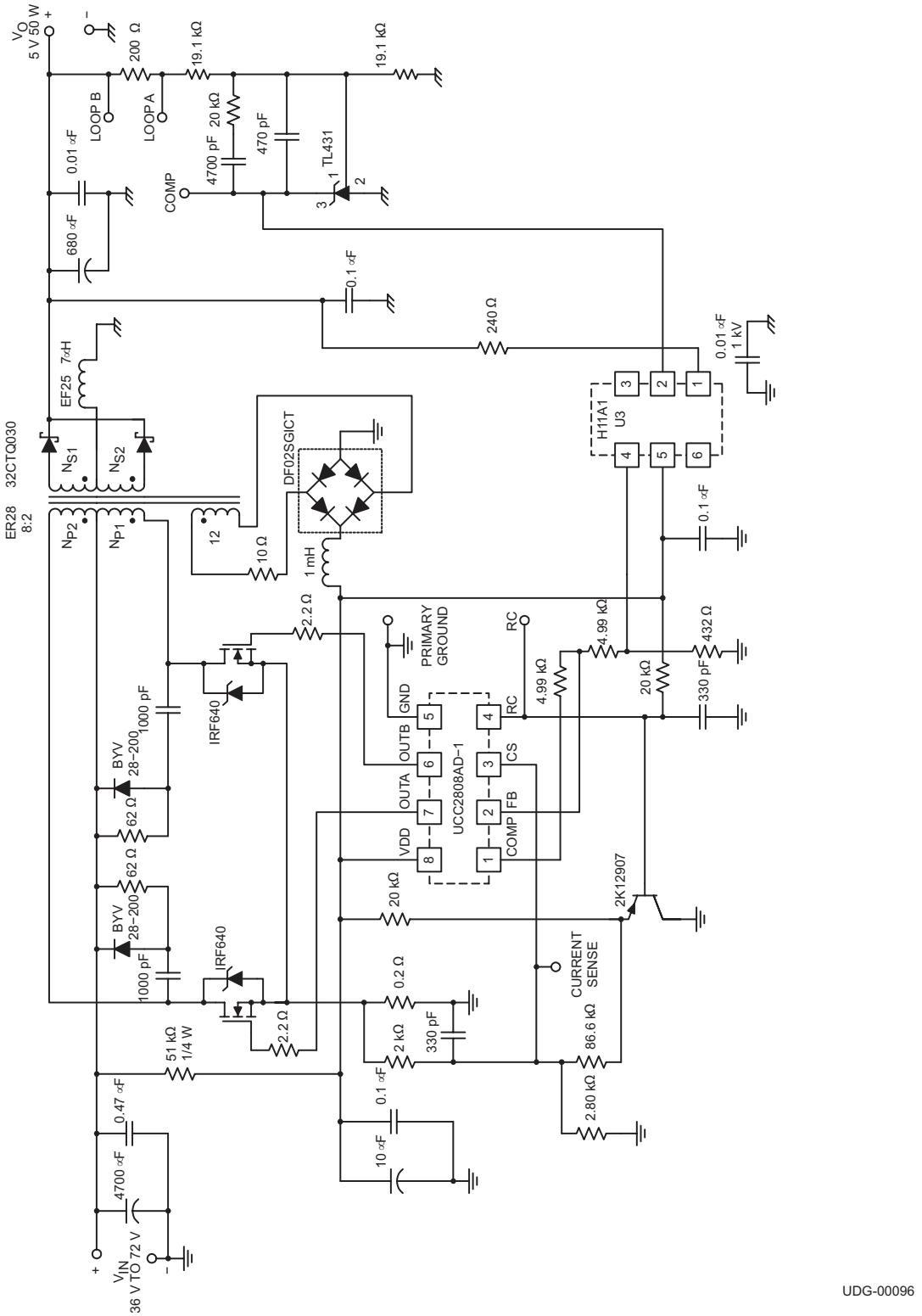


Figure 2. Typical Application Diagram: 48-V In, 5-V, 50-W Output

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs EXTERNAL RC VALUES

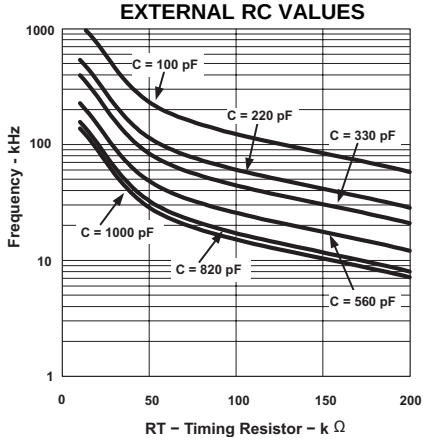


Figure 3.

IDD vs OSCILLATOR FREQUENCY

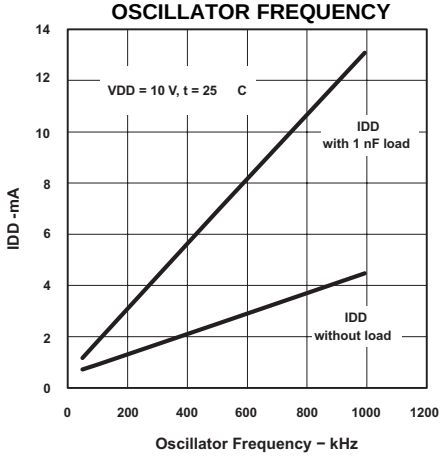


Figure 4.

COMP TO CS OFFSET vs TEMPERATURE

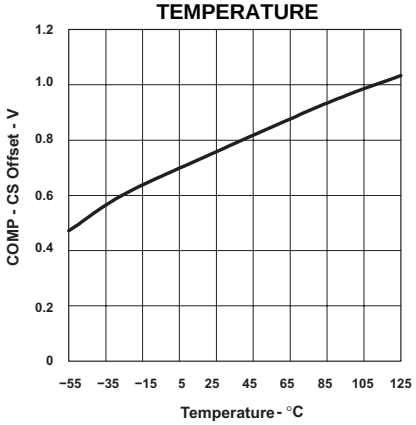


Figure 5.

ERROR AMPLIFIER GAIN AND PHASE RESPONSE vs FREQUENCY

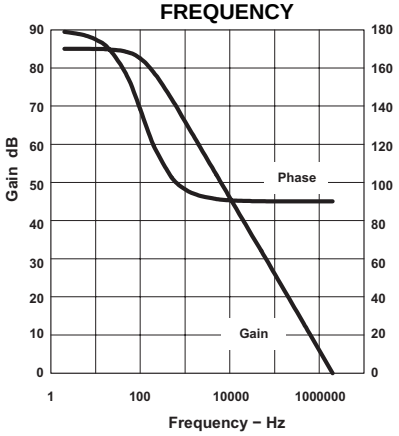


Figure 6.

OUTPUT DEAD TIME vs EXTERNAL RC VALUES

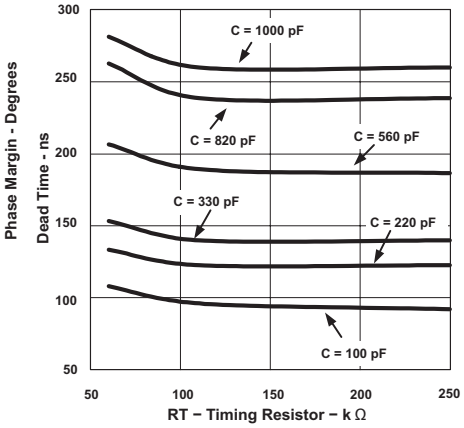


Figure 7.

DEAD TIME vs TEMPERATURE

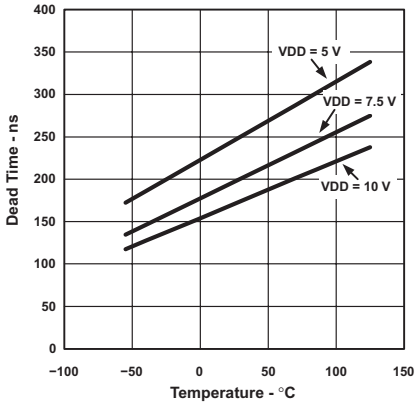


Figure 8.

TYPICAL CHARACTERISTICS (continued)

RC $R_{DS(on)}$ vs TEMPERATURE

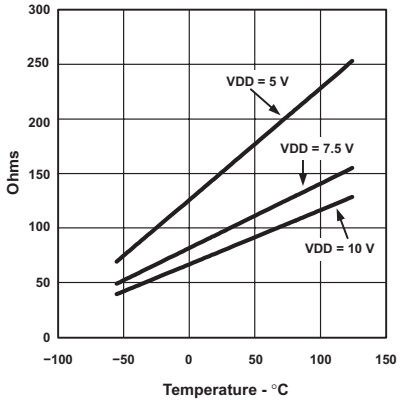


Figure 9.

CS $R_{DS(on)}$ vs TEMPERATURE

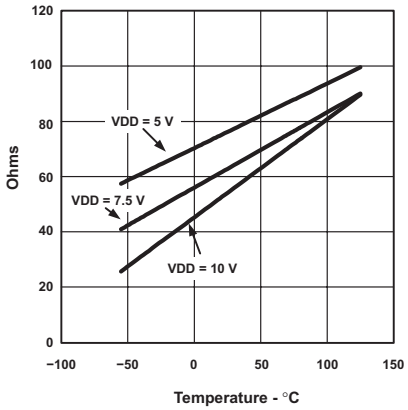


Figure 10.

REVISION HISTORY

Changes from Revision A (April, 2008) to Revision B	Page
• Changed top-side marking for SOIC (D) package from UCC2808AD-1Q1 to 2D08-1 and UCC2808AD-2Q1 to 2D08-2.	2

PACKAGING INFORMATION

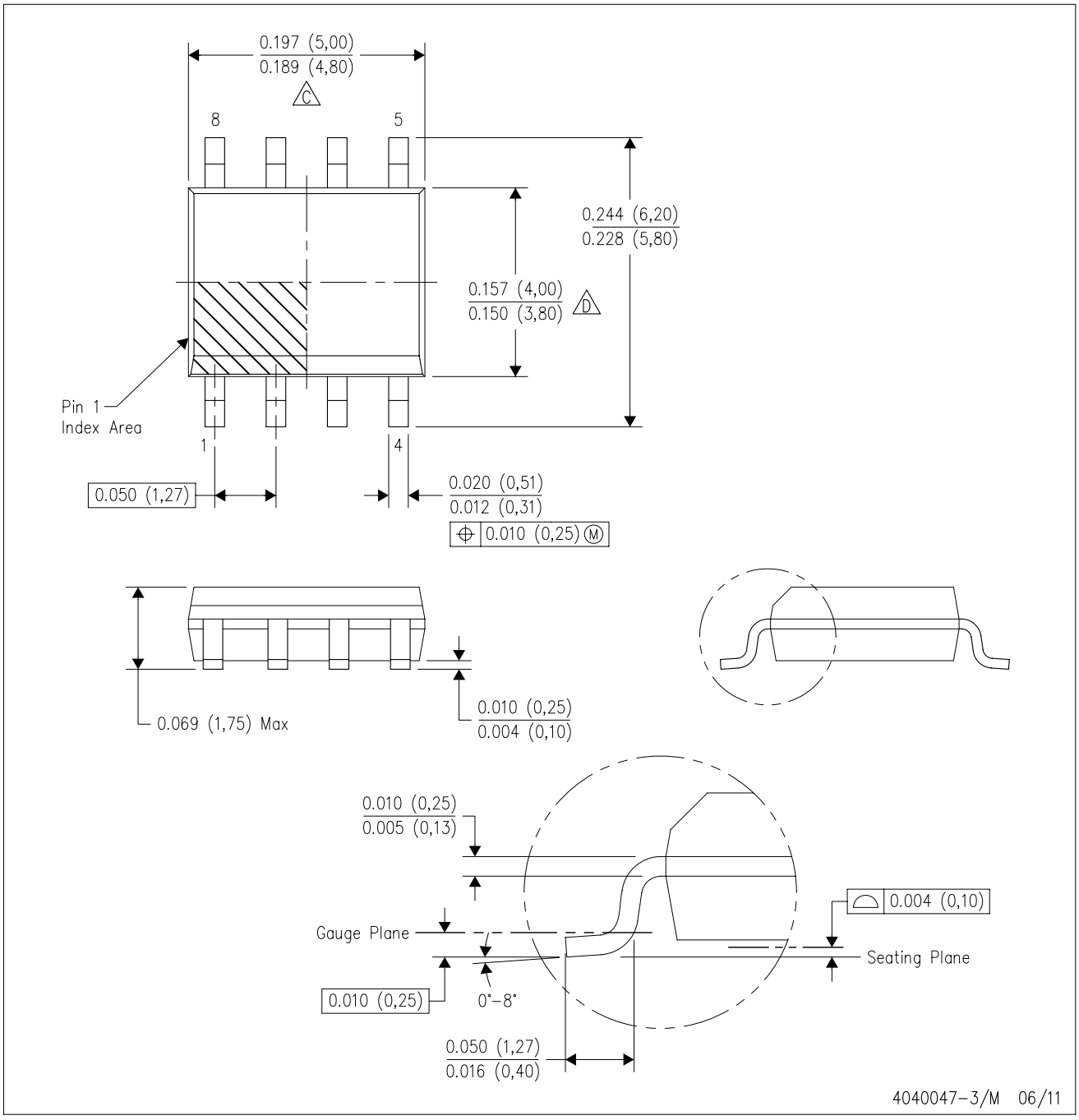
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC2808AQDR-1G4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC2808AQDR-1Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC2808AQDR-2G4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC2808AQDR-2Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

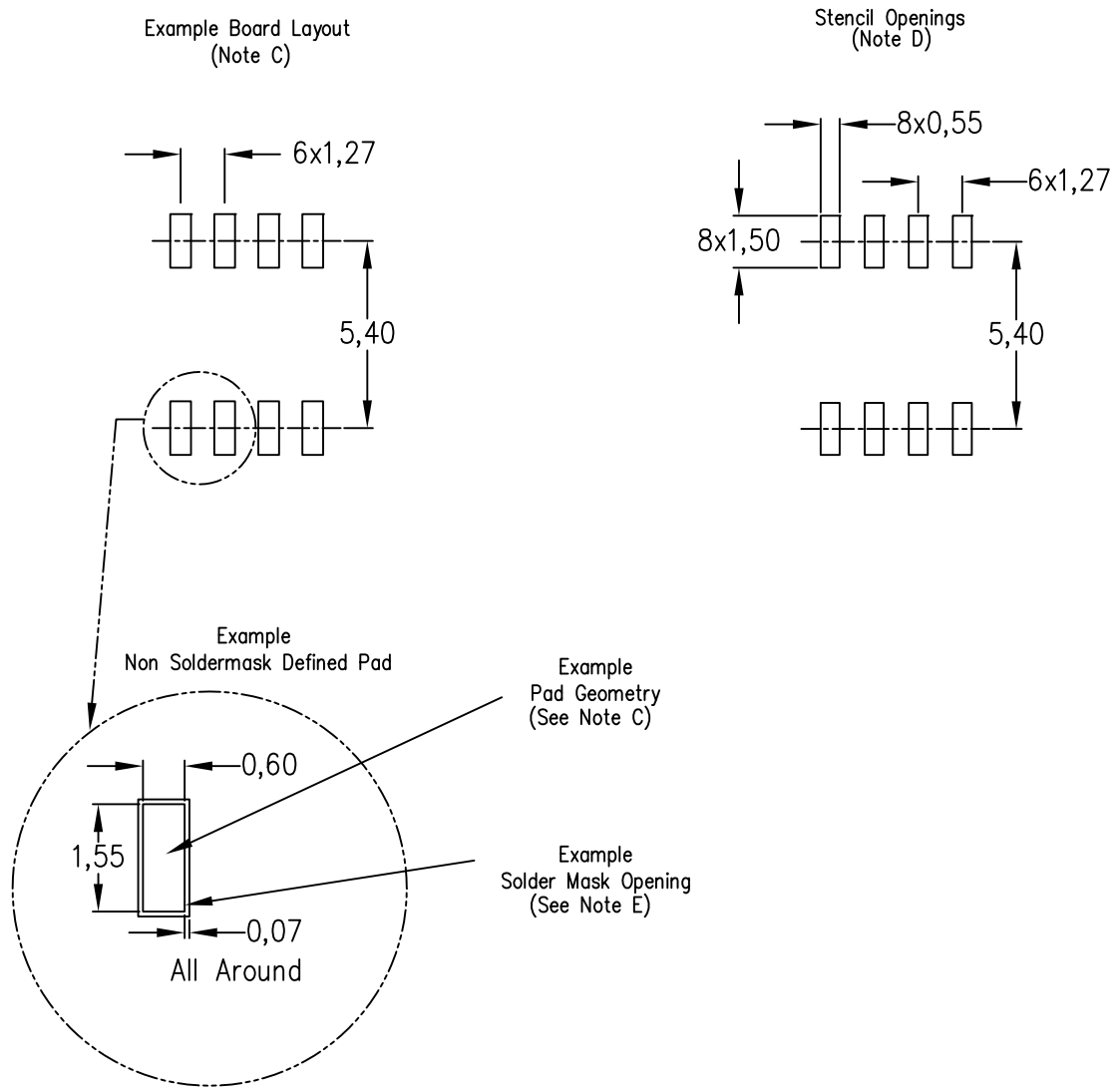
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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