DUAL 4-A HIGH-SPEED LOW-SIDE MOSFET DRIVER WITH ENABLE

Check for Samples: UCC27424-EP, UCC27423-EP

FEATURES

- Industry-Standard Pinout
- Enable Functions for Each Driver
- High Current-Drive Capability of ±4 A
- Unique Bipolar and CMOS True-Drive Output Stage Provides High Current at MOSFET Miller Thresholds
- TTL-/CMOS-Compatible Inputs Independent of Supply Voltage
- 20-ns Typical Rise and 15-ns Typical Fall Times With 1.8-nF Load
- Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns With Input Rising
- 4.5-V to 15-V Supply Voltage
- Dual Outputs Can Be Paralleled for Higher Drive Current
- Available in Thermally-Enhanced MSOP PowerPAD™ Package With 4.7°C/W θjc

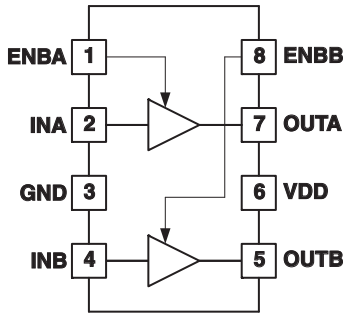
APPLICATIONS

- Switch-Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Line Drivers
- Class-D Switching Amplifiers

SUPPORTS DEFENSE, AEROSPACE AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/150°C) Temperature Range(1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

D OR DGN PACKAGE
(TOP VIEW)



(1) Custom temperature ranges available

DESCRIPTION/ORDERING INFORMATION

The UCC27423 and UCC27424 high-speed MOSFET drivers can deliver large peak currents into capacitive loads. Two standard logic options are offered – dual inverting and dual noninverting drivers. The UCC27424 thermally enhanced 8-pin PowerPAD™ MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. The UCC27423 is offered in a standard SOIC-8 (D) package.

Using a design that inherently minimizes shoot-through current, this driver delivers 4 A of current where it is needed most – at the Miller plateau region during the MOSFET switching transition. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

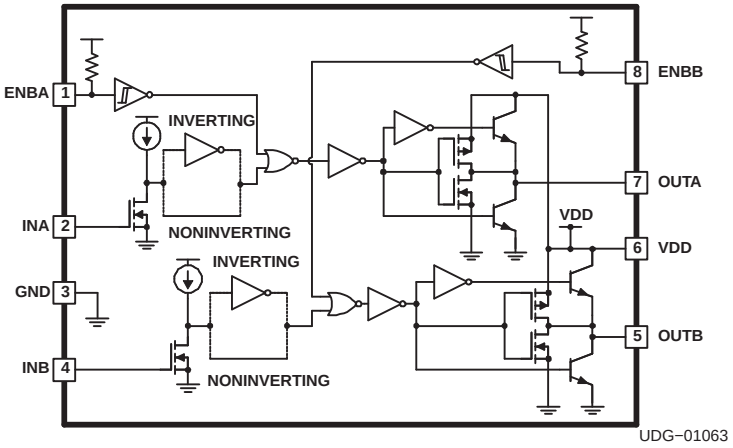
The UCC27423 and UCC27424 provide enable (ENB) functions to better control the operation of the driver applications. ENBA and ENBB are implemented on pins 1 and 8, which previously were left unused in the industry-standard pinout. ENBA and ENBB are pulled up internally to V_{DD} for active-high logic and can be left open for standard operation.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	PART NUMBER	MEDIUM	QUANTITY
–55°C to 125°C	MSOP-8 PowerPAD™ (DGN)(3)	UCC27424MDGNREP	Tape and Reel	2500/Reel
	SOIC 8 (D)	UCC27423MDREP		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(3) The PowerPAD package is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ENBA	1	I	Enable for driver A with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is pulled up internally to V_{DD} with a 100-kΩ resistor for active-high operation. The output state when the device is disabled is low, regardless of the input state.
ENBB	8	I	Enable for driver B with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is pulled up internally to VDD with a 100-kΩ resistor for active-high operation. The output state when the device is disabled is low, regardless of the input state.
GND	3		Common ground. This ground should be connected very closely to the source of the power MOSFET that the driver is driving.
INA	2	I	Input A. Input signal of the A driver, which has logic-compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. It should not be left floating.
INB	4	I	Input B. Input signal of the A driver, which has logic-compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. It should not be left floating.
OUTA	7	O	Driver output A. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
OUTB	5	O	Driver output B. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
VDD	6	I	Supply. Supply voltage and the power input connection for this device.

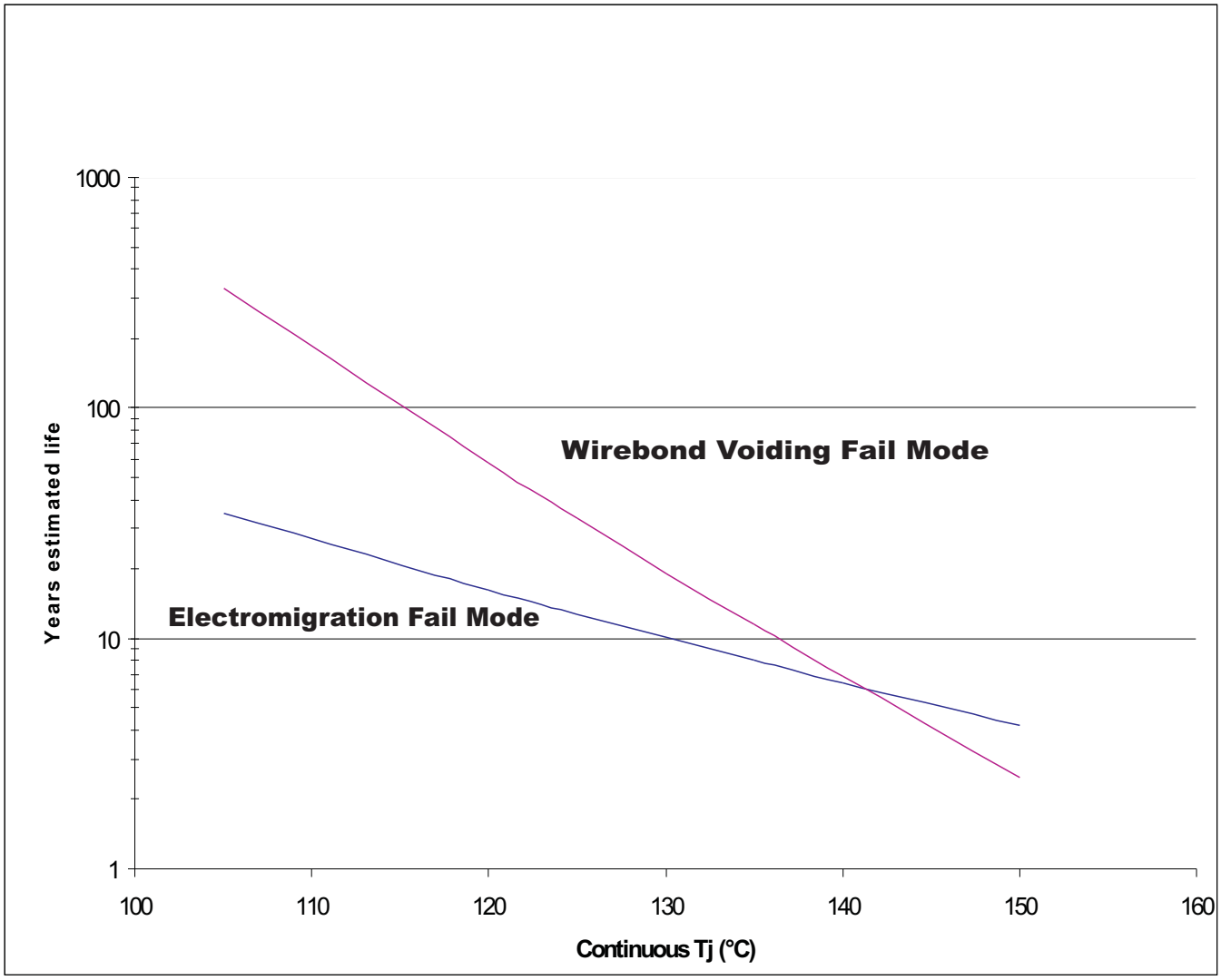
POWER DISSIPATION RATING TABLE

PACKAGE	SUFFIX	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING (mW) T_A = 70°C	DERATING FACTOR ABOVE 70°C (mW/°C)
MSOP-8 PowerPAD(1)	DGN	4.7	50 – 59	1370(2)	17.1(2)
SOIC 8	D	42	84 - 160	344 - 655(3)(4)	6.25 - 11.9(3)(4)

(1) The PowerPAD package is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.
(2) 150°C operating junction temperature is used for power-rating calculations.
(3) The range of values indicates the effect of PC board. These values are intended to give the system designer an indication of the best- and worst-case conditions. In general, the system designer should attempt to use larger traces on the PC board, where possible, in order to spread the heat away from the device more effectively. For information on the PowerPAD package, refer to technical brief, *PowerPad™ Thermally-Enhanced Package*, literature number SLMA002, and application brief, *PowerPad™ Made Easy*, literature number SLMA004.
(4) 125°C operating junction temperature is used for power-rating calculation.

Table 1. Inputs/Outputs

		INPUTS (VIN_L, VIN_H)		OUTPUTS	
ENBA	ENBB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	X	X	L	L



A. See Datasheet for Absolute Maximum and Minimum Recommended Operating Conditions.

B. Silicon Operating Life Design Goal is 10 years @ 105°C Junction Temperature (does not include package interconnect life).

C. Enhanced Plastic Product Disclaimer Applies.

Figure 1. UCC27424MDGNREP Operating Life Derating Chart

Absolute Maximum Ratings(1) (2)

over operating free-air temperature range (unless otherwise noted)

				MN	MAX	UNIT
V_{DD}	Supply voltage range			–0.3	16	V
	Output current	OUTA, OUTB	DC, I_{OUT_DC}		0.2	A
			Pulsed (0.5 µs), I_{OUT_PULSED}		4.5	
V_{IN}	Input voltage range	INA, INB			–5 to 6 or V_{DD} + 0.3 (whichever is larger)	V
	Enable voltage	ENBA, ENBB			–0.3 to 6 or V_{DD} + 0.3 (whichever is larger)	V
	Power dissipation at T_A = 25°C	D package			650	mW
		DGN package			3	W
T_J	Junction operating temperature range			–55	150	°C
T_{stg}	Storage temperature range			–65	150	°C
	Lead temperature (soldering, 10 s)				300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

Electrical Characteristics

V_{DD} = 4.5 V to 15 V, T_A = –55°C to 125°C, T_A = T_J (unless otherwise noted)

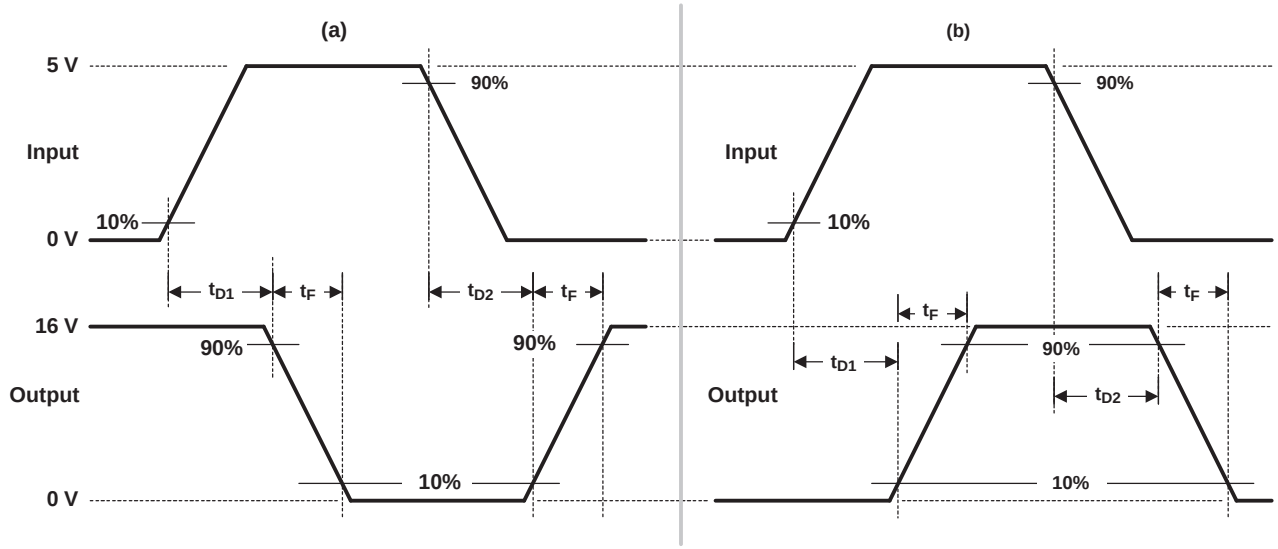
PARAMETER		TEST CONDITIONS		UCC27423			UCC27424			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Input (INA, INB)										
V_{IN_H}	Logic 1 input threshold			2			2			V
V_{IN_L}	Logic 0 input threshold					1			1	V
	Input current	0 V ≤ V_{IN} ≤ V_{DD}		–10	0	10	–10	0	10	µA
Output (OUTA, OUTB)										
	Output current	V_{DD} = 14 V(1) (2)			4			4		A
V_{OH}	High-level output voltage	V_{OH} = V_{DD} – V_{OUT}, I_{OUT} = –10 mA			330	450		330	450	mV
V_{OL}	Low-level output level	I_{OUT} = 10 mA			22	40		22	40	mV
	Output resistance high	I_{OUT} = –10 mA, V_{DD} = 14 V(3)	T_A = 25°C	25	30	35	25	30	35	Ω
			T_A = full range	14		45	18		45	
	Output resistance low	I_{OUT} = –10 mA, V_{DD} = 14 V(3)	T_A = 25°C	1.9	2.2	2.5	1.9	2.2	2.5	Ω
			T_A = full range	0.95		4	1.2		4	
	Latch-up protection(1)			500			500			mA
Switching Time										
t_R	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF(1)			20	40		20	40	ns
t_F	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF(1)			15	40		15	40	ns
t_{D1}	Delay, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF(1)			35	55		35	50	ns
t_{D2}	Delay, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF(1)			25	60		25	45	ns
Enable (ENBA, ENBB)										
V_{IN_H}	High-level input voltage	LOW-to-HIGH transition		1.7	2.4	3.1	1.7	2.4	2.9	V
V_{IN_L}	Low-level input voltage	HIGH-to-LOW transition		1.1	1.8	2.3	1.1	1.8	2.2	V
	Hysteresis			0.13	0.55	1.1	.10	0.55	0.9	V
R_{ENBL}	Enable impedance	V_{DD} = 14 V, ENBL = GND		75	100	160	75	100	140	kΩ
t_{D3}	Propagation delay time(4)	C_{LOAD} = 1.8 nF(1)			30	60		30	60	ns
t_{D4}	Propagation delay time(4)	C_{LOAD} = 1.8 nF(1)			100	150		100	150	ns

(1) Specified by design. Not tested in production.
(2) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.
(4) See Figure 2

Electrical Characteristics (continued)

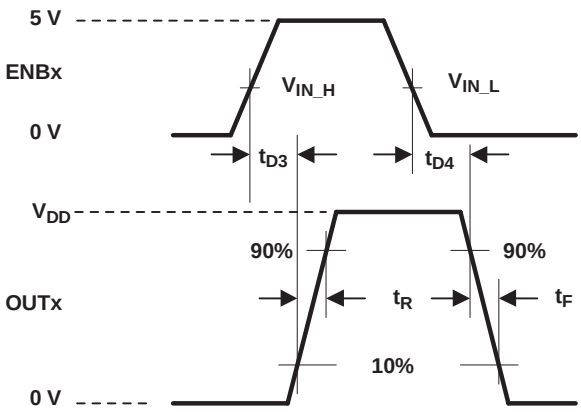
V_{DD} = 4.5 V to 15 V, T_A = –55°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS		UCC27423			UCC27424			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Overall										
I_{DD}	Static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	INA = 0 V	INB = 0 V		900	1350		300	450	µA
			INB = HIGH		750	1100		750	1100	
		INA = HIGH	INB = 0 V		750	1100		750	1100	
			INB = HIGH		600	900		1200	1800	
	Disabled, V_{DD} = 15 V, ENBA = ENBB = 0 V	INA = 0 V	INB = 0 V		300	450		300	450	
			INA = HIGH		450	700		450	700	
		INA = HIGH	INB = 0 V		450	700		450	700	
			INB = HIGH		600	900		600	900	



D. The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 2. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver



E. The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 3. Switching Waveform for Enable to Output

APPLICATION INFORMATION

General Information

High-frequency power supplies often require high-speed, high-current drivers such as the UCC27423 and UCC27424. A leading application is the need to provide a high-power buffer stage between the pulse-width modulation (PWM) output of the control IC and the gates of the primary power MOSFET or insulated gate bipolar transistor (IGBT) switching devices. In other cases, the driver IC is used to drive the power-device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices, which can present an extremely large load to the control circuitry.

Driver ICs are used when it is not feasible to have the primary PWM regulator IC directly drive the switching devices, for one or more reasons. The PWM IC may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases, there may be a desire to minimize the effect of high-frequency switching noise by placing the high-current driver physically close to the load. Also, newer ICs that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are intended to drive only the high-impedance input to drivers such as the UCC27423 and UCC27424. Finally, the control IC may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltages, yet, they are equally compatible with 0 to V_{DD} signals. The inputs of the UCC27423 and UCC27424 are designed to withstand 500-mA reverse current without either damage to the IC or logic upset. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow-changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an effort to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, limit the rise or fall times to the power device. Then, an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor also may help remove power dissipation from the device package, as discussed in the section on Thermal Considerations.

Output Stage

Inverting outputs of the UCC27423 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC27424 are intended to drive external N-channel MOSFETs.

Each output stage is capable of supplying ±4-A peak current pulses and swings to both VDD and GND. The pullup/ pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot, due to the body diode of the external MOSFET. This means that, in many cases, external Schottky clamp diodes are not required.

The UCC27423 family delivers the 4-A gate drive where it is most needed during the MOSFET switching transition - at the Miller plateau region - providing efficiency gains. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC27423 and UCC27424 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. [1]

Two circuits are used to test the current capabilities of the UCC27423 driver. In each case external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test, there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made 200 ns after the input pulse is applied, following the initial transient.

The first circuit in Figure 4 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC27423 is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

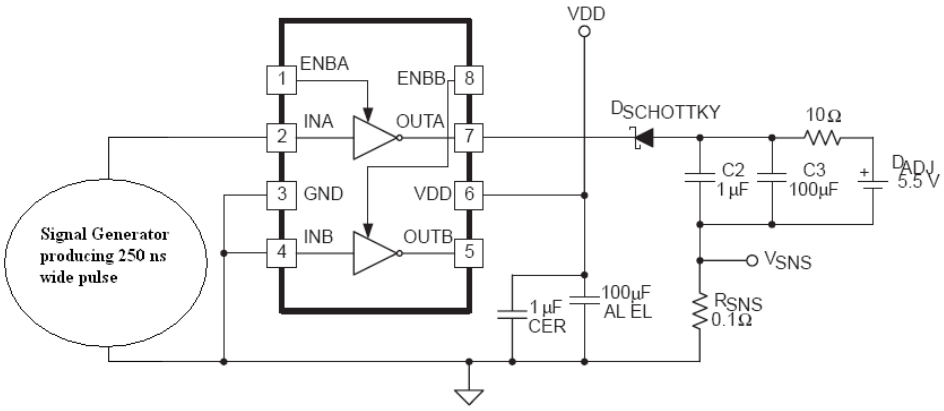


Figure 4. Current Sinking

The circuit shown in Figure 5 is used to test the current source capability, with the output clamped to around 5 V with a string of Zener diodes. The UCC27423 is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

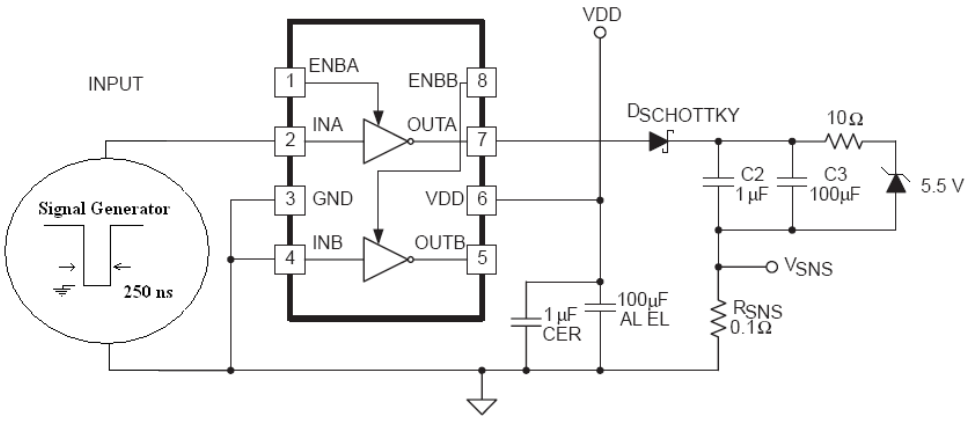


Figure 5. Current Sourcing

It should be noted that the current sink capability is slightly stronger than the current source capability at lower VDD. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET, and the current sink has an N-channel MOSFET.

In a large majority of applications, it is advantageous that the turn-off capability of a driver is stronger than the turn-on capability. This helps to ensure that the MOSFET is held OFF during common power-supply transients, which may turn the device back ON.

Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together and the OUTA/OUTB outputs together. Then, a single signal can control the paralleled combination as shown in Figure 6.

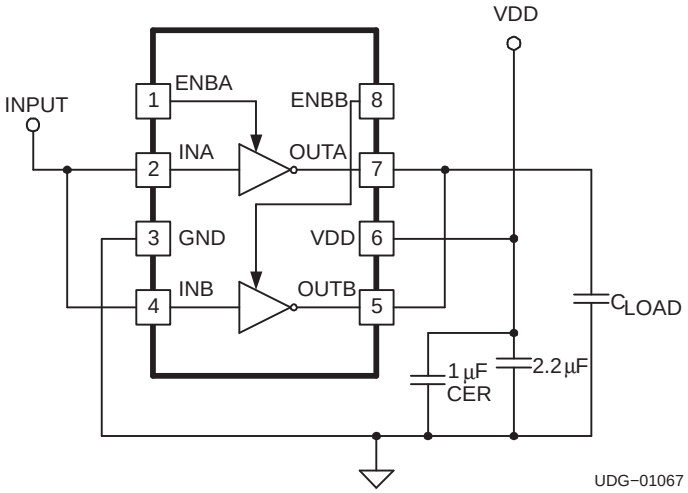


Figure 6. Parallel Outputs

Operational Waveforms and Circuit Layout

Sink and source currents of the driver are dependent upon VDD value and the output capacitive load. The larger the VDD value, the higher the current capability. Also, the larger the capacitive load, the higher the current and source capabilities.

Trace resistance and inductance, including wires and cables for testing, slow down the rise and fall times of the outputs. Thus, the driver's current capabilities are reduced.

To achieve higher current results, reduce resistance and inductance on the board as much as possible and increase the capacitive output load value in order to swamp out the effect of the inductance values.

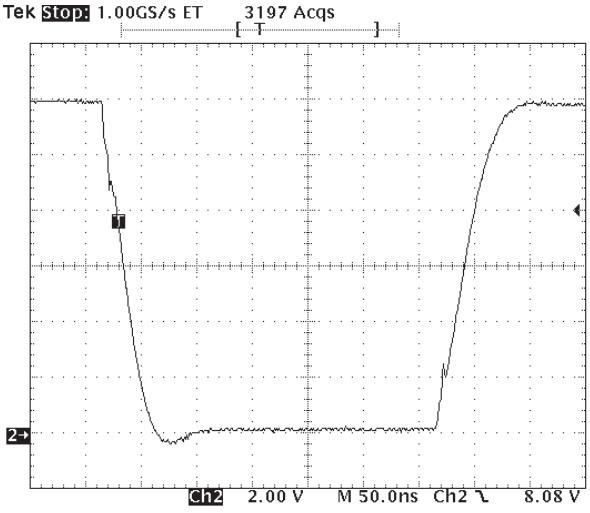


Figure 7. Pulse Response

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. It is advantageous to connect the driver IC as close as possible to the leads. The driver IC layout has ground on the opposite side of the output, so the ground should be connected to the bypass capacitors and the load with copper trace, as wide as possible. These connections also should be made with a small enclosed loop area to minimize the inductance.

VDD

Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

I_{OUT} = Qg × f, where f is frequency

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located closest to the VDD-to-ground connection. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel, to help deliver the high-current peaks to the load. The parallel combination of capacitors should present a low-impedance characteristic for the expected current levels in the driver application.

Drive Current and Power Requirements

The UCC27423 and UCC27424 are capable of delivering 4-A of current to a MOSFET gate for a period of several-hundred nanoseconds. High-peak current is required to turn the device ON quickly. To turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power-conversion equipment.

References 1 and 2 discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference 2 includes information on the previous generation of bipolar IC gate drivers.

When a driver IC is tested with a discrete, capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$E = \frac{1}{2}CV^2$, where C is the load capacitor and V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss, given by the following:

$P = 2 \times \frac{1}{2}CV^2f$, where f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

P = 10 nF × $(12)^2$ × (300 kHz) = 0.432 W

With a 12-V supply, this equates to a current of:

$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 0.036\ A$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption should be considered. With no load, the IC current draw is 0.0027 A. Under this condition, the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable, current due to cross conduction in the output stages of the driver. However, these small current differences are buried in the high-frequency switching spikes and are beyond the measurement capabilities of a basic laboratory setup. The measured current with a 10-nF load is reasonably close to that which is predicted.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance, plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge, Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, Qg = CeffV, to provide the following equation for power:

$P = C \times V^2 \times f = Q_g \times f$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

Enable

The UCC27423 and UCC27424 provide dual enable inputs for improved control of each driver channel operation. The inputs incorporate logic-compatible thresholds with hysteresis. They are pulled internally up to V_{DD} with a 100-kΩ resistor for active-high operation. When ENBA and ENBB are driven high, the drivers are enabled and, when ENBA and ENBB are low, the drivers are disabled. The default state of the enable pin is to enable the driver and, therefore, can be left open for standard operation. The output states when the drivers are disabled is low, regardless of the input state. See Table 1 for a truth table of the operation using enable logic.

Enable inputs are compatible with both logic signals and slow-changing analog signals. They can be driven directly or a power-up delay can be programmed with a capacitor between ENBA, ENBB, and AGND. ENBA and ENBB control input A and input B, respectively.

THERMAL INFORMATION

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. In order for a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced, while keeping the junction temperature within rated limits.

As shown in the power-dissipation rating table, the SOIC-8 (D) package has a power rating of around 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in our earlier example is 0.432 W with a 10-nF load, 12 VDD, switched at 300 kHz. Thus, only one load of this size could be driven using the D package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

The MSOP-8 PowerPAD (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As shown in reference 3, the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the IC package, reducing the θjc down to 4.7°C/W. Data is presented in reference 3 to show that the power dissipation can be quadrupled in the PowerPAD package configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat-removal subsystem, as summarized in Reference 4. This allows a significant improvement in heatsinking over that available in the D package and is shown to more than double the power capability of the D package. Note that the PowerPAD package is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

References

1. Power Supply Seminar SEM-1400 Topic 2: *Design and Application Guide For High-Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments literature number SLUP133.
2. Application note, *Practical Considerations in High-Performance MOSFET, IGBT, and MCT Gate Drive Circuits*, by Bill Andreycak, Texas Instruments literature number SLUA105.
3. Technical brief, *PowerPad™ Thermally-Enhanced Package*, Texas Instruments literature number SLMA002.
4. Application brief, *PowerPad™ Made Easy*, Texas Instruments literature number SLMA004.

Table 2. Related Products

PRODUCT	DESCRIPTION	PACKAGES
UCC37324	Dual 4-A low-side drivers	MSOP-8 PowerPAD, SOIC-8, PDIP-8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY (VDD = 4.5 V)

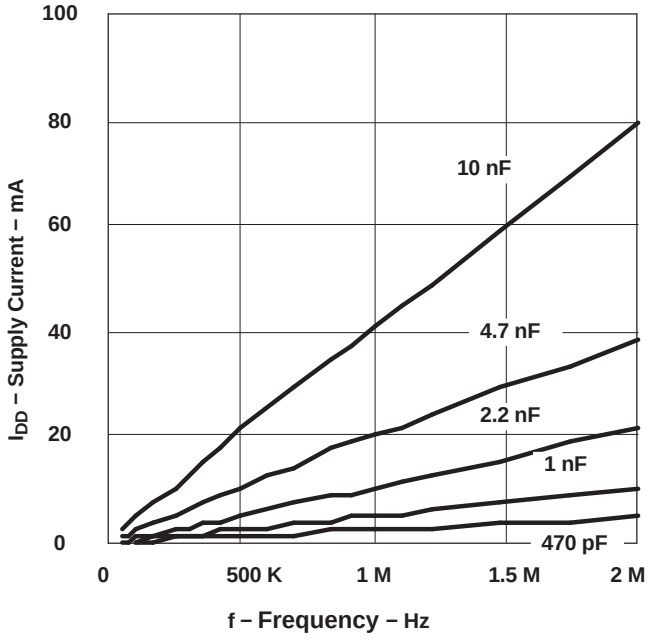


Figure 8.

SUPPLY CURRENT
vs
FREQUENCY (VDD = 8 V)

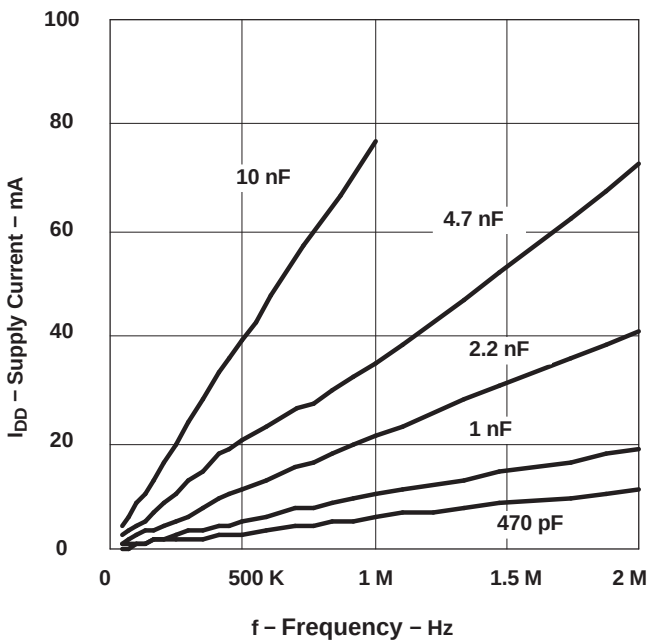


Figure 9.

SUPPLY CURRENT
vs
FREQUENCY (V_{DD} = 12 V)

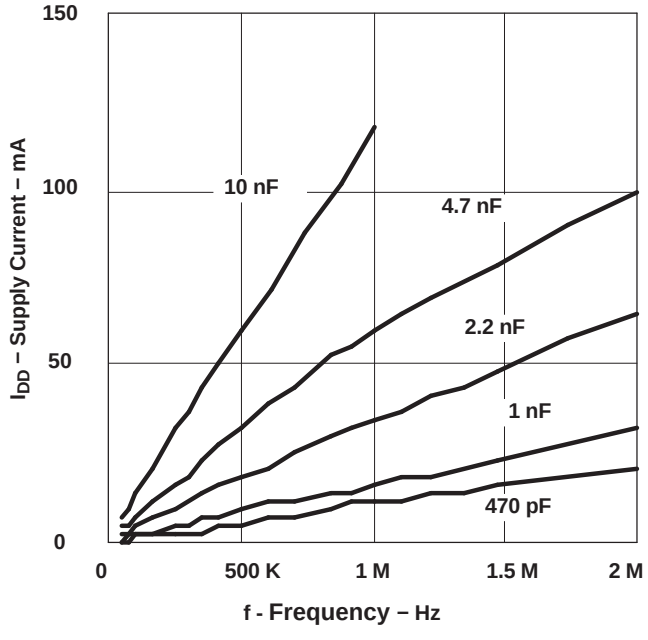


Figure 10.

SUPPLY CURRENT
vs
FREQUENCY (VDD = 15 V)

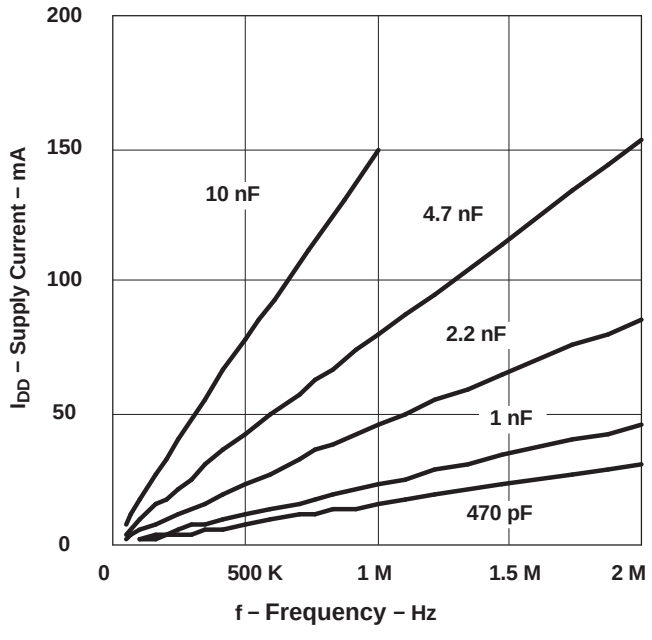


Figure 11.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE (C_{LOAD} = 2.2 nF)

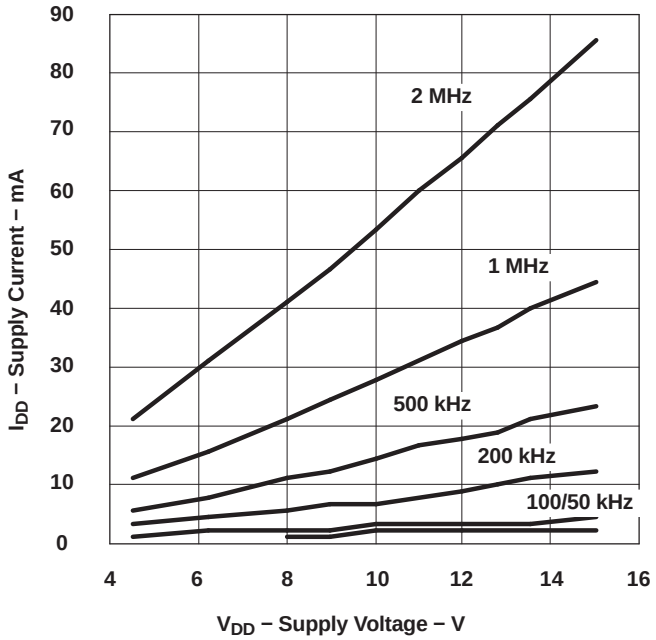


Figure 12.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE (C_{LOAD} = 4.7 nF)

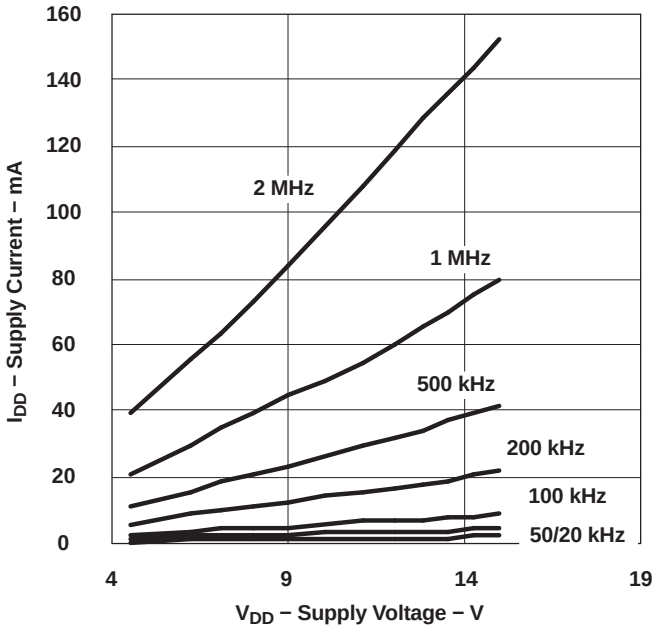


Figure 13.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

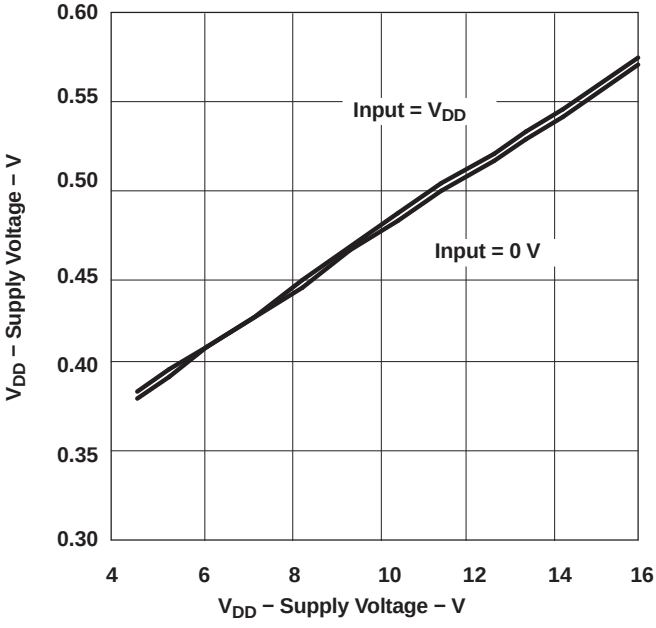


Figure 14.

RISE TIME
vs
SUPPLY VOLTAGE

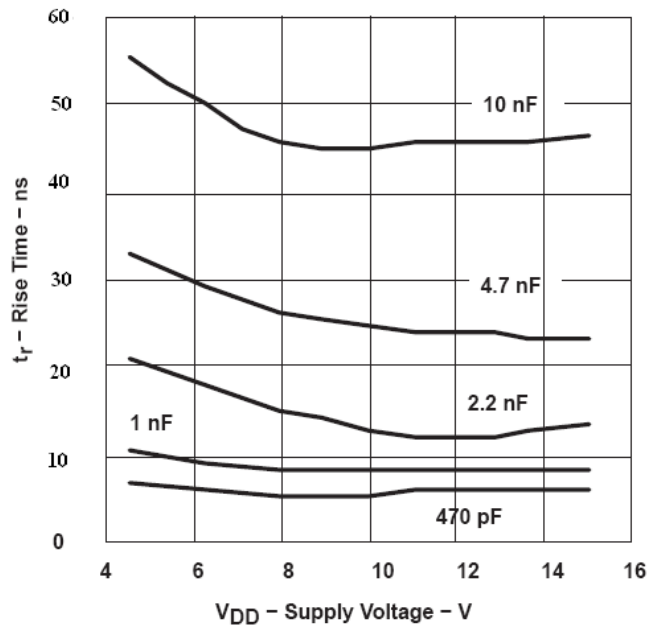


Figure 15.

TYPICAL CHARACTERISTICS (continued)

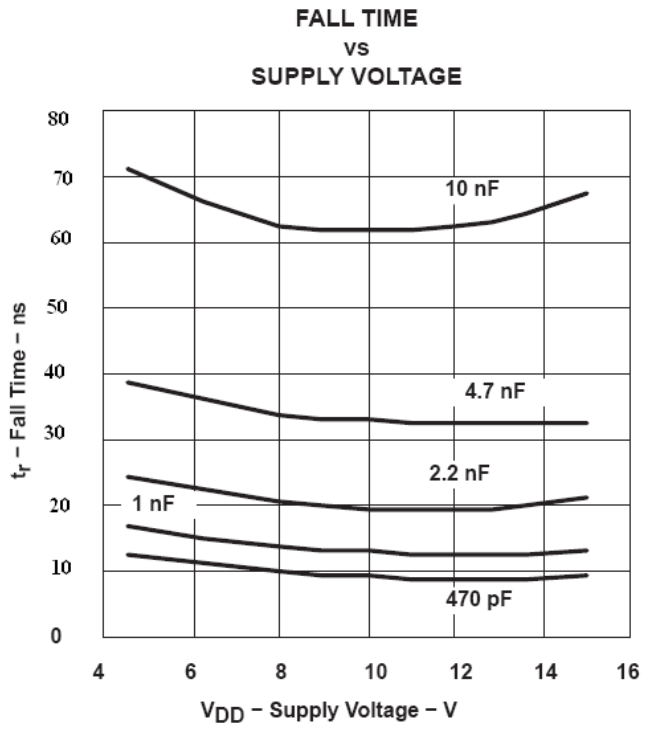


Figure 16.

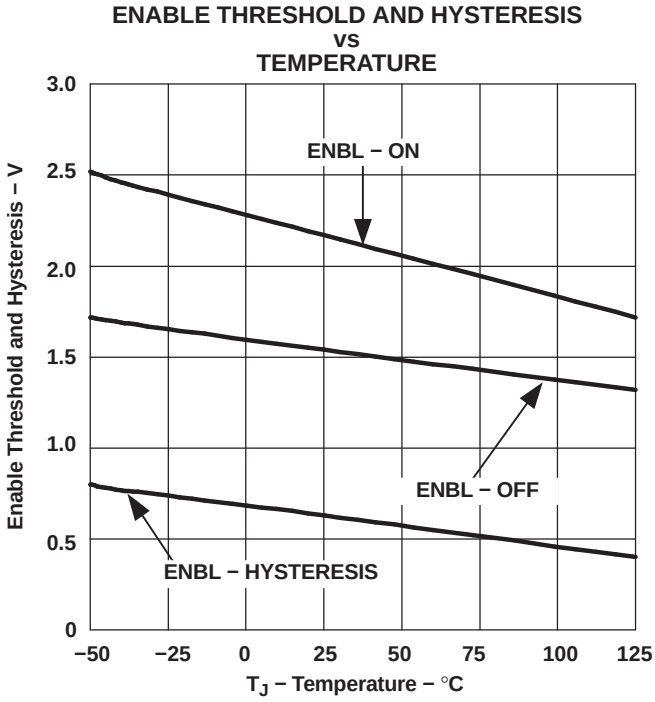


Figure 17.

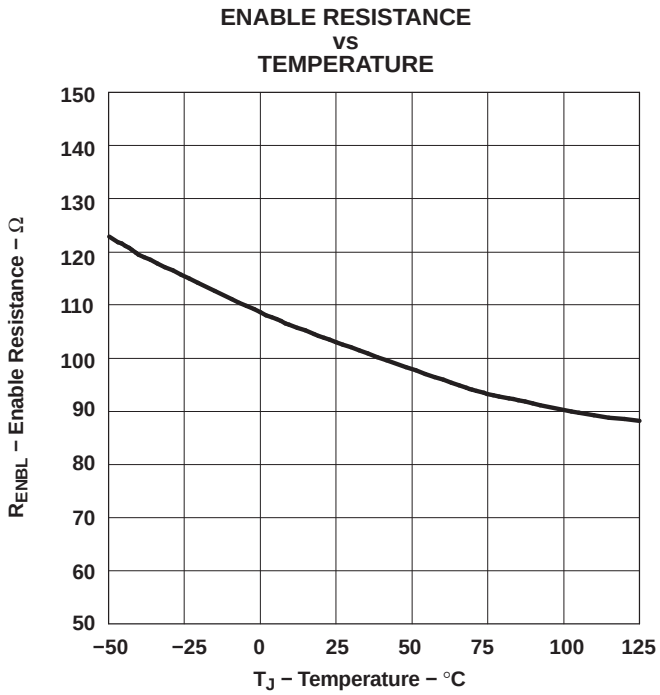


Figure 18.

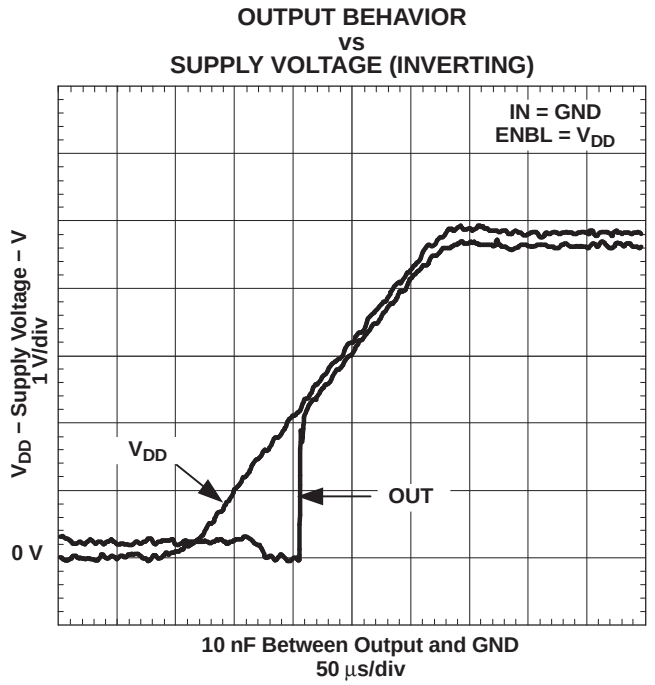


Figure 19.

TYPICAL CHARACTERISTICS (continued)

OUTPUT BEHAVIOR vs SUPPLY VOLTAGE (INVERTING)

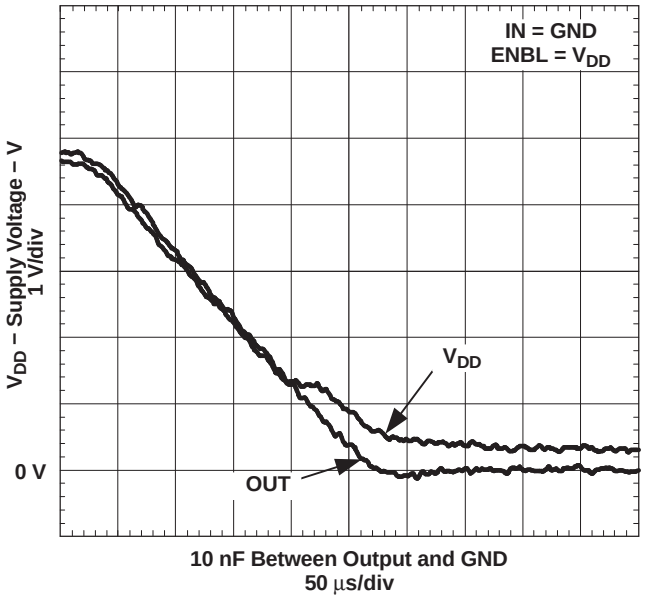


Figure 20.

OUTPUT BEHAVIOR vs VDD (INVERTING)

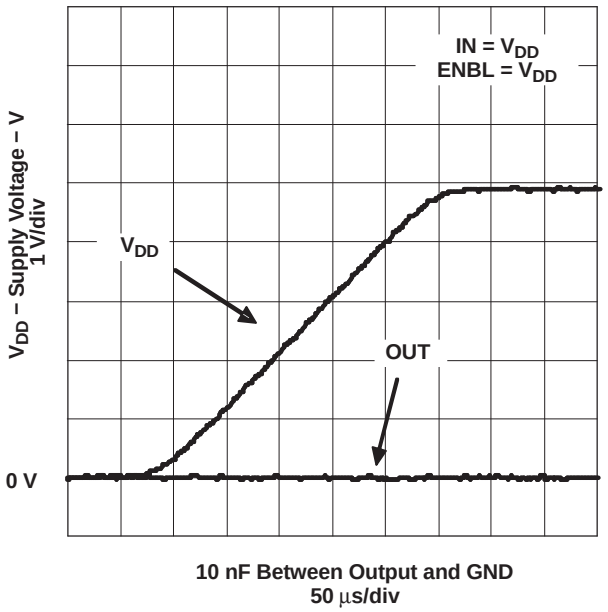


Figure 21.

OUTPUT BEHAVIOR vs VDD (INVERTING)

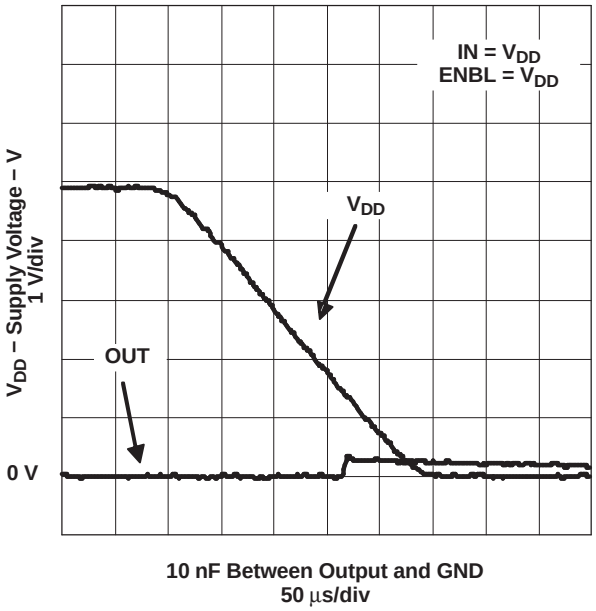


Figure 22.

OUTPUT BEHAVIOR vs VDD (NONINVERTING)

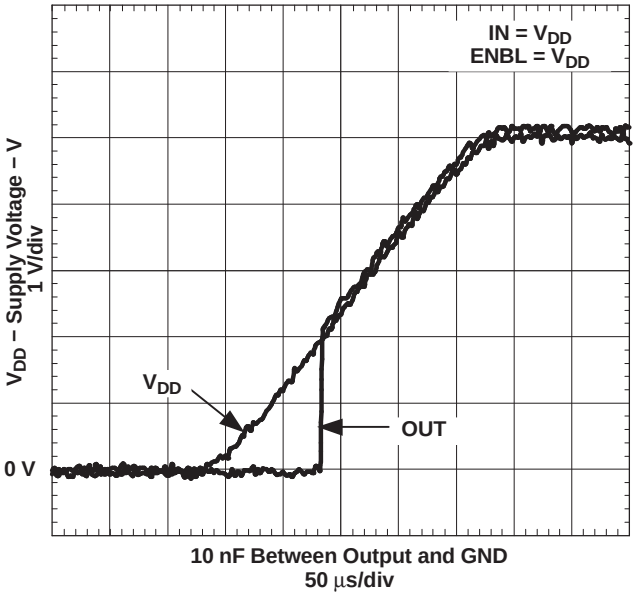


Figure 23.

TYPICAL CHARACTERISTICS (continued)

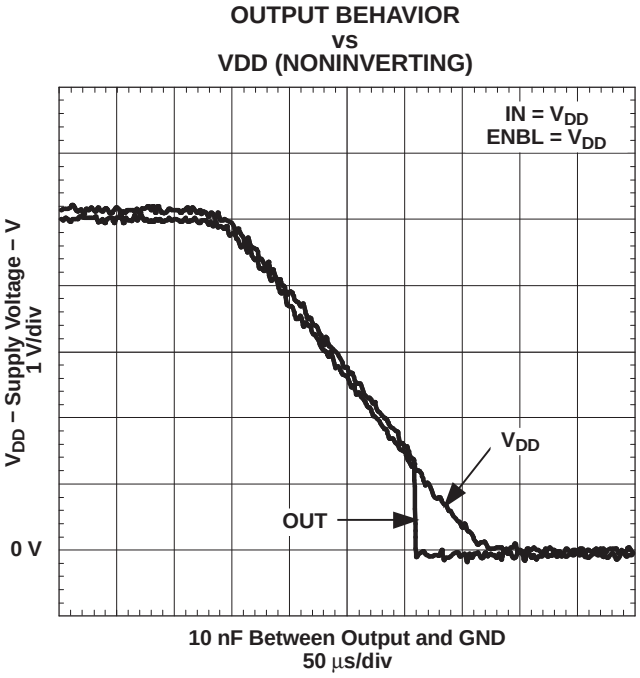


Figure 24.

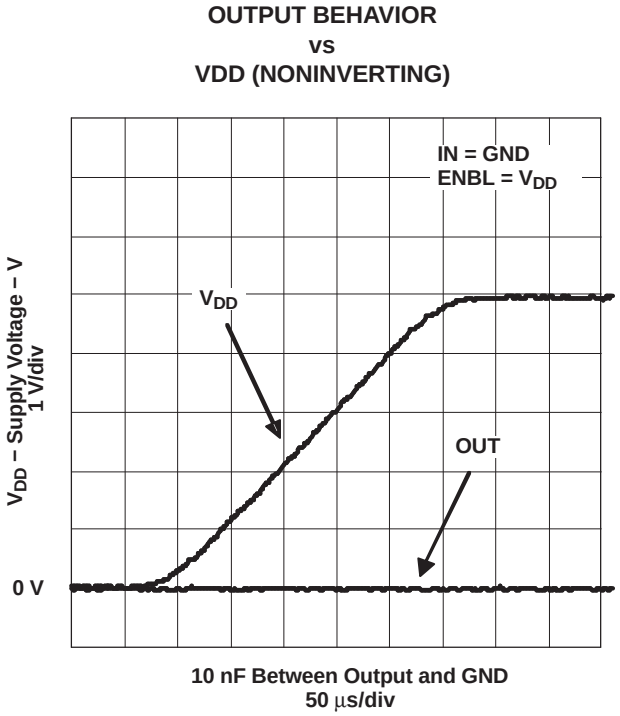


Figure 25.

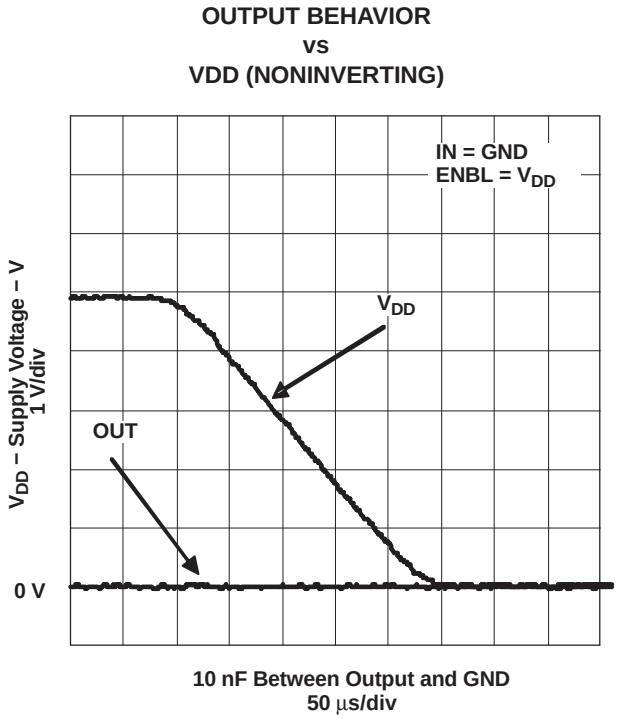


Figure 26.

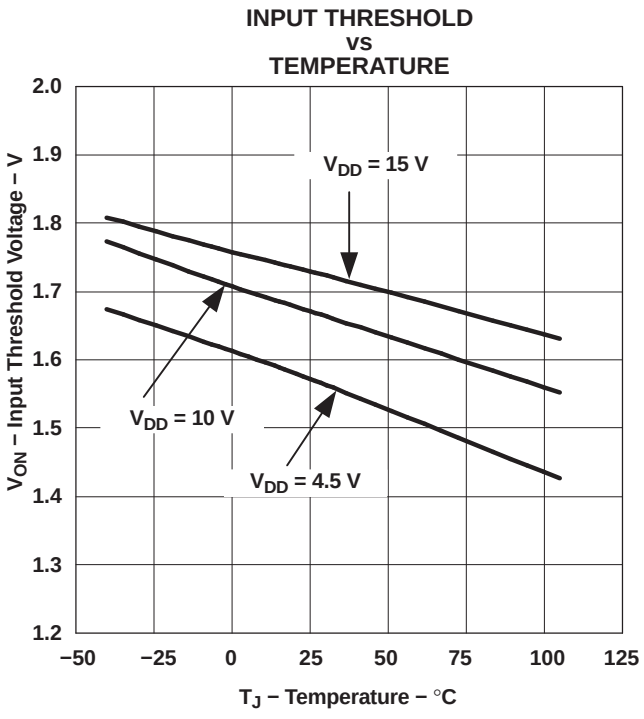


Figure 27.

REVISION HISTORY

Changes from Revision A (November, 2009) to Revision B **Page**

- Changed minimum supply voltage from 4-V to 4.5-V in FEATURES section 1
- Changed Figure 4. Current Sinking 9
- Changed Figure 5. Current Sourcing 9
- Changed first paragraph of Operational Waveforms and Circuit Layout section 10
- Changed Figure 15. RISE TIME vs SUPPLY VOLTAGE 15
- Changed Figure 16. FALL TIME vs SUPPLY VOLTAGE 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC27423MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	27423EP	Samples
UCC27424MDGNREP	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	424E	Samples
V62/07624-01XE	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	424E	Samples
V62/07624-02YE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	27423EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF UCC27423-EP, UCC27424-EP :

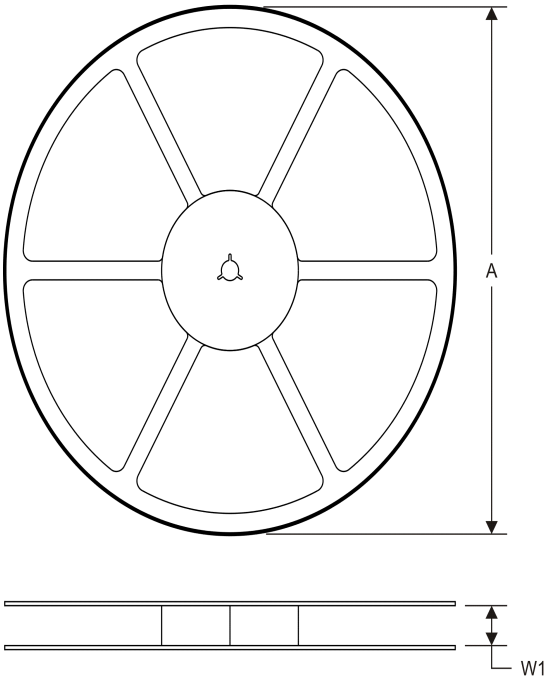
- Catalog: UCC27423, UCC27424
- Automotive: UCC27423-Q1, UCC27424-Q1

NOTE: Qualified Version Definitions:

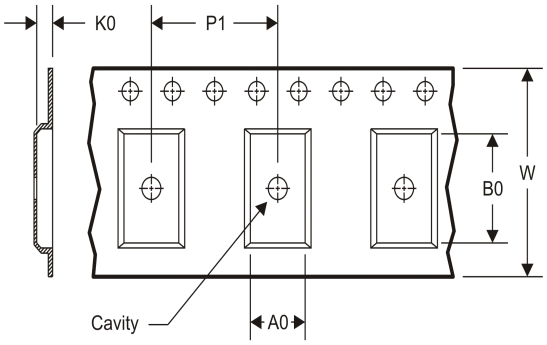
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



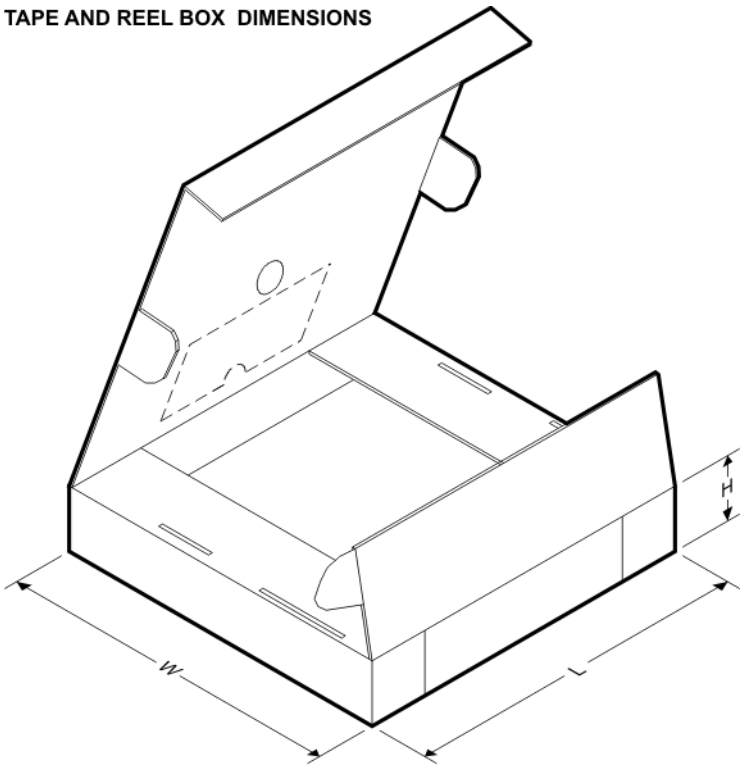
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27423MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424MDGNREP	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

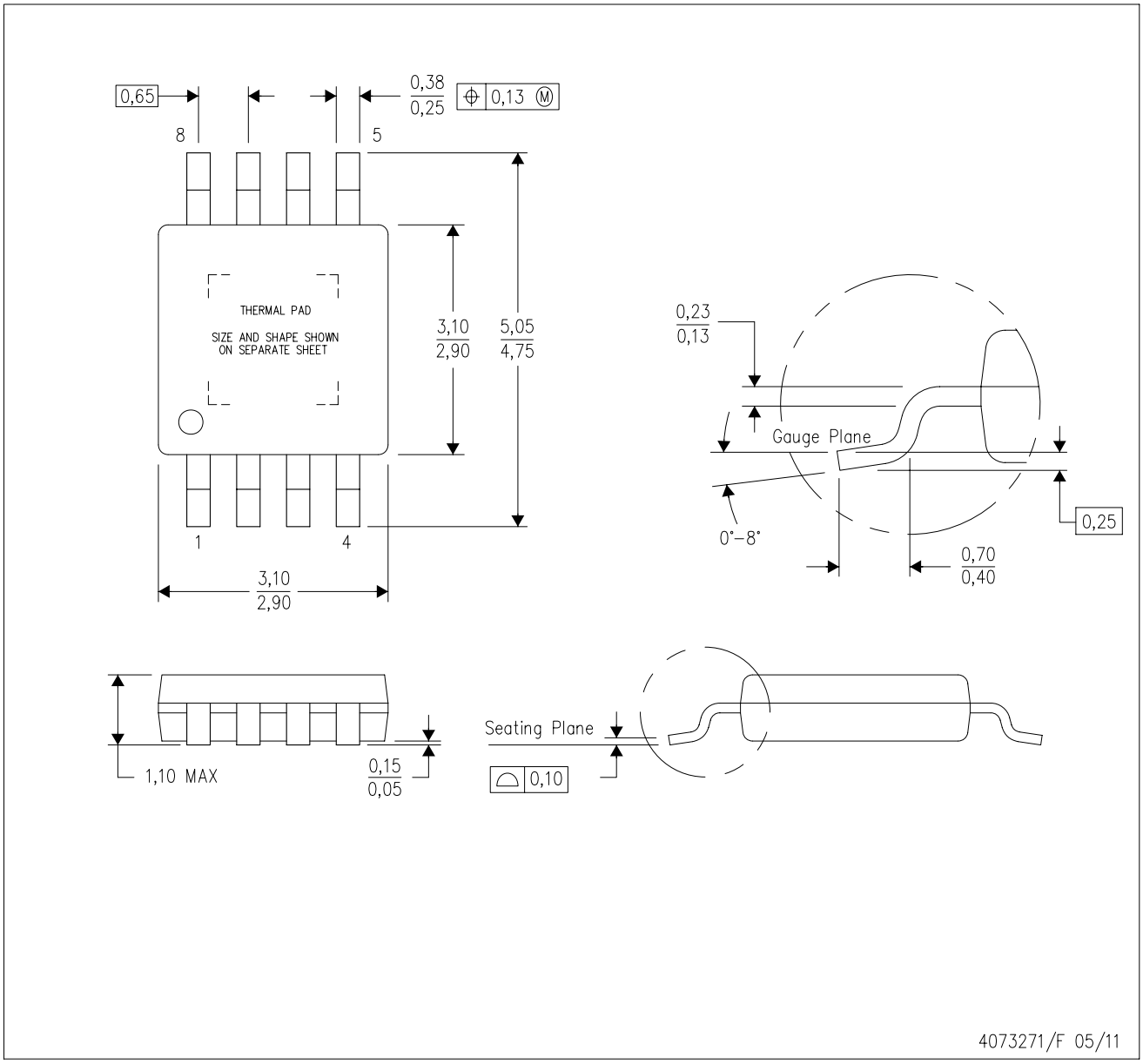
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27423MDREP	SOIC	D	8	2500	367.0	367.0	35.0
UCC27424MDGNREP	MSOP-PowerPAD	DGN	8	2500	367.0	367.0	35.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

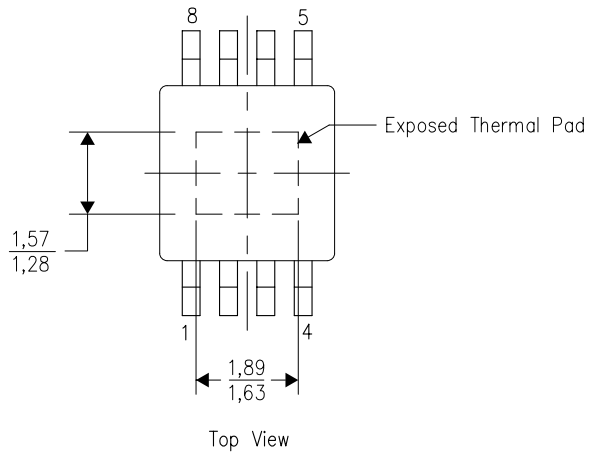
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

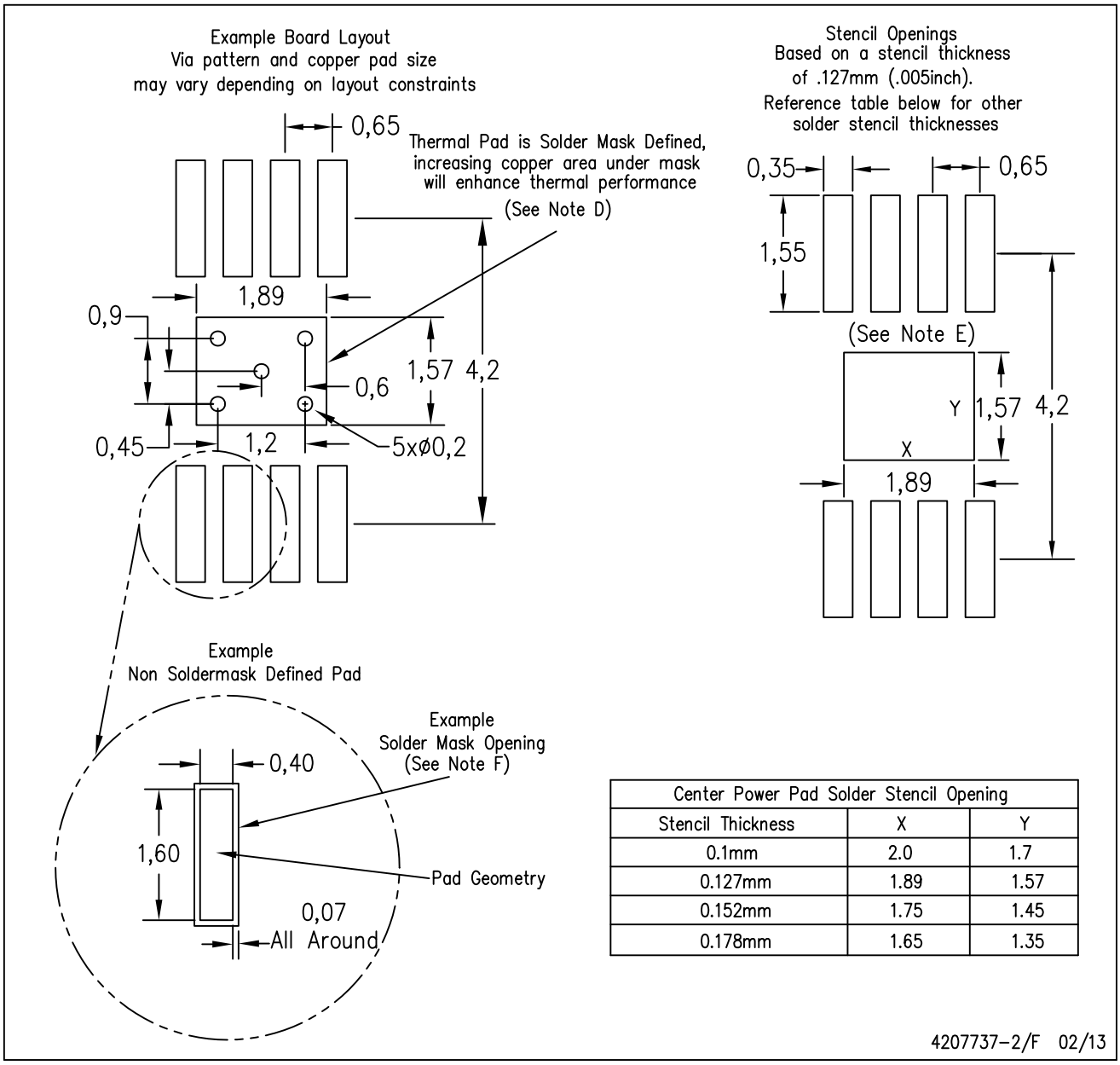
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

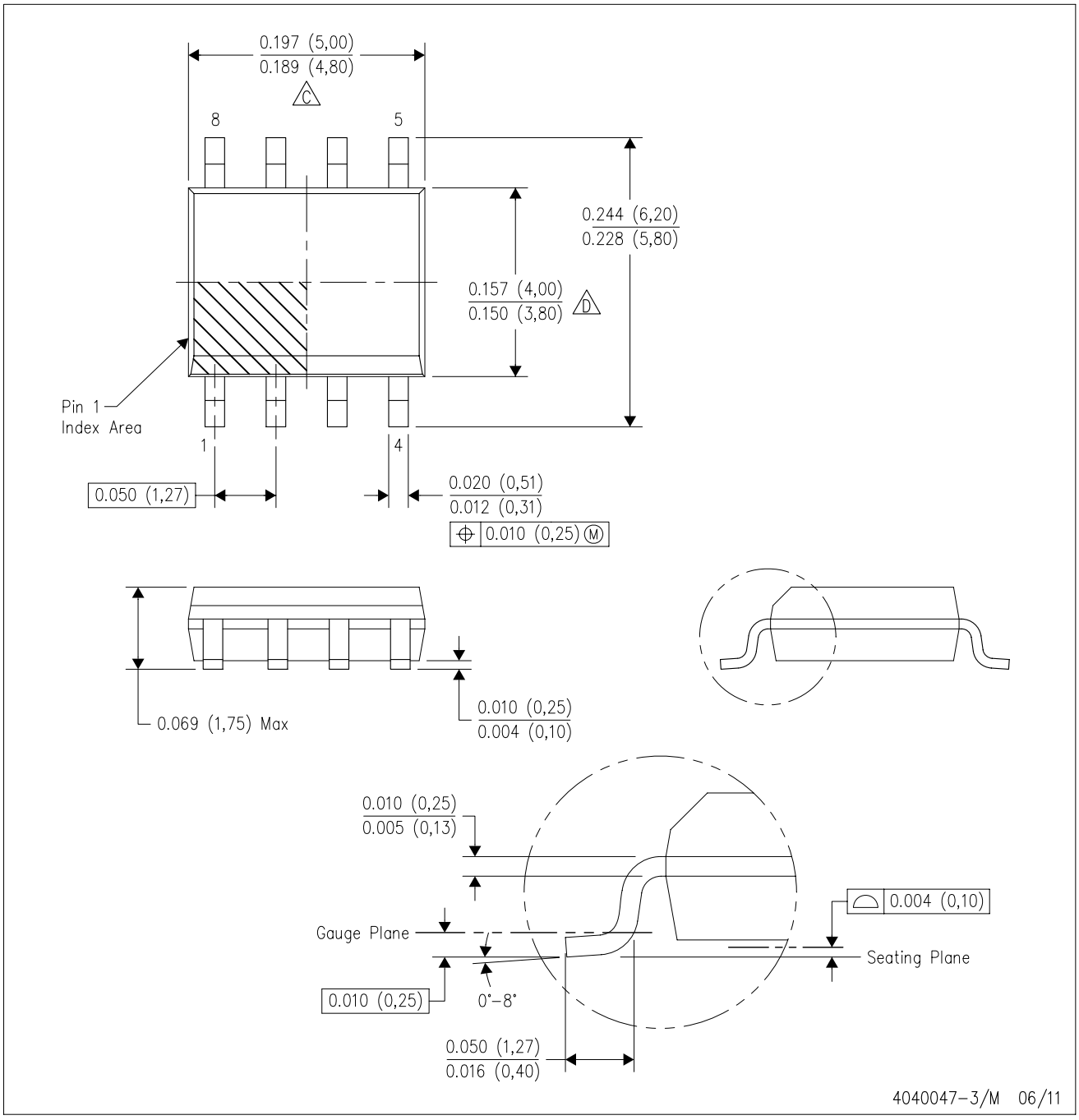


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

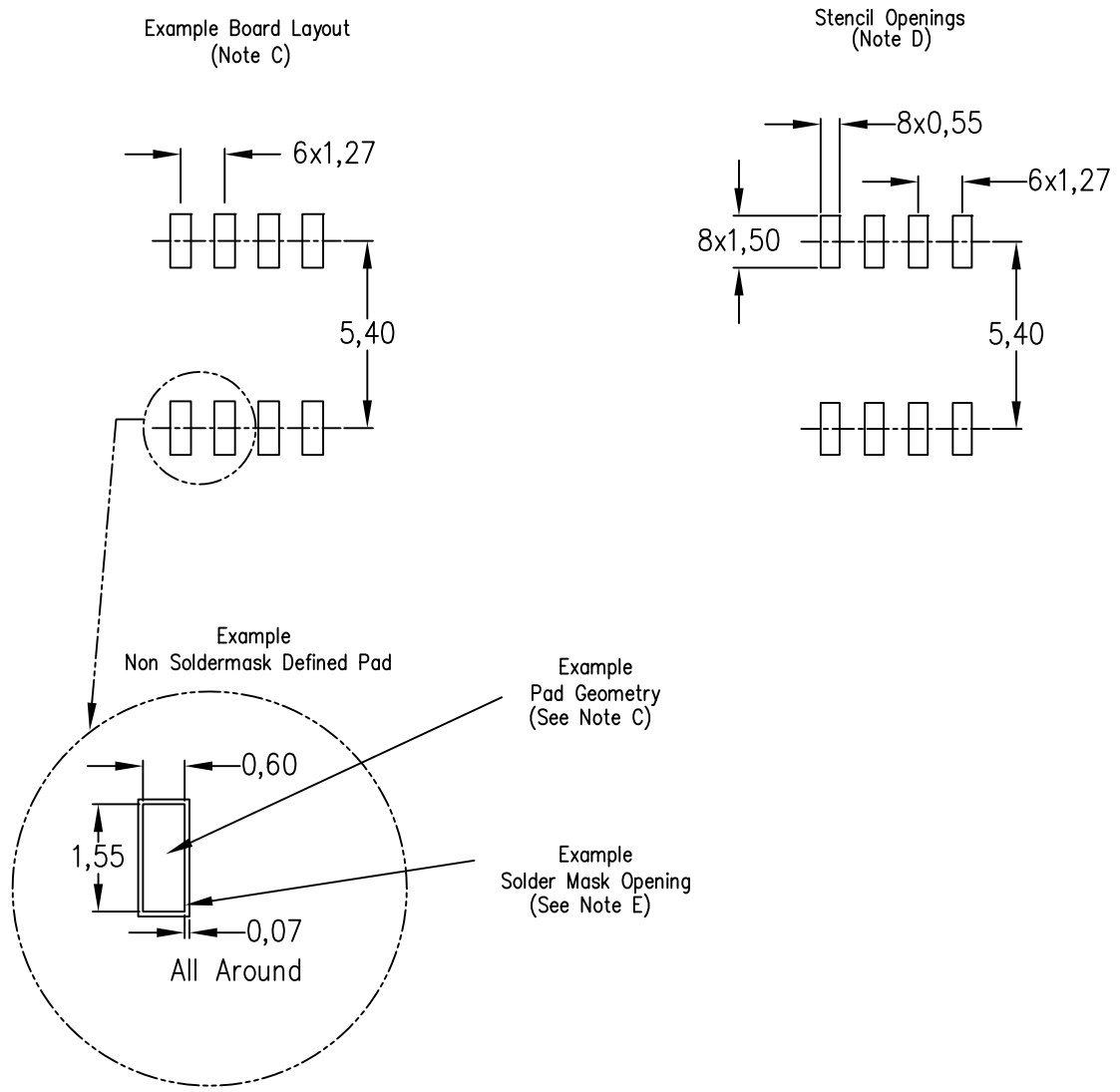
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
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