120-V BOOT, 3-A PEAK, HIGH-FREQUENCY HIGH-SIDE/LOW-SIDE DRIVER

FEATURES

- **Qualified for Automotive Applications**
- **Specified from –40°C to 140°C**
- **Drives Two N-Channel MOSFETs in High-Side/Low-Side Configuration**
- **Maximum Boot Voltage 120 V**
- **Maximum V_{DD} Voltage 20 V**
- **On-Chip 0.65-V VF, 0.6-Ω RD Bootstrap Diode**
- **Greater than 1 MHz of Operation**
- **20-ns Propagation Delay Times**
- **3-A Sink, 3-A Source Output Currents**
- **8-ns Rise/7-ns Fall Time with 1000-pF Load**
- **1-ns Delay Matching**
- **Undervoltage Lockout for High-Side and Low-Side Driver**

APPLICATIONS

- **Power Supplies for Telecom, Datacom, and Merchant Markets**
- **Half-Bridge Applications and Full-Bridge Converters**
- **Isolated Bus Architecture**
- **Two-Switch Forward Converters**
- **Active-Clamp Forward Converters**
- **High-Voltage Synchronous-Buck Converters**
- **Class-D Audio Amplifiers**

DESCRIPTION

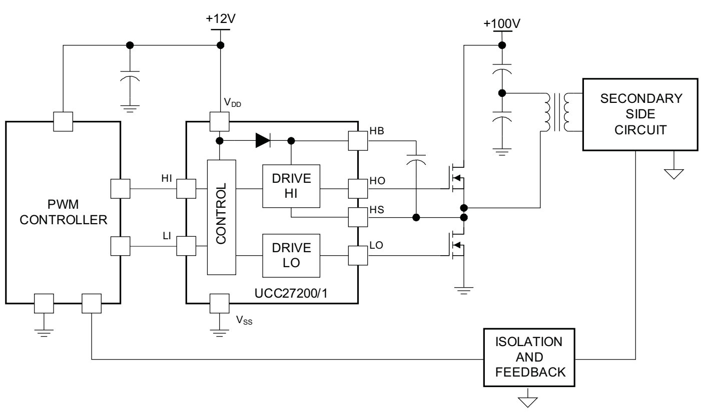
The UCC27200/1 family of high-frequency N-channel MOSFET drivers include a 120-V bootstrap diode and high-side/low-side driver with independent inputs for maximum control flexibility. This allows for N-channel MOSFET control in half-bridge, full-bridge, two-switch forward, and active clamp forward converters. The low-side and the high-side gate drivers are independently controlled and matched to 1 ns between the turn-on and turn-off of each other.

An on-chip bootstrap diode eliminates the external discrete diodes. Undervoltage lockout is provided for both the high-side and the low-side drivers, forcing the outputs low if the drive voltage is below the specified threshold.

Two versions of the UCC2720x are offered – the UCC27200 has high-noise-immune CMOS input thresholds, and the UCC27201 has TTL-compatible thresholds.

Both devices are offered in the 8-pin PowerPad™ SOIC (DDA) package.

Simplified Application Diagram



ORDERING INFORMATION(1)

T_J	INPUT COMPATIBILITY	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 140°C	CMOS	PowerPad – DDA	Reel of 2500	UCC27200QDDARQ1	27200Q
	TTL			UCC27201QDDARQ1	27201Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature (unless otherwise noted)

V_{DD}	Supply voltage range		–0.3 V to 20 V
V_{LI}, V_{HI}	Input voltages on LI and HI		–0.3 V to 20 V
V_{LO}	Output voltage on LO	DC	–0.3 V to V_{DD} + 0.3 V
		Repetitive pulse < 100 ns	–2 V to V_{DD} + 0.3 V
V_{HO}	Output voltage on HO	DC	V_{HS} – 0.3 V to V_{HB} + 0.3 V
		Repetitive pulse < 100 ns	V_{HS} – 2 V to V_{HB} + 0.3 V, (V_{HB} – V_{HS} < 20)
V_{HS}	HS voltage range	DC	–1 V to 120 V
		Repetitive pulse < 100 ns	–5 V to 120 V
V_{HB}	HB voltage range		–0.3 V to 120 V
	HB-HS voltage range		–0.3 V to 20 V
T_J	Operating virtual-junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
T_{lead}	Lead temperature	Soldering, 10 seconds	300°C
P_D	Power dissipation	T_A = 25°C(3)	2.7 W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to V_{SS}. Currents are positive into, negative out of the specified terminal.
(3) This data was taken using the JEDEC proposed high-K test PCB (See *Thermal Characteristics* for details).

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range		8	12	17	V
V_{HS}	HS voltage		–1		105	V
	HS voltage (repetitive pulse <100 ns)		–5		110	
V_{HB}	HB voltage		V_{HS} + 8, V_{DD} – 1		V_{HS} + 17, 115	V
	Voltage slew rate on HS				50	V/ns
T_J	Operating junction temperature		–40		140	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)			2000	V
		Charged-Device Model (CDM)			1000	

THERMAL CHARACTERISTICS

over operating free-air temperature range, maximum power dissipation at ambient temperature: $P_D = (150 – T_A)/\theta_{JA}$ (unless otherwise noted)

PACKAGE	θ_{JA} (JUNCTION TO AMBIENT)	θ_{JC} (JUNCTION TO CASE)	θ_{JP} (JUNCTION TO THERMAL PAD)
DDA[(1)]	46°C/W	71°C/W	4.8°C/W

(1) Test board conditions:
a. 3-in × 3-in, four layers, 0.062-in thickness
b. 2-oz copper traces located on the top and bottom of the PCB
c. 2-oz copper ground planes on the internal two layers
d. Six thermal vias in the PowerPad area under the device package

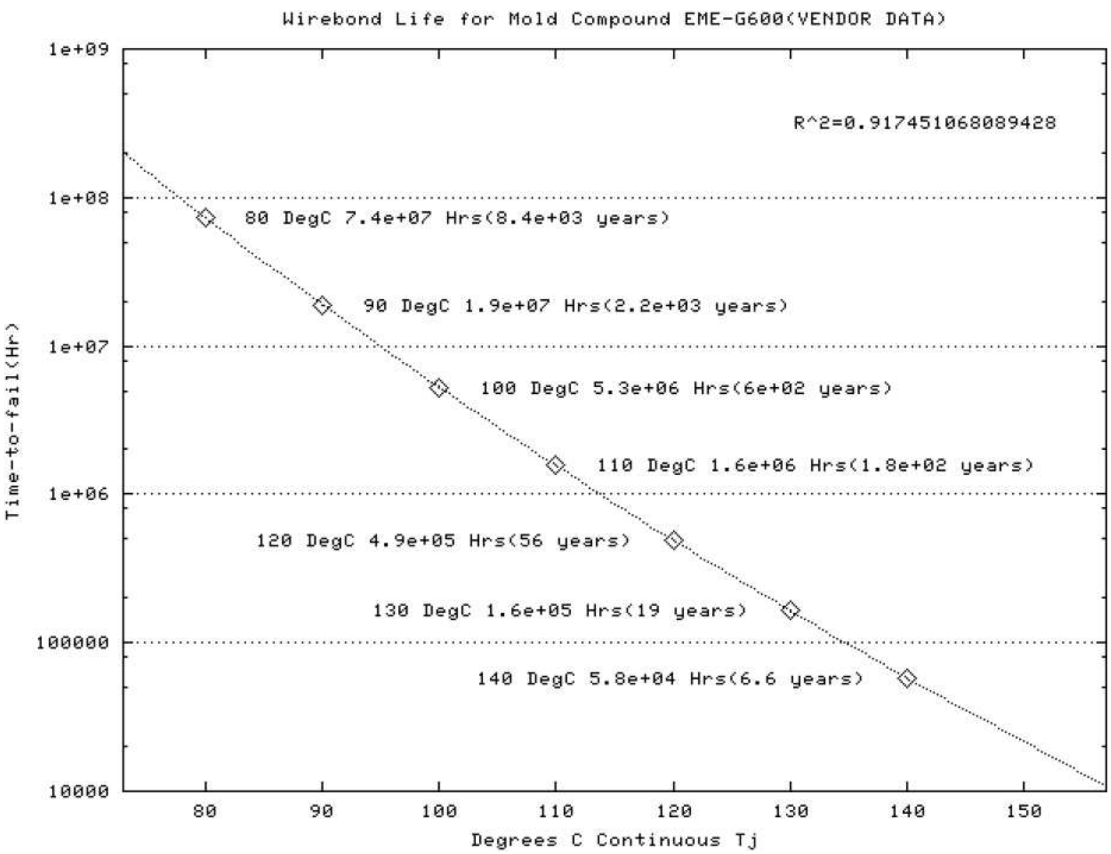


Figure 1. Wirebond Life

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_A = T_J = –40°C to 140°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply Currents								
I_{DD}	V_{DD} quiescent current		V_{LI} = V_{HI} = 0			0.4	0.8	mA
I_{DDO}	V_{DD} operating current	UCC27200	f = 500 kHz, C_{LOAD} = 0			2.5	4	mA
		UCC27201				3.8	5.5	
I_{HB}	Boot voltage quiescent current		V_{LI} = V_{HI} = 0 V			0.4	0.8	mA
I_{HBO}	Boot voltage operating current		f = 500 kHz, C_{LOAD} = 0			2.5	4	mA
I_{HBS}	HB to V_{SS} quiescent current		V_{HS} = V_{HB} = 110 V			0.000 5	1	µA
I_{HBSO}	HB to V_{SS} operating current		f = 500 kHz, C_{LOAD} = 0			0.1		mA
Input								
V_{HIT}	Input rising threshold	UCC27200				5.8	8	V
V_{LIT}	Input falling threshold	UCC27200			3	5.4		V
V_{IHYS}	Input voltage hysteresis	UCC27200				0.4		V
V_{HIT}	Input voltage threshold	UCC27201				1.7	2.5	V
V_{LIT}	Input voltage threshold	UCC27201			0.8	1.6		V
V_{IHYS}	Input voltage hysteresis	UCC27201				100		mV
R_{IN}	Input pulldown resistance				100	200	350	kΩ
Undervoltage Lockout (UVLO) Protection								
	V_{DD} rising threshold				6.2	7.1	7.8	V
	V_{DD} threshold hysteresis					0.5		V
	VHB rising threshold				5.8	6.7	7.2	V
	VHB threshold hysteresis					0.4		V
Bootstrap Diode								
V_F	Low-current forward voltage		I_{VDD} – HB = 100 µA			0.65	0.85	V
V_{FI}	High-current forward voltage		I_{VDD} – HB = 100 mA			0.85	1.1	
R_D	Dynamic resistance, ΔVF/ΔI		I_{VDD} – HB = 100 mA and 80 mA			0.6	1.0	Ω
LO Gate Driver								
V_{LOL}	Low level output voltage		I_{LO} = 100 mA			0.18	0.4	V
V_{LOH}	High level output voltage		I_{LO} = –100 mA, V_{LOH} = V_{DD} – V_{LO}	T_J = –40°C to 125°C		0.25	0.4	V
				T_J = –40°C to 140°C		0.25	0.42	
	Peak pullup current		V_{LO} = 0 V			3		A
	Peak pulldown current		V_{LO} = 12 V			3		A
HO Gate Driver								
V_{HOL}	Low-level output voltage		I_{HO} = 100 mA			0.18	0.4	V
V_{HOH}	High-level output voltage		I_{HO} = –100 mA, V_{HOH} = V_{HB} – V_{HO},	T_J = –40°C to 125°C		0.25	0.4	V
				T_J = –40°C to 140°C		0.25	0.42	
	Peak pullup current		V_{HO} = 0 V			3		A
	Peak pulldown current		V_{HO} = 12 V			3		A

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_A = T_J = –40°C to 140°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delays							
T_{DLFF}	V_{LI} falling to V_{LO} falling	C_{LOAD} = 0	T_J = –40°C to 125°C		20	45	ns
			T_J = –40°C to 140°C		20	50	ns
T_{DHFF}	V_{HI} falling to V_{HO} falling	C_{LOAD} = 0	T_J = –40°C to 125°C		20	45	ns
			T_J = –40°C to 140°C		20	50	ns
T_{DLRR}	V_{LI} rising to V_{LO} rising	C_{LOAD} = 0	T_J = –40°C to 125°C		20	45	ns
			T_J = –40°C to 140°C		20	50	ns
T_{DHRR}	V_{HI} rising to V_{HO} rising	C_{LOAD} = 0	T_J = –40°C to 125°C		20	45	ns
			T_J = –40°C to 140°C		20	50	ns
Delay Matching							
T_{MON}	LI ON, HI OFF				1	7	ns
T_{MOFF}	LI OFF, HI ON				1	7	ns
Output Rise and Fall Time							
t_R	LO, HO	C_{LOAD} = 1000 pF			8		ns
t_F	LO, HO	C_{LOAD} = 1000 pF			7		ns
t_R	LO, HO (3 V to 9 V)	C_{LOAD} = 0.1 µF			0.35	0.6	µs
t_F	LO, HO (3 V to 9 V)	C_{LOAD} = 0.1 µF			0.3	0.6	µs
Miscellaneous							
	Minimum input pulse width that changes the output					50	ns
	Bootstrap diode turn-off time	I_F = 20 mA, I_{REV} = 0.5 A (1) (2)			20		ns

(1) Typical values for T_A = 25°C
(2) I_F: Forward current applied to bootstrap diode. I_{REV}: Reverse current applied to bootstrap diode.

TYPICAL CHARACTERISTICS

UCC27200 OPERATING CURRENT
vs
FREQUENCY

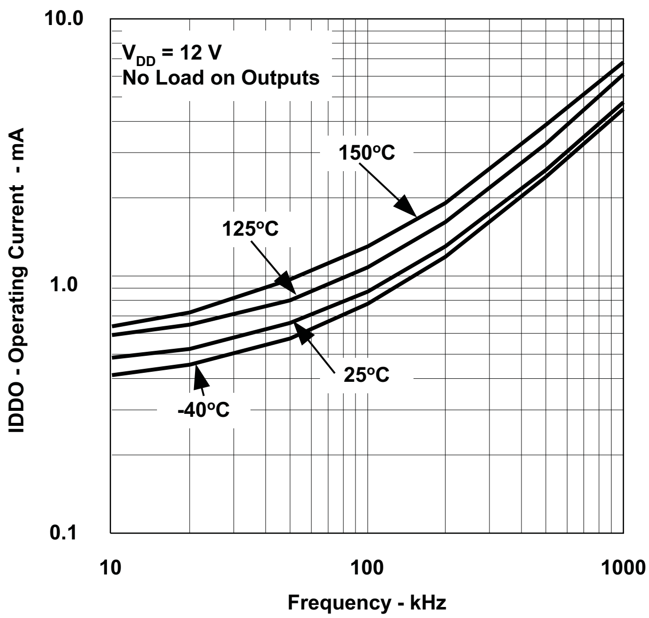


Figure 2.

UCC27201 OPERATING CURRENT
vs
FREQUENCY

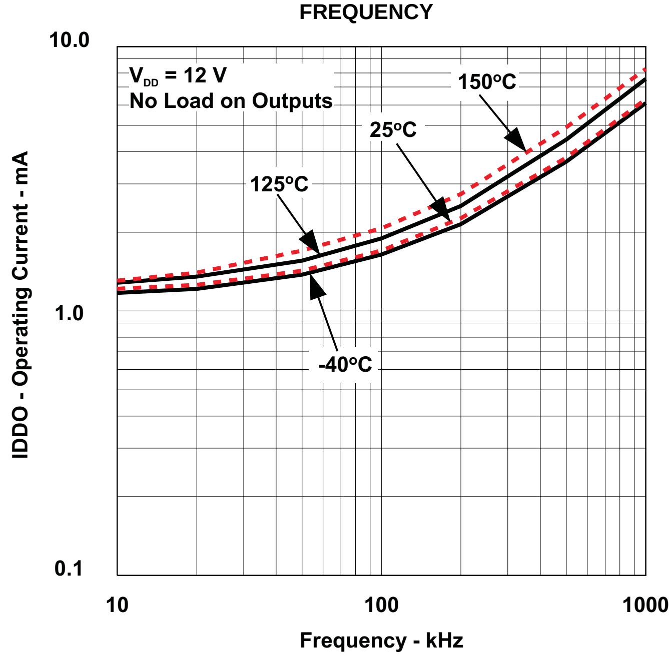


Figure 3.

BOOT VOLTAGE OPERATING CURRENT
vs
FREQUENCY

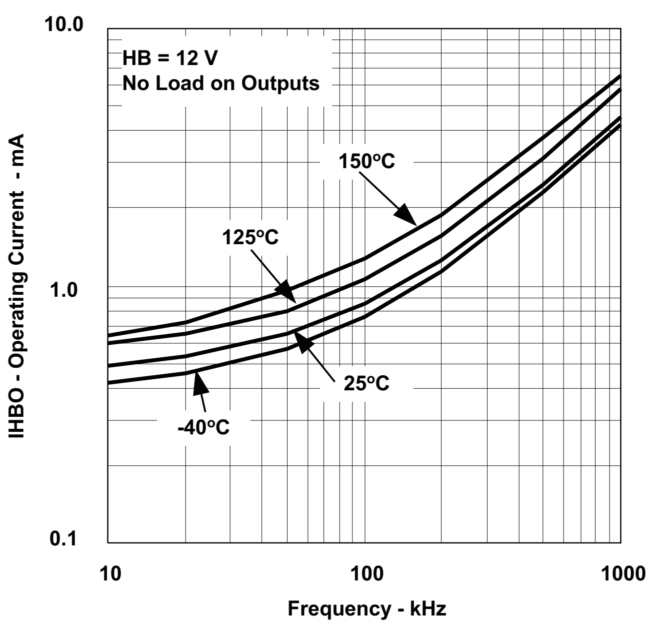


Figure 4.

HB TO V_{SS} OPERATING CURRENT
vs
FREQUENCY

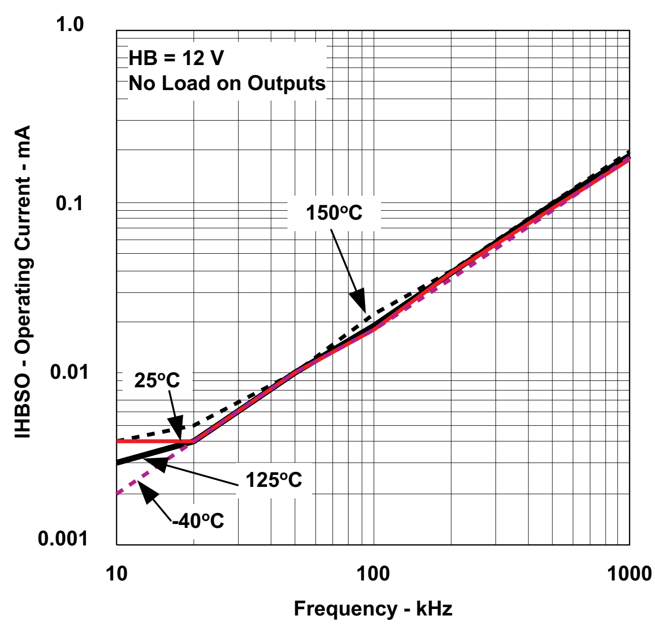


Figure 5.

TYPICAL CHARACTERISTICS (continued)

UCC27200 INPUT THRESHOLD vs SUPPLY VOLTAGE

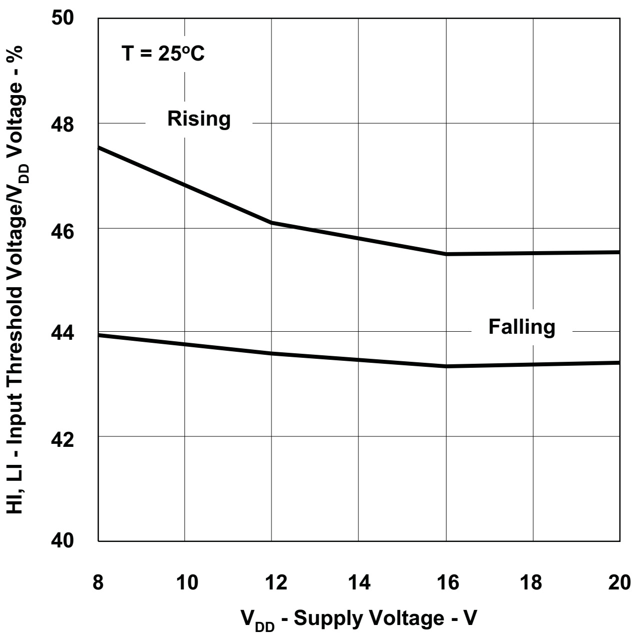


Figure 6.

UCC27201 INPUT THRESHOLD vs SUPPLY VOLTAGE

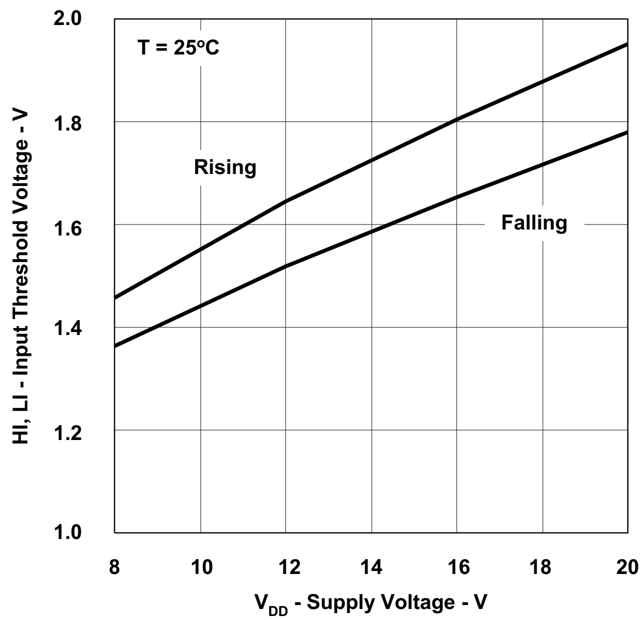


Figure 7.

UCC27200 INPUT THRESHOLD vs TEMPERATURE

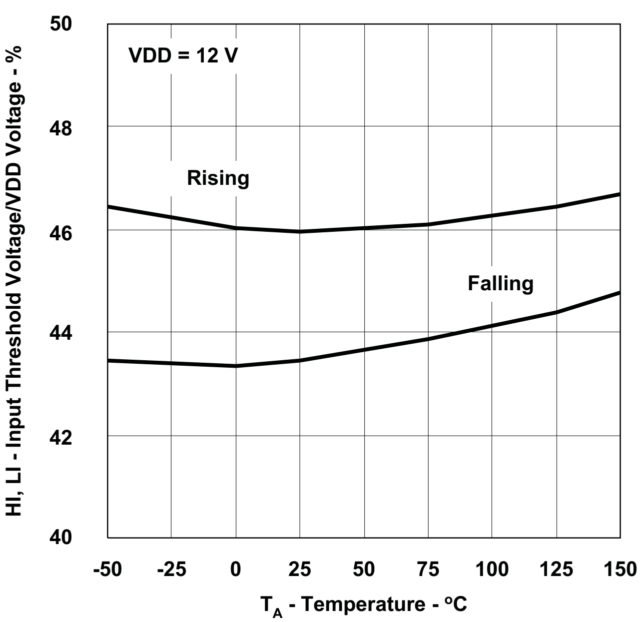


Figure 8.

UCC27201 INPUT THRESHOLD vs TEMPERATURE

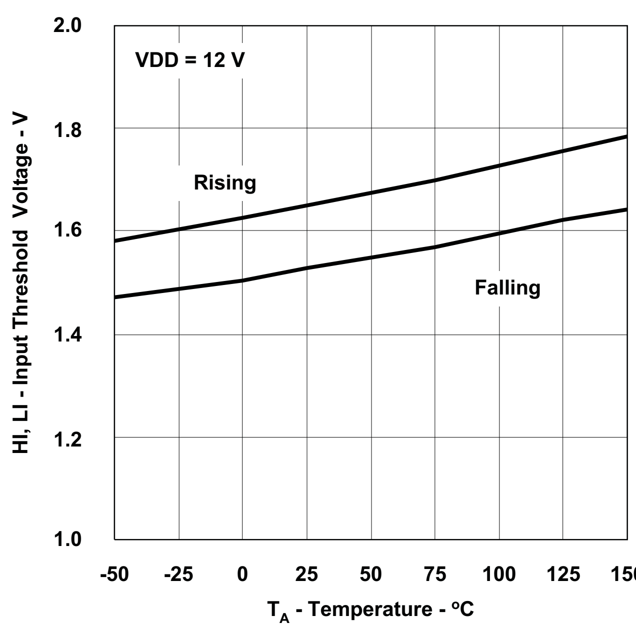


Figure 9.

TYPICAL CHARACTERISTICS (continued)

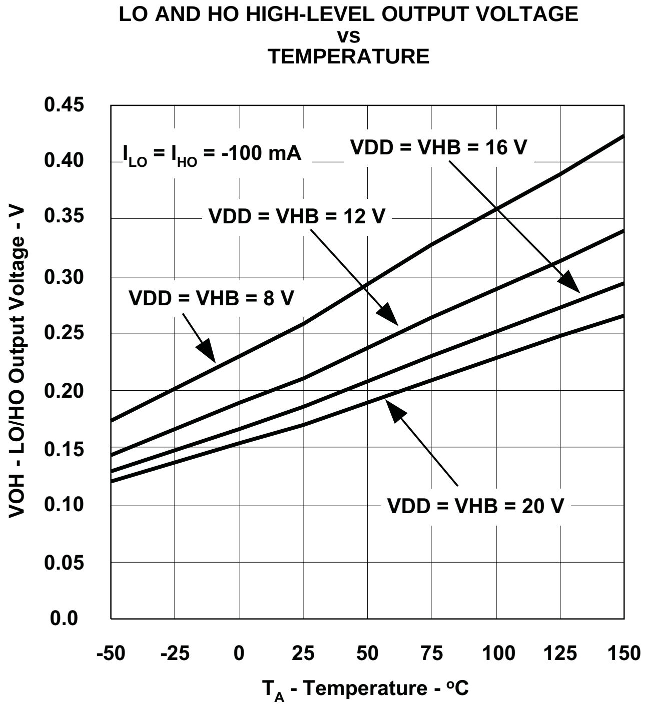


Figure 10.

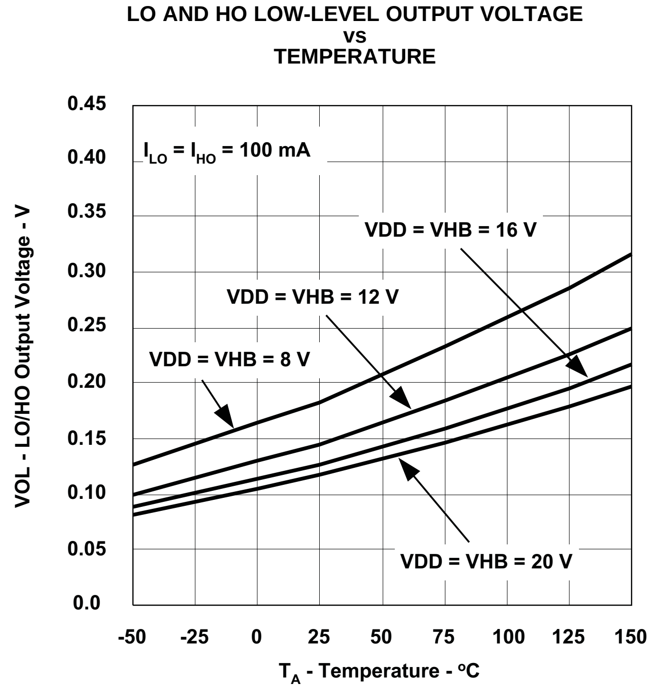


Figure 11.

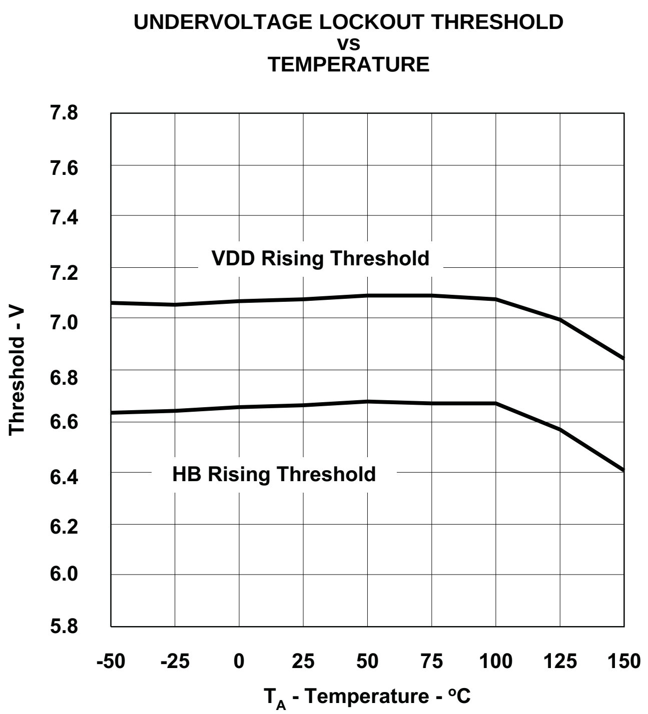


Figure 12.

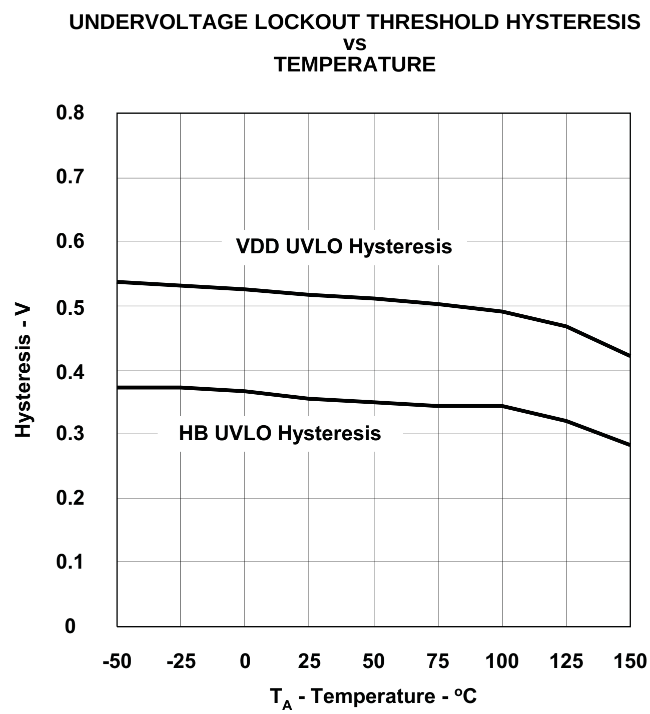


Figure 13.

TYPICAL CHARACTERISTICS (continued)

UCC27200 PROPAGATION DELAYS
vs
TEMPERATURE

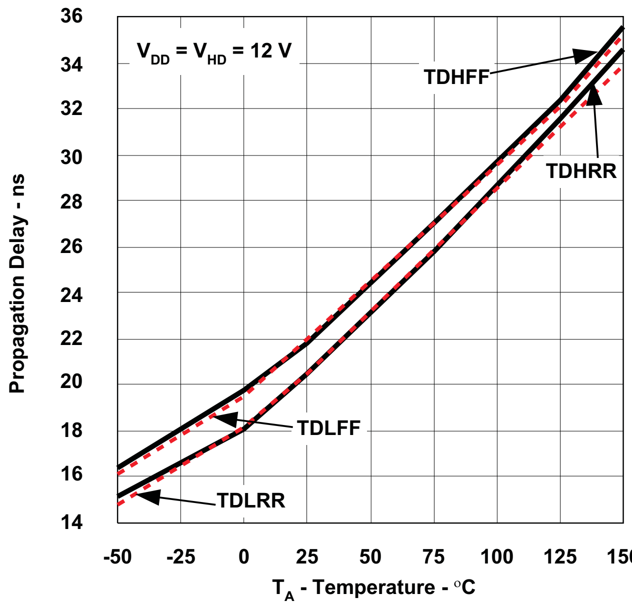


Figure 14.

UCC27201 PROPAGATION DELAYS
vs
TEMPERATURE

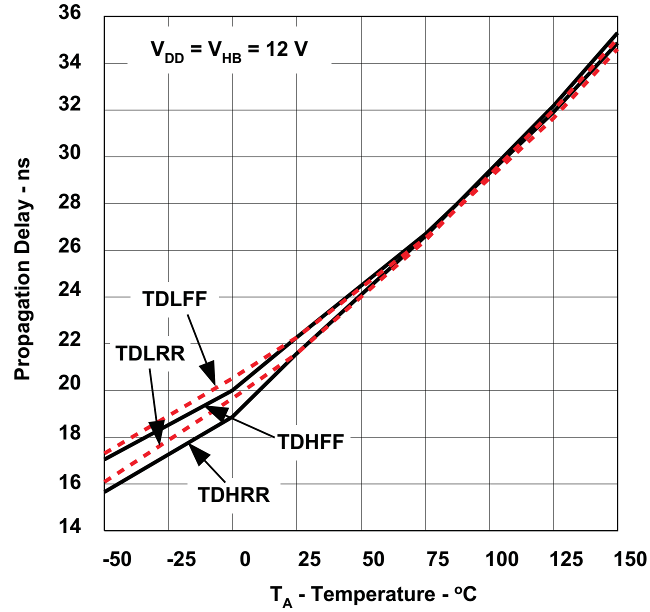


Figure 15.

UCC27200 PROPAGATION DELAY
vs
SUPPLY VOLTAGE

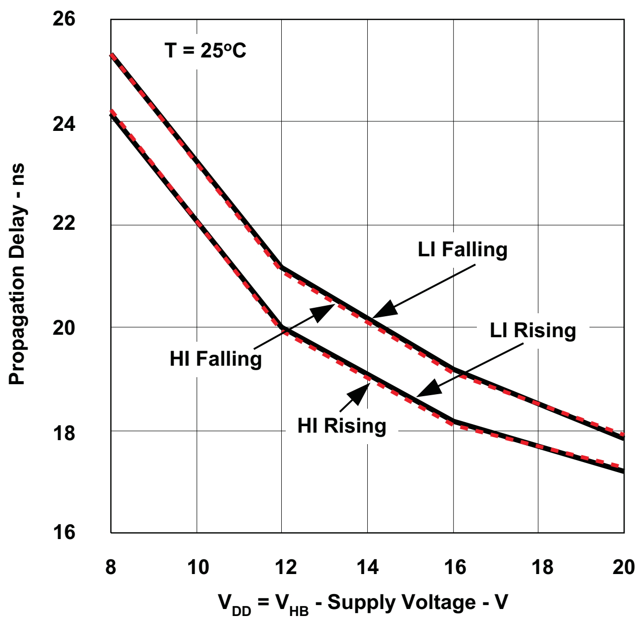


Figure 16.

UCC27201 PROPAGATION DELAY
vs
SUPPLY VOLTAGE

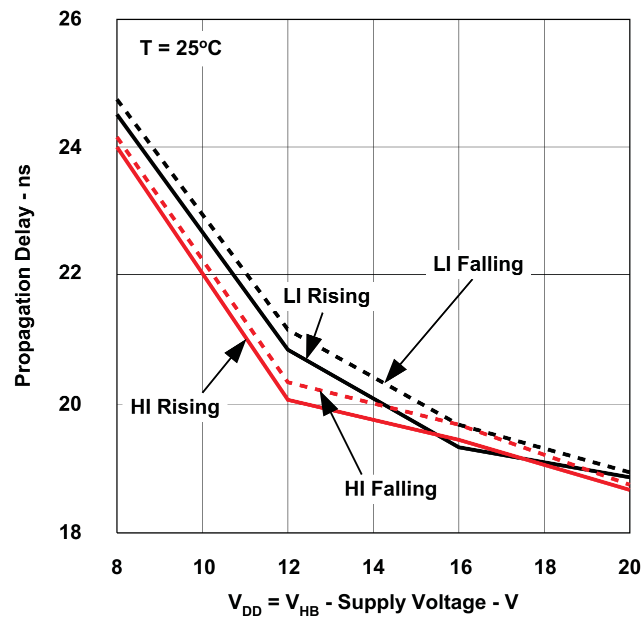


Figure 17.

TYPICAL CHARACTERISTICS (continued)

DELAY MATCHING
vs
TEMPERATURE

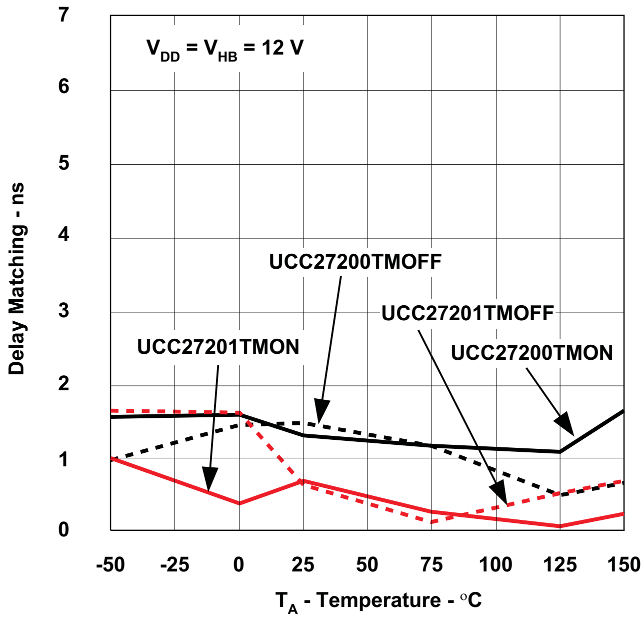


Figure 18.

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

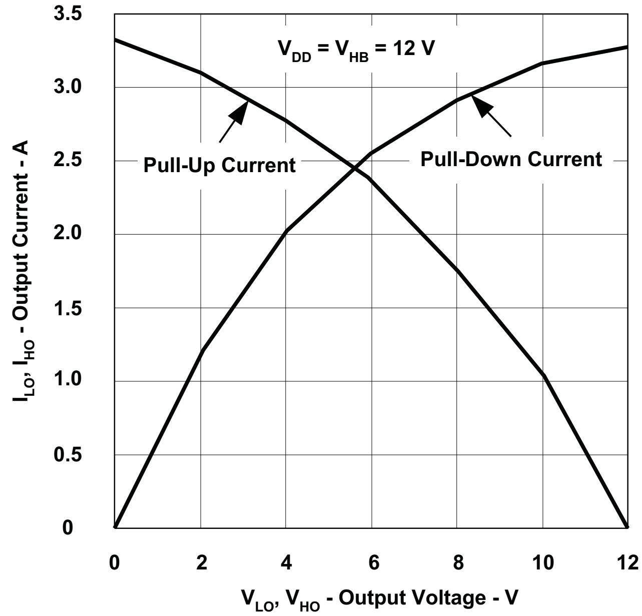


Figure 19.

DIODE CURRENT
vs
DIODE VOLTAGE

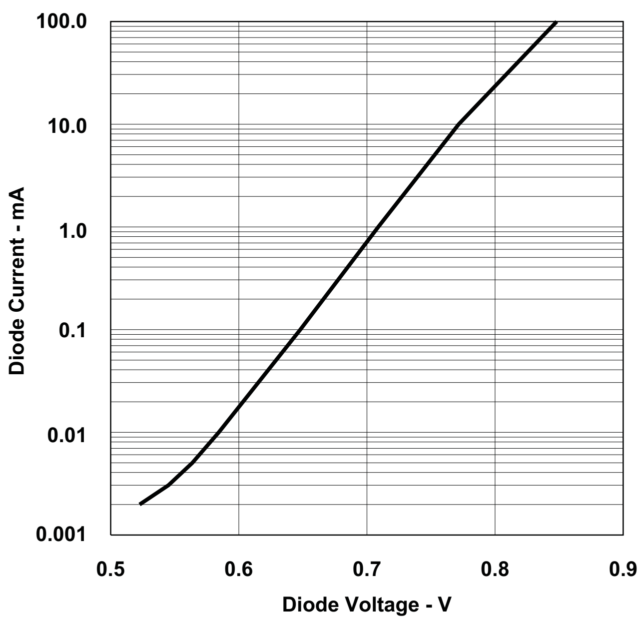


Figure 20.

QUIESCENT CURRENT
vs
SUPPLY VOLTAGE

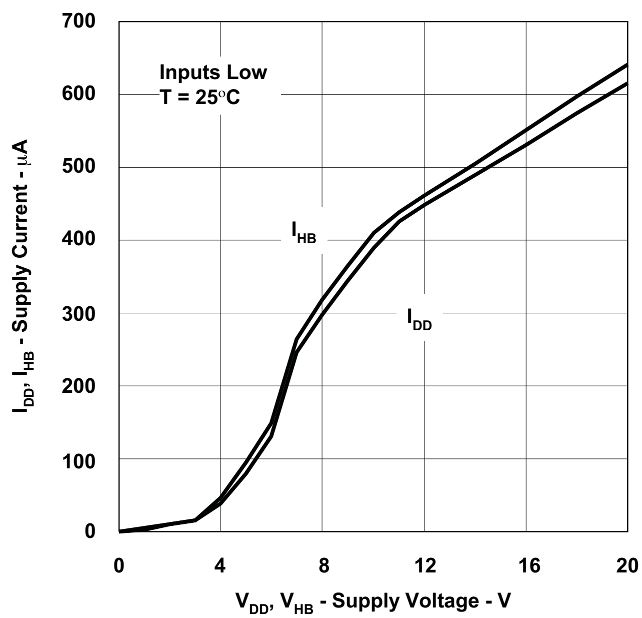
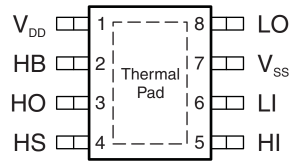


Figure 21.

DEVICE INFORMATION

DDA PACKAGE
(TOP VIEW)

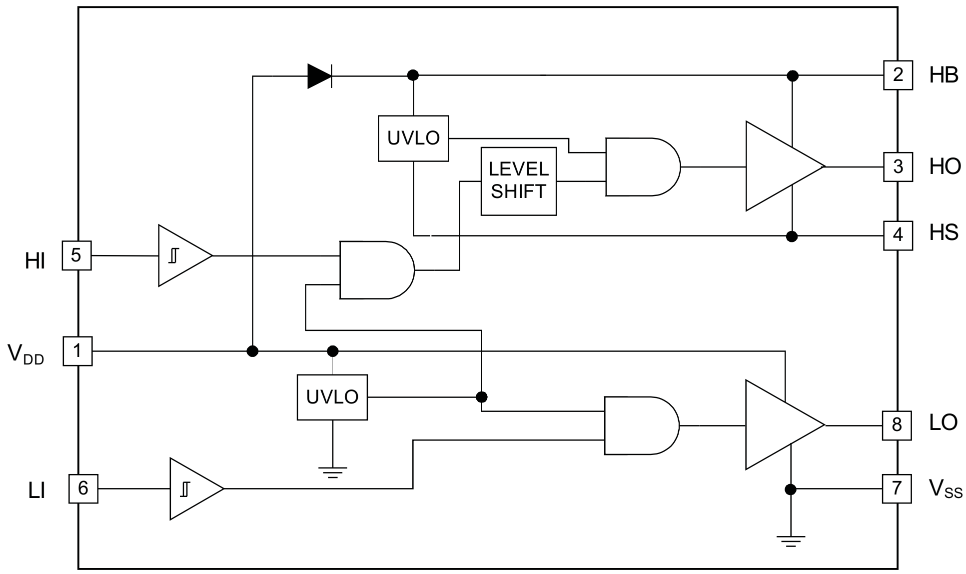


A. The V_{SS} pin and the exposed thermal die pad are internally connected.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	I	Positive supply to the lower gate driver. Decouple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22 µF to 1.0 µF.
HB	2	I	High-side bootstrap supply. The bootstrap diode is on-chip, but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF, however, the value is dependant on the gate charge of the high-side MOSFET.
HO	3	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	I	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	5	I	High-side input
LI	6	I	Low-side input
V_{SS}	7	O	Negative supply terminal for the device which is generally grounded
LO	8	O	Low-side output. Connect to the gate of the low-side power MOSFET.
PowerPAD	PAD		Electrically referenced to V_{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

FUNCTIONAL BLOCK DIAGRAM



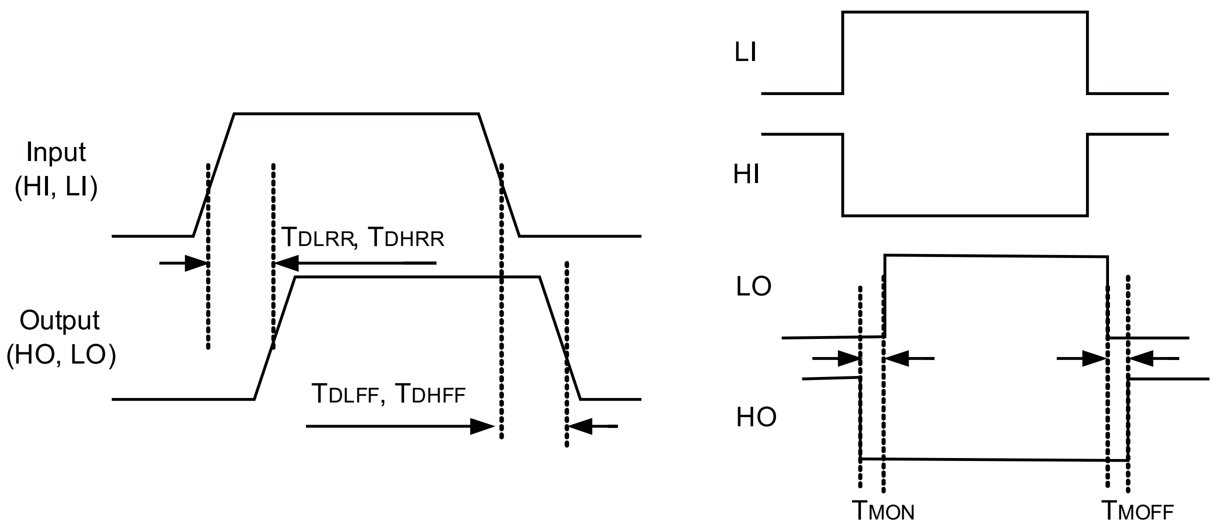


Figure 22. Timing Diagrams

APPLICATION INFORMATION

Functional Description

The UCC27200 and UCC27201 are high-side/low-side drivers. The high side and low side each have independent inputs, which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27200 and UCC27201. The UCC27200 is the CMOS-compatible input version, and the UCC27201 is the TTL- or logic-compatible version. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS}, which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

NOTE:

The term UCC2720x applies to both the UCC27200 and UCC27201.

Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27200 is 200 kΩ nominal and input capacitance is approximately 2 pF. The 200 kΩ is a pulldown resistance to Vss (ground). The CMOS compatible input of the UCC27200 provides a rising threshold of 48% of V_{DD} and falling threshold of 45% of V_{DD}. The inputs of the UCC27200 are intended to be driven from 0 to V_{DD} levels.

The input stages of the UCC27201 incorporate an open drain configuration to provide the lower input thresholds. The input impedance is 200 kΩ nominal and input capacitance is approximately 4 pF. The 200 kΩ is a pulldown resistance to V_{SS} (ground). The logic level compatible input provides a rising threshold of 1.7 V and a falling threshold of 1.6 V.

Undervoltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. V_{DD} as well as V_{HB} to V_{HS} differential voltages are monitored. The V_{DD} UVLO disables both drivers when V_{DD} is below the specified threshold. The rising V_{DD} threshold is 7.1 V with 0.5-V hysteresis. The V_{HB} UVLO disables only the high-side driver when the V_{HB} to V_{HS} differential voltage is below the specified threshold. The V_{HB} UVLO rising threshold is 6.7 V with 0.4-V hysteresis.

Level Shift

The level-shift circuit is the interface from the high-side input to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC2720x family of drivers. The diode anode is connected to V_{DD} and cathode connected to VHB. With the VHB capacitor connected to HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and a voltage rating margin that allow for efficient and reliable operation.

Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from V_{DD} to V_{SS} and the high-side is referenced from V_{HB} to V_{HS}.

Design Tips

Switching the MOSFETs

Achieving optimum drive performance at high frequency efficiently requires special attention to layout and minimizing parasitic inductances. Care must be taken at the driver die and package level as well as the PCB layout to reduce parasitic inductances as much as possible. Figure 23 shows the main parasitic inductance elements and current flow paths during the turn on and turn off of the MOSFET by charging and discharging its CGS capacitance.

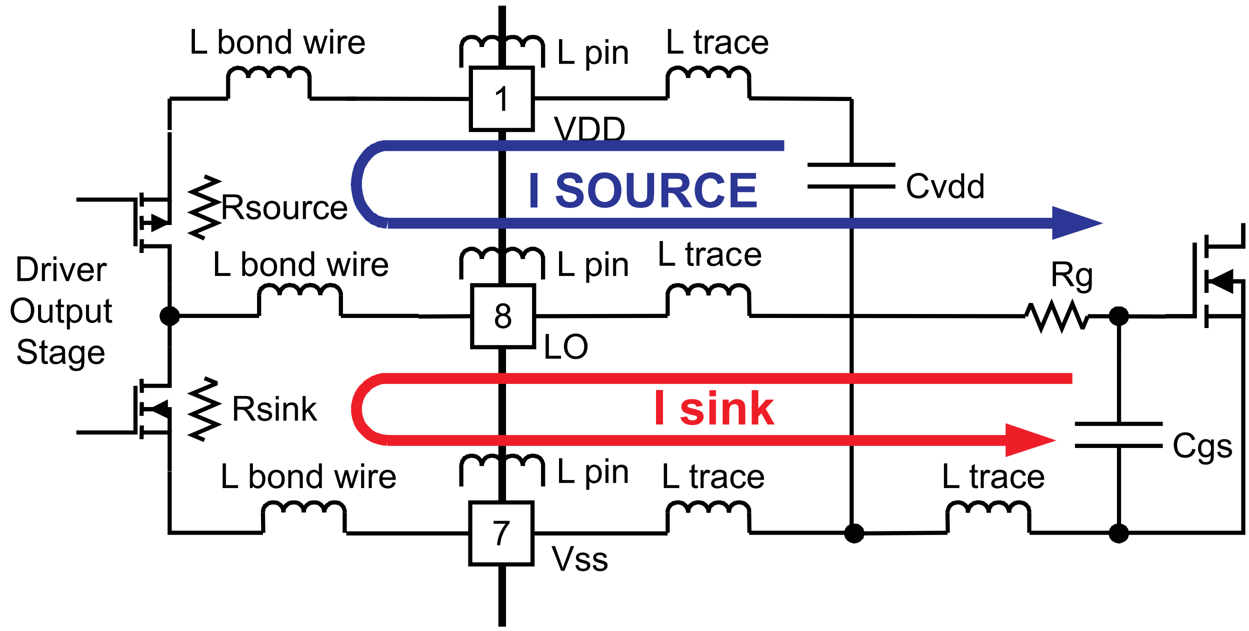


Figure 23. MOSFET Drive Paths and Circuit Parasitics

The I_{SOURCE} current charges the C_{GS} gate capacitor and the I_{SINK} current discharges it. The rise and fall time of the voltage across the gate to source defines how quickly the MOSFET can be switched. Based on actual measurements, the analytical curves in Figure 24 and Figure 25 indicate the output voltage and current of the drivers during the discharge of the load capacitor. Figure 24 shows voltage and current as a function of time. Figure 25 indicates the relationship of voltage and current during fast switching. These figures demonstrate the actual switching process and limitations due to parasitic inductances.

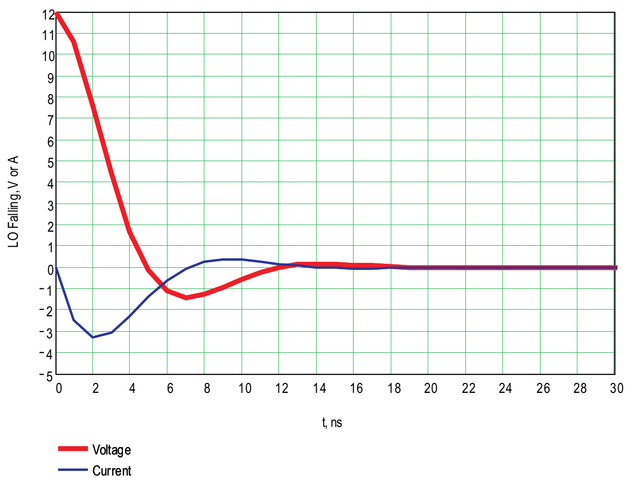


Figure 24. Turn-Off Voltage and Current vs Time

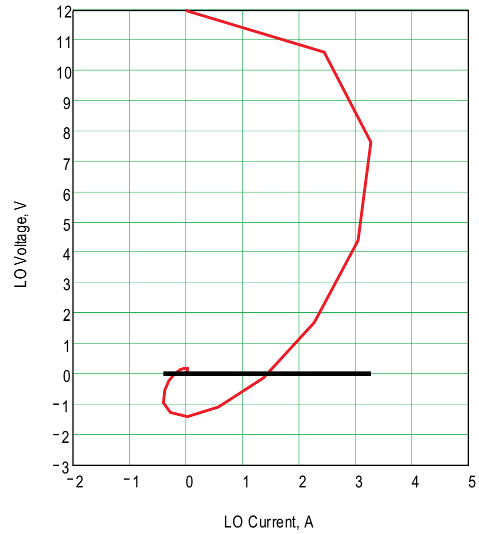


Figure 25. Turn-Off Voltage and Current Switching

Turning off the MOSFET must be achieved as fast as possible to minimize switching losses. For this reason, the UCC2720x drivers are designed for high peak currents and low output resistance. The sink capability is specified as 0.18 V at 100-mA dc current, implying 1.8-Ω $R_{DS(on)}$. With 12-V drive voltage, no parasitic inductance, and a linear resistance, one would expect initial sink current amplitude of 6.7 A for both high-side and low-side drivers. Assuming a pure R-C discharge circuit of the gate capacitor, one would expect the voltage and current waveforms to be exponential. Due to the parasitic inductances and nonlinear resistance of the driver MOSFETs, the actual waveforms have some ringing, and the peak sink current of the drivers is approximately 3.3 A, as shown in Figure 19. The overall parasitic inductance of the drive circuit is estimated at 4 nH.

Actual measured waveforms are shown in Figure 26 and Figure 27. As shown, the typical rise time of 8 ns and fall time of 7 ns is conservatively rated.

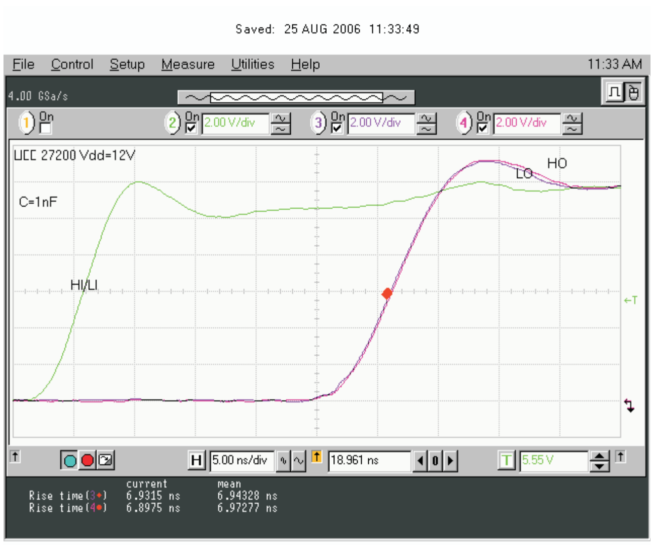


Figure 26. V_{LO} and V_{HO} Rise Time, 1-nF Load, 5 ns/Div

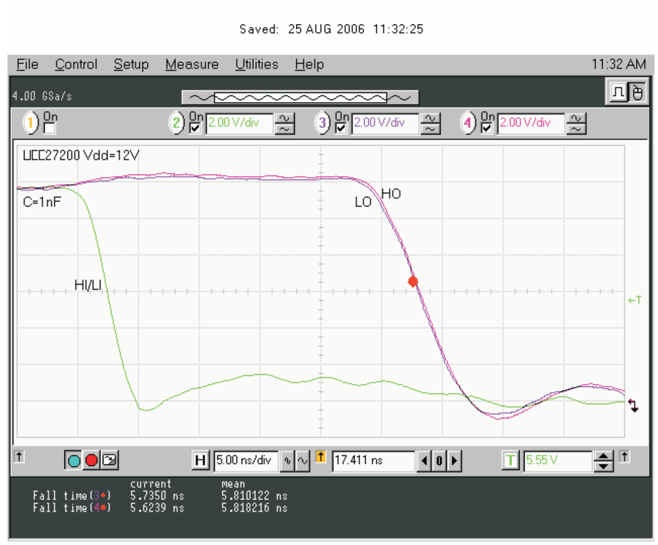


Figure 27. V_{LO} and V_{HO} Fall Time, 1-nF Load, 5-ns/Div

Dynamic Switching of the MOSFETs

The true behavior of MOSFETS presents a dynamic capacitive load primarily at the gate to source threshold voltage. Using the turn-off case as the example, when the gate to source threshold voltage is reached, the drain voltage starts rising, and the drain-to-gate parasitic capacitance couples charge into the gate, resulting in the turn-off plateau. The relatively low threshold voltages of many MOSFETS and the increased charge that must be removed (Miller charge) makes good driver performance necessary for efficient switching. An open-loop half-bridge power converter was utilized to evaluate performance in actual applications. The schematic of the half-bridge converter is shown in Figure 30. The turn-off waveforms of the UCC27200 driving two MOSFETs in parallel are shown in Figure 28 and Figure 29.

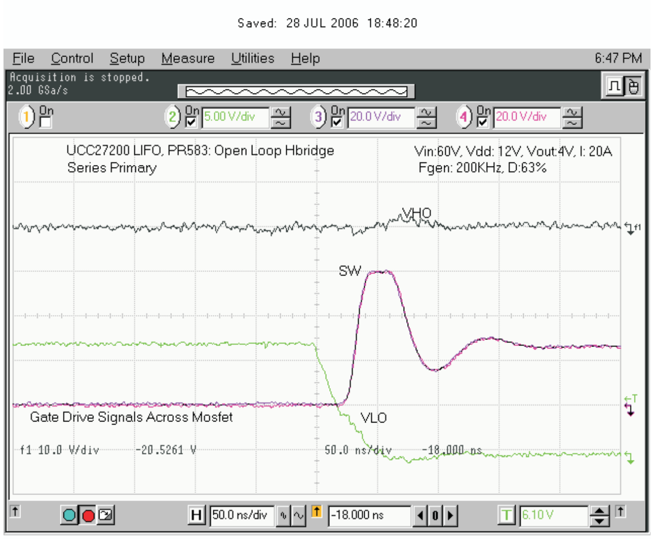


Figure 28. V_{LO} Fall Time in Half-Bridge Converter

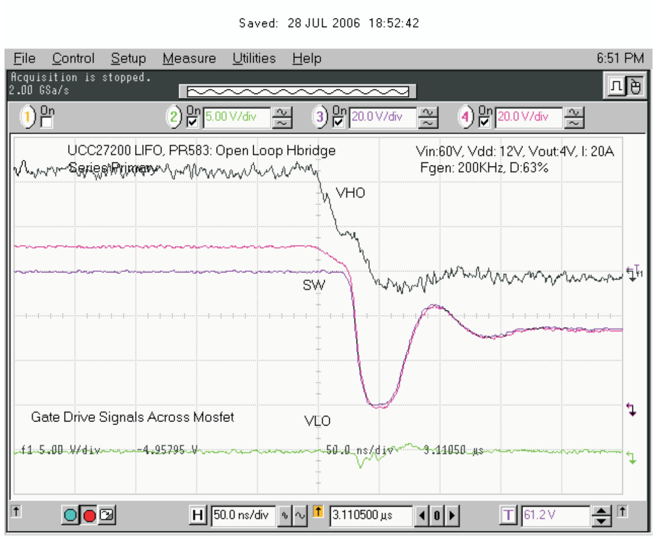


Figure 29. V_{HO} Fall Time in Half-Bridge Converter

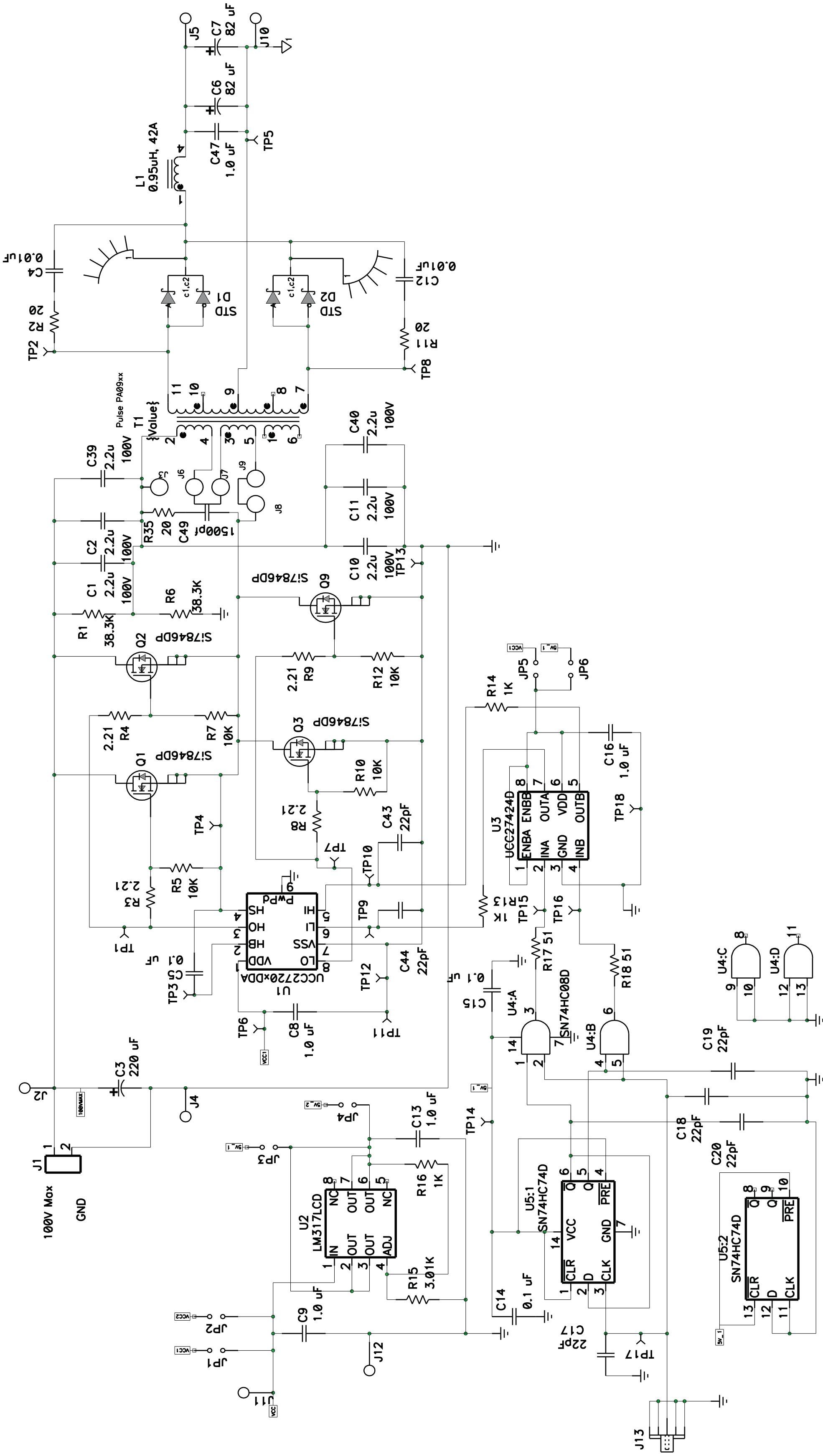

J5
C7 82 uF
J10
C6 82 uF
C47 1.0 uF
TP5
L1 0.95uH, 42A
C4 0.01uF
R2 20
TP2
D1 STD
D2 STD
C12 0.01uF
R11 20
TP8
T1 {Value}
Pulse PA09xx
C39 2.2u 100V
C40 2.2u 100V
C11 2.2u 100V
C10 2.2u 100V
TP13
R35 20
C49 1500pF
C2 2.2u 100V
C1 2.2u 100V
R6 38.3K
R1 38.3K
Q9 Si7846DP
Q2 Si7846DP
Q3 Si7846DP
Q1 Si7846DP
R9 2.21
R12 10K
R4 2.21
R7 10K
R10 10K
R8 2.21
C43 22pF
TP7
TP10
TP4
R5 10K
R3 2.21
TP1
U1 UCC2720xDDA
C5 0.1 uF
TP3
TP9
C44 22pF
TP12
TP6
C8 1.0 uF
TP11
R14 1K
JP5
JP6
C16 1.0 uF
U3 UCC27424D
TP18
R13 1K
TP15
TP16
R17 51
R18 51
C15 0.1 uF
U4:A
U4:B
U4:C
U4:D
SN74HC08D
C19 22pF
C3 220 uF
J2
J4
J1
100V Max
GND
JP4
C13 1.0 uF
JP3
R16 1K
U2 LM317LCD
R15 3.01K
TP14
C18 22pF
C20 22pF
U5:1 SN74HC74D
U5:2 SN74HC74D
C14 0.1 uF
C17 22pF
TP17
JP2
JP1
C9 1.0 uF
J12
J11
J13

Figure 30. Open-Loop Half-Bridge Converter

Delay Matching and Narrow Pulse Widths

The total delays encountered in the PWM, driver, and power stage must be considered for a number of reasons, primarily for the delay in current limit response. Also to be considered are differences in delays between the drivers which can lead to various concerns depending on the topology. The sync-buck topology switching requires careful selection of dead time between the high- and low-side switches to avoid cross conduction and excessive body diode conduction. Bridge topologies can be affected by a resulting volt-sec imbalance on the transformer, if there is imbalance in the high- and low-side pulse widths in a steady-state condition.

Narrow pulse width performance is an important consideration when transient and short circuit conditions are encountered. Although there may be relatively long steady state PWM output-driver-MOSFET signals, very narrow pulses may be encountered in soft start, large load transients, and short-circuit conditions.

The UCC2720x driver family offers excellent performance in high- and low-side driver delay matching and narrow pulse width performance. The delay matching waveforms are shown in Figure 31 and Figure 32. The UCC2720x driver narrow pulse performance is shown in Figure 33 and Figure 34.

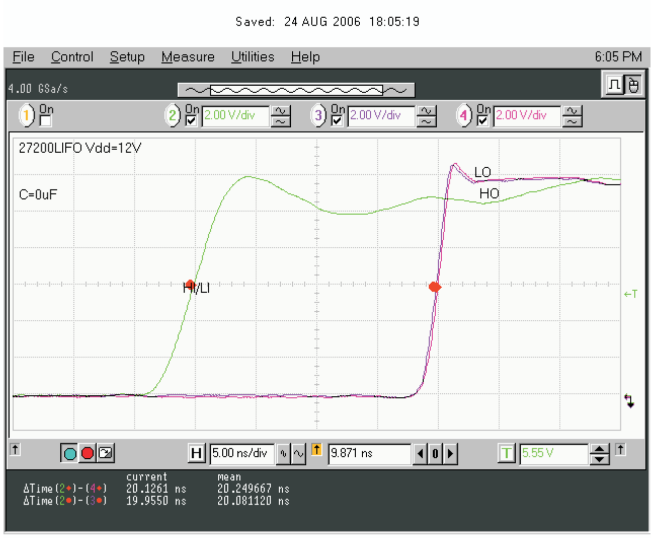


Figure 31. V_{LO} and V_{HO} Rising Edge Delay Matching

Figure 32. V_{LO} and V_{HO} Falling Edge Delay Matching

Figure 33. 20-ns Input Pulse Delay Matching

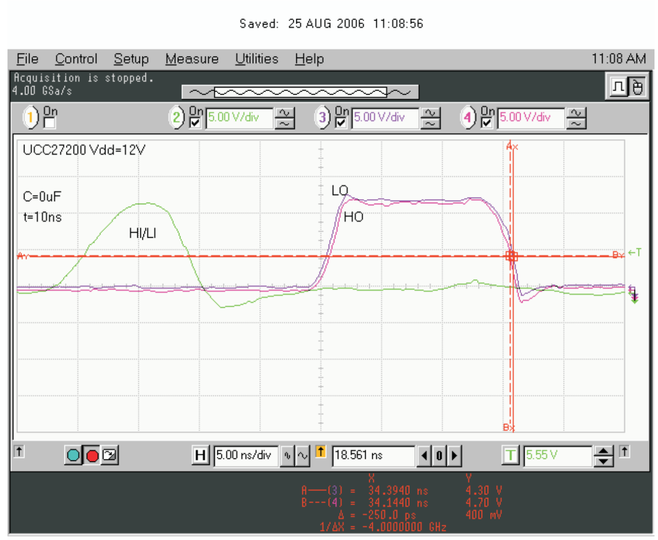


Figure 34. 10-ns Input Pulse Delay Matching

Boot-Diode Performance

The UCC2720x family of drivers internally incorporates the bootstrap diode necessary to generate the high-side bias. The characteristics of this diode are important to achieve efficient reliable operation. The dc characteristics to consider are V_F and dynamic resistance. A low V_F and high dynamic resistance results in a high forward voltage during charging of the bootstrap capacitor. The UCC2720x has a boot diode rated at 0.65-V V_F and dynamic resistance of 0.6 Ω for reliable charge transfer to the bootstrap capacitor. The dynamic characteristics to consider are diode recovery time and stored charge. Diode recovery times that are specified with no conditions can be misleading. Diode recovery times at no forward current (I_F) can be noticeably less than with forward current applied. The UCC2720x boot diode recovery is specified at 20 ns at I_F = 20 mA, I_{REV} = 0.5 A. At 0-mA I_F, the reverse recovery time is 15 ns.

Another less obvious consideration is how the stored charge of the diode is affected by applied voltage. On every switching transition when the HS node transitions from low to high, charge is removed from the boot capacitor to charge the capacitance of the reverse-biased diode. This is a portion of the driver power losses and it reduces the voltage on the HB capacitor. At higher applied voltages, the stored charge of the UCC2720x PN diode is often less than a comparable Schottky diode.

Layout Recommendations

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and V_{HB} (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA package as GND by connecting it to the V_{SS} pin (GND). Note: The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.
- Use similar rules for the HS node as for GND for the high side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. Where possible, widths of 60 mil to 100 mil are preferred.
- Use two or more vias if the driver outputs or SW node need to be routed from one layer to another. For GND, the number of vias should be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid L_I and H_I (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high-impedance leads.
- Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

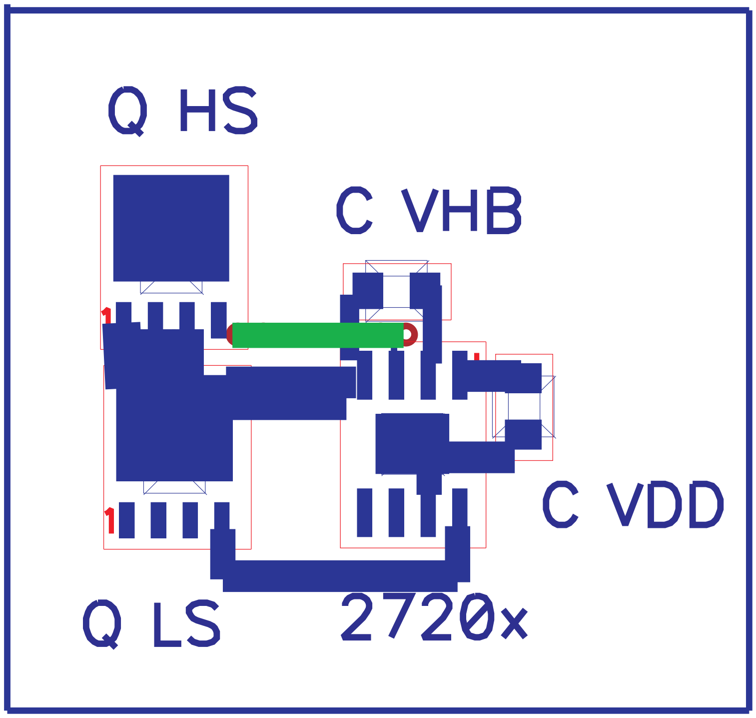


Figure 35. Example Component Placement

Additional References

These references and links to additional information may be found at www.ti.com.

1. Additional layout guidelines for PCB land patterns may be found in application brief SLUA271.
2. Additional thermal performance guidelines may be found in application reports SLMA002 and SLMA004.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC27200QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
UCC27201QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

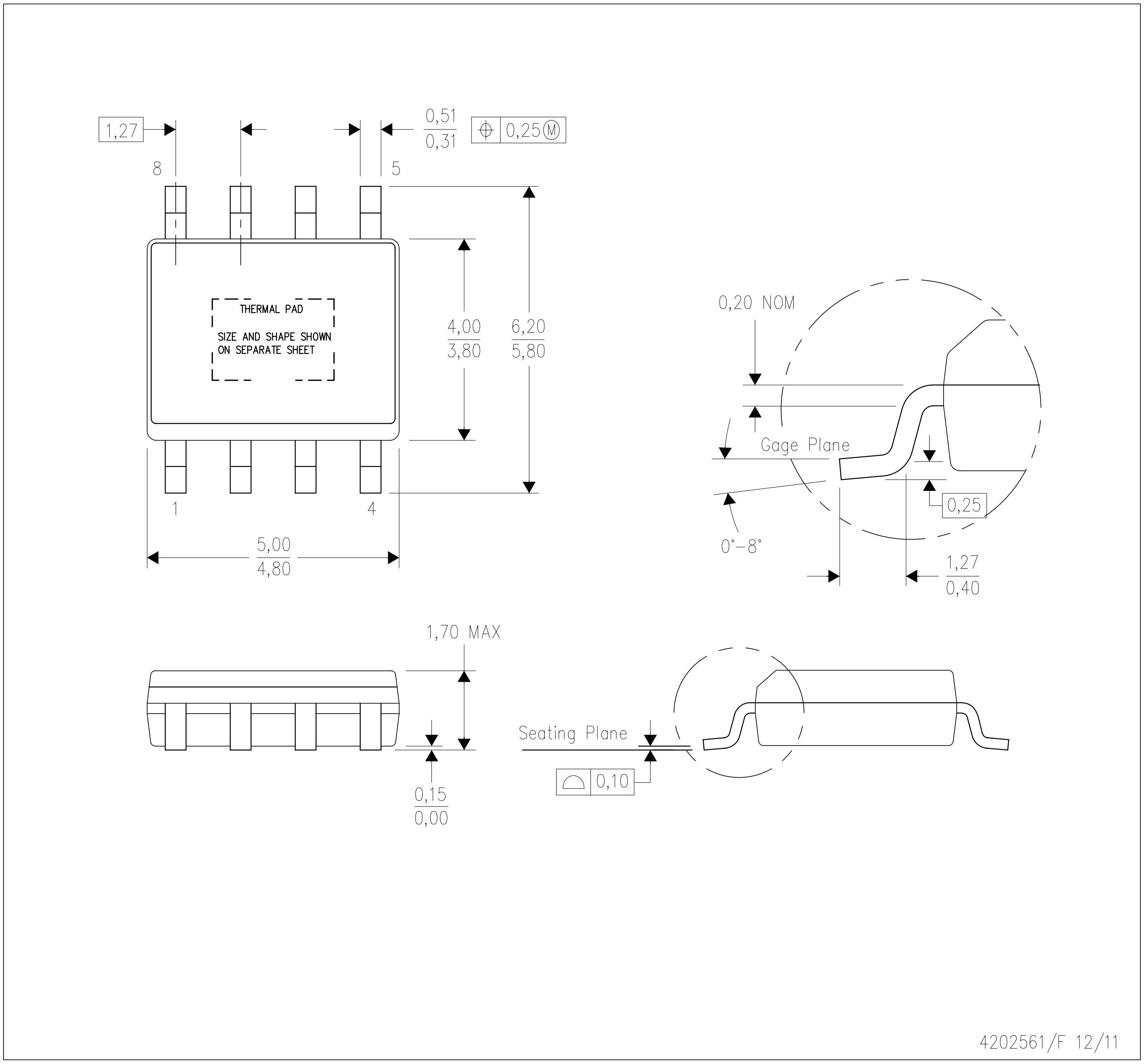
OTHER QUALIFIED VERSIONS OF UCC27200-Q1, UCC27201-Q1 :

- Catalog: UCC27200, UCC27201

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

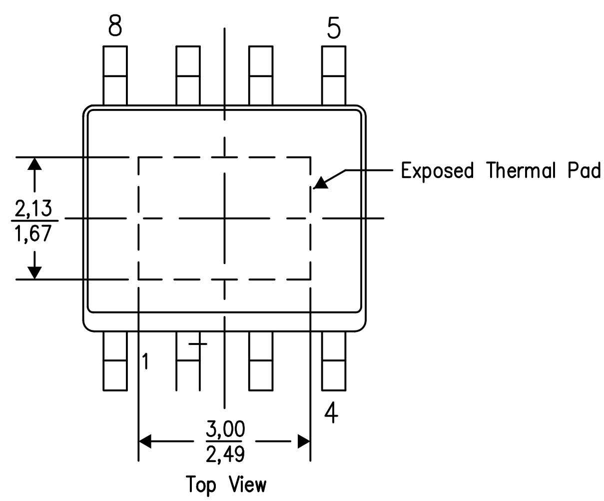
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



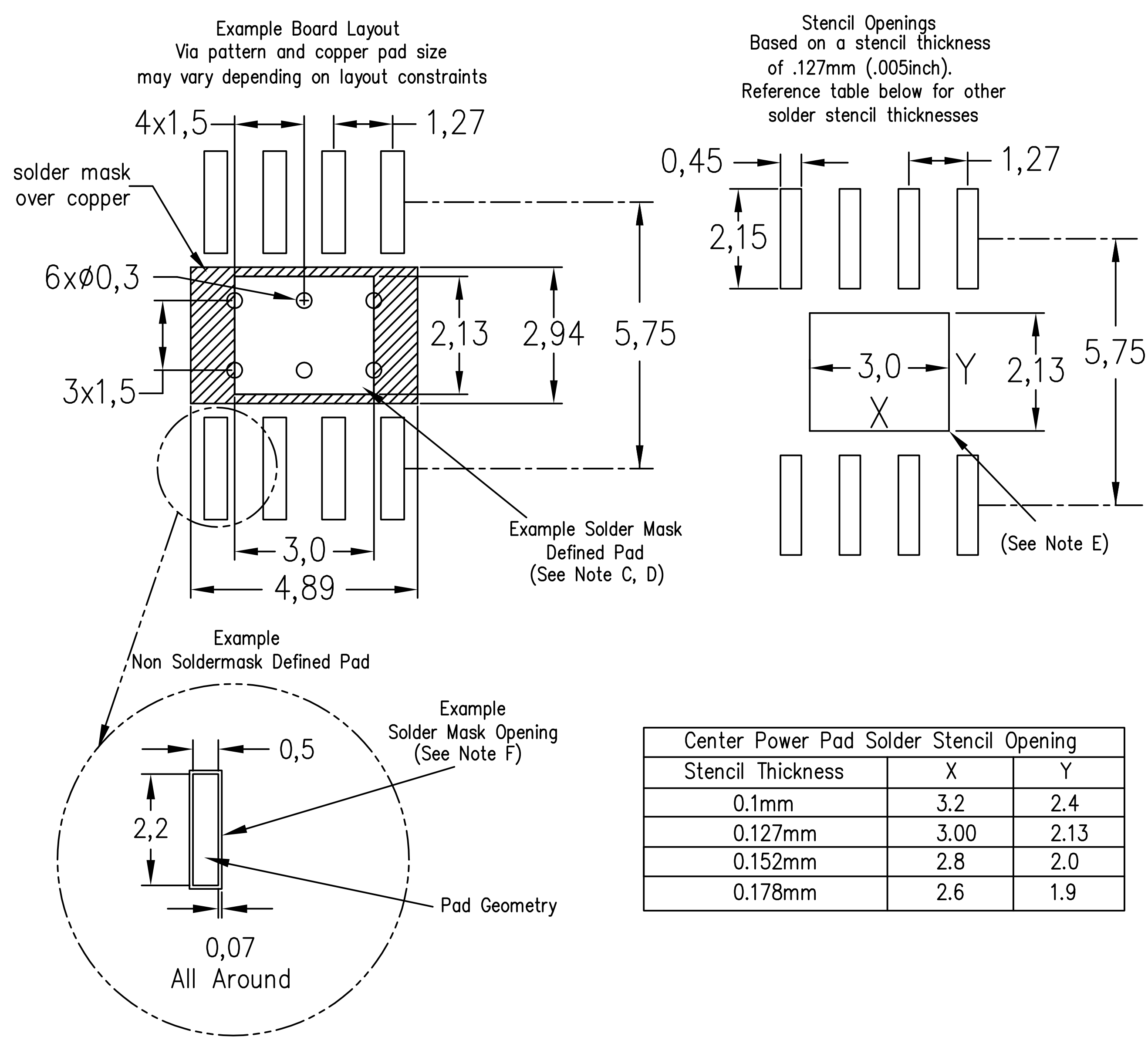
Exposed Thermal Pad Dimensions

4206322–5/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.2	2.4
0.127mm	3.00	2.13
0.152mm	2.8	2.0
0.178mm	2.6	1.9

4208951–5/D 04/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.