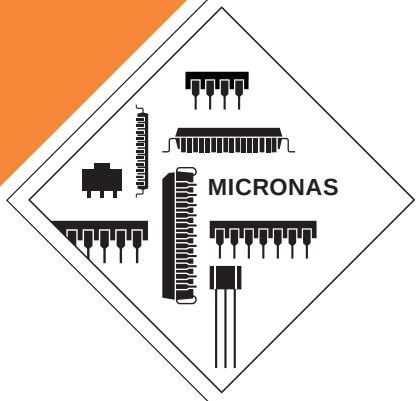


DATA SHEET

UAC 355xB
Universal Serial Bus (USB) Codecs

Edition April 15, 2003
6251-544-1DS

MICRONAS

Contents

Contents, continued

Universal Serial Bus (USB) Codecs

1. Introduction

UAC 355xB is Micronas' new USB audio IC family. It contains a high-performance stereo audio ADC/DAC, digital serial interfaces, and an additional DAC channel for the subwoofer signal.

The audio ADC with direct microphone and line input makes the UAC 355xB the ideal solution for all kinds of USB codec applications. This includes the replacement of analog sound cards in PCs. Integrated headphone amplifiers allow direct headphone connection. Therefore, the IC can be employed as a single-chip headset solution without an extra power supply (bus-powered).

Apart from the standard audio processing, such as volume, bass, and treble, the UAC 355xB offers a programmable 5-band parametric equalizer for correcting the frequency response of the applied speaker. Adjustable dynamic low-frequency processing for the subwoofer channel leads to a reduced number of external analog components. Internal sampling rate converters offer high flexibility in handling all sampling rates for USB upstream and downstream independently.

The codec function of the UAC 355xB is extended by additional interfaces like I^2S, allowing all kinds of digital audio processing systems to be connected to the USB (e.g., Dolby Digital or MP3 decoding chips, such as DPL 4519G, MAS 3528E, or MAS 35x9F).

General-purpose inputs and outputs connect the UAC 355xB to peripheral hardware, such as buttons, keyboards, LEDs, etc. Via I^2C, more complex peripherals, such as LCD displays can be controlled; and the UAC 355xB itself can be remote-controlled via I^2C in non-USB environments.

All in all, the IC is designed as the ideal connecting matrix between USB, analog and digital audio input and output, home stereo, compressed audio, and all kinds of human interface devices. Many functions are adjustable to the customer's needs. Moreover, complete firmware-plug-in download functionality of the on-chip microcontroller turns the UAC 355xB into a customer-specific IC. Micronas supplies standard ROM firmware based on the USB Composite Class, Audio Class, and HID Class, one for general codec applications and one firmware for headset applications.

Apart from the basic versions UAC3554/3555B with Micronas' standard firmware, there is an emulator version UAC 3556B, which contains an 8 KB program RAM in addition to the program ROM. This version can be used for firmware development, prototyping or small quantity production.

Table 1–1: Members of the UAC 355xB Family

Version	Description
UAC 3554B	USB headset
UAC 3555B	USB codec
UAC 3556B	USB codec – emulator version with internal program RAM

1.1. Features

- single-chip, USB specification 2.0 compliant, stereo audio A/D and D/A converter
- supports 8/16-bit mono/stereo recording and up to 24-bit playback
- supports streaming of compressed audio (Dolby Digital, MP3) to external decoder
- Vendor Identification and Device Configuration with external EEPROM
- bus-powered and self-powered mode possible
- remote wake-up
- 12 general-purpose I/O pins with HID support
- I^2S input/output interface
- independent adaptive sample rates of 6.4 to 48 kHz for USB recording and playback (enhanced full duplex)
- audio baseband control: bass, treble, loudness, volume, balance, and mute
- dynamic bass management (Micronas Dynamic Bass (MDB)
- digital speaker equalizer (5-band parametric equalizer)
- adjustable digital active crossover filter for subwoofer
- THD better than –90 dB and SNR of typically 96 dB for D/A converters
- THD better than –90 dB and SNR of typically 92 dB for A/D converters
- power supply rejection ratio >95 dB for analog outputs
- integrated low-power stereo headphone amplifier
- subwoofer output
- I^2C interface (master/slave)
- customized firmware extensions with plug-ins possible

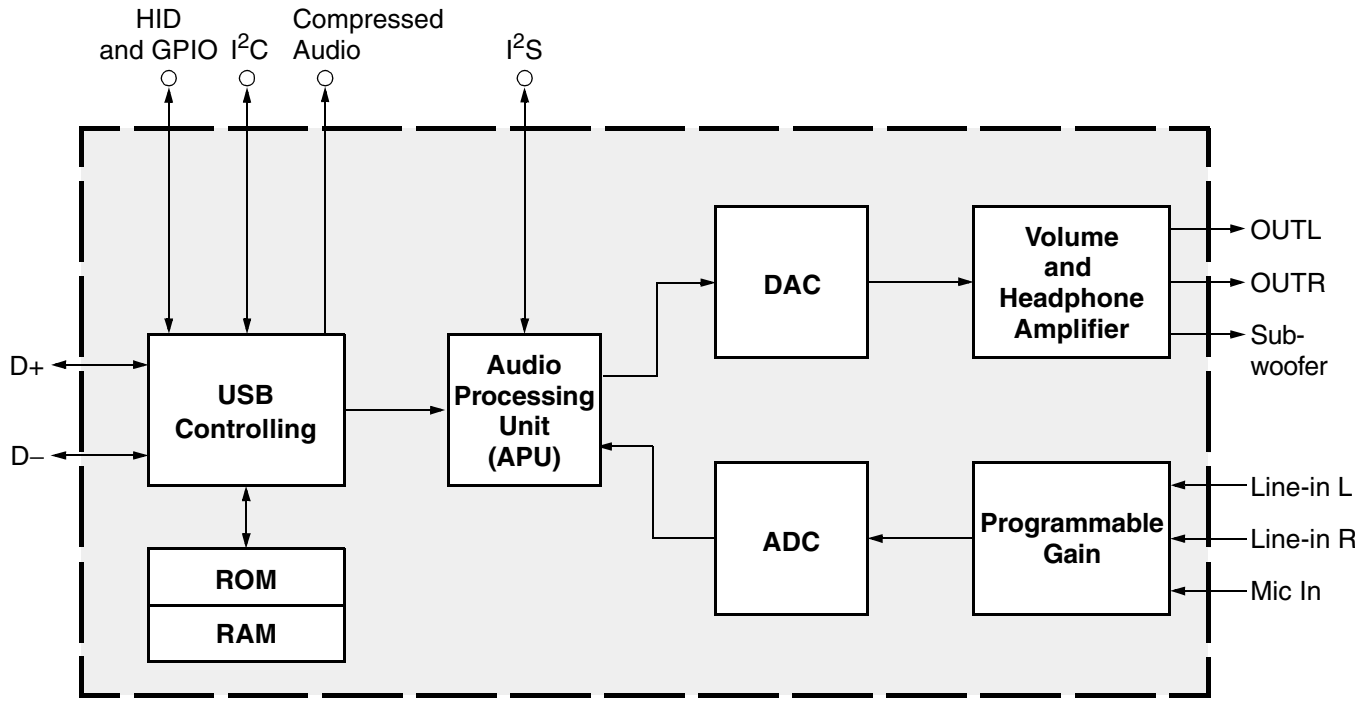


Fig. 1–1: Block diagram of the UAC 355xB

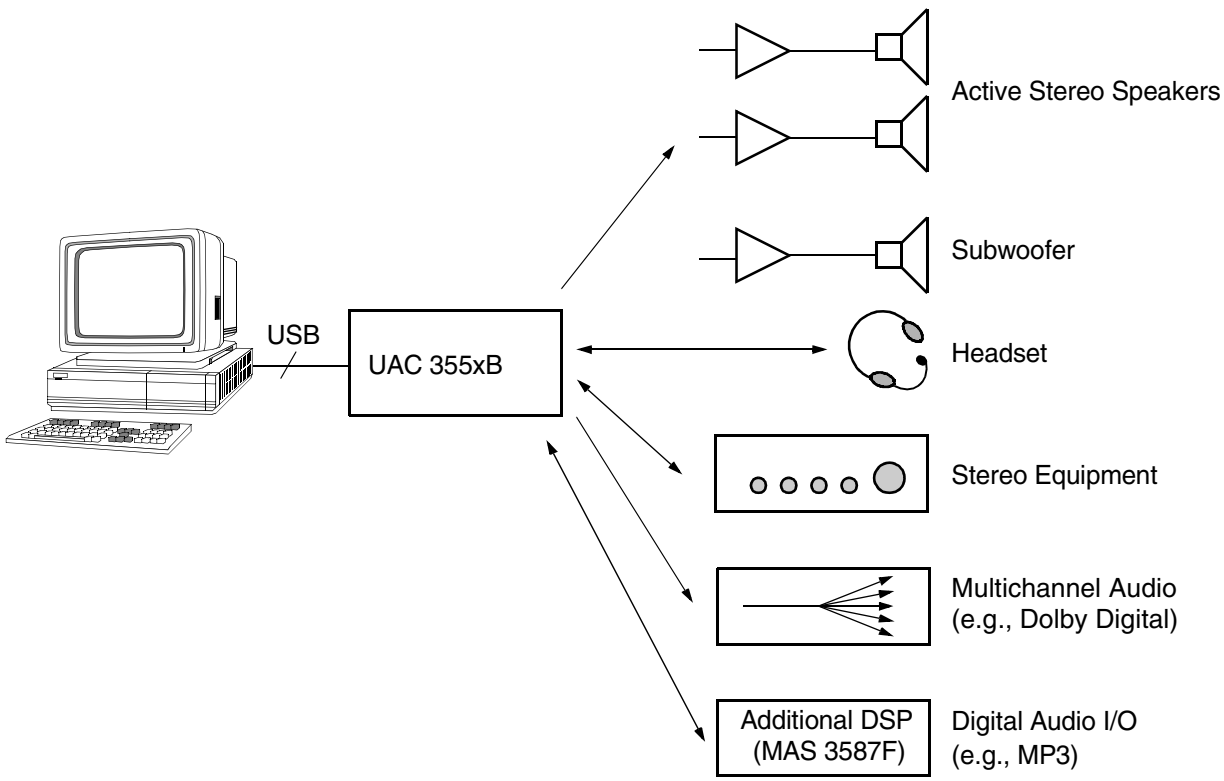


Fig. 1–2: System application diagram

2. Hardware Description

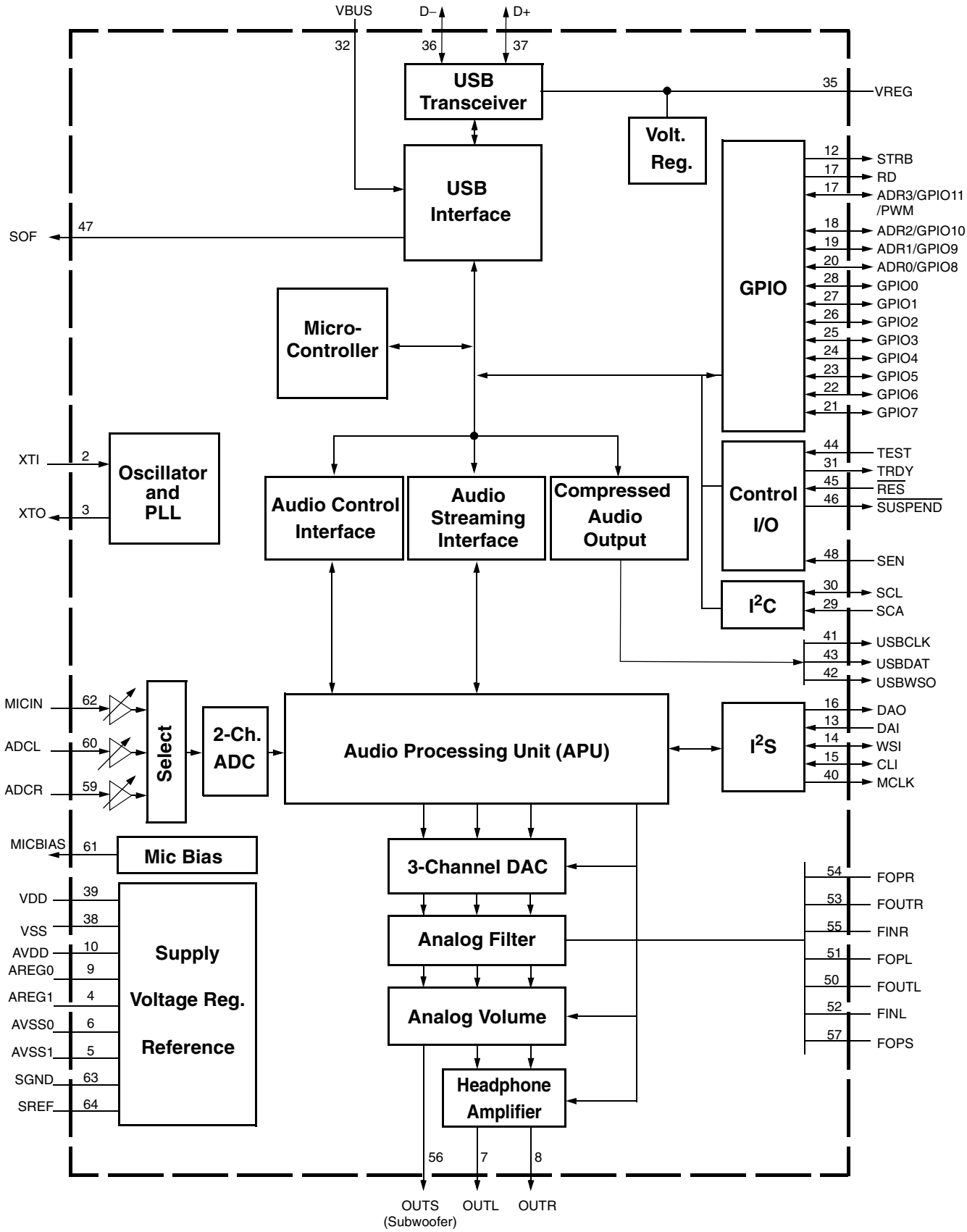


Fig. 2–1: Detailed block diagram of the UAC 355xB

2.1. General Information

This description summarizes all hardware platform capabilities of the UAC 355xB. The function of a certain application, however, is defined in the microcontroller's firmware. This is explained in Section 4. "Firmware" on page 21 for the standard codec and headset firmware.

The basic functions (playback, recording, audio control, HID) of the UAC 355xB can entirely be used by any USB operating system without additional drivers.

However, the IC offers far more functionality if vendor-specific controlling or download code is used. With external I^2C controlling, the IC can even work as an audio codec in a non-USB environment. The use of this complete functionality is not described in the standard data sheet and can be found in separate application notes (www.micronas.com).

A detailed block diagram of the UAC 355xB is depicted in Fig. 2–4. The functions of the blocks are explained in the following sections.

2.2. Universal Serial Bus (USB)

2.2.1. Transceiver

The differential input transceiver is used to handle the USB data signal according to the full-speed (12 MB/s) USB driver characteristics (USB SPEC 2.0). This block is supplied by an internal voltage regulator. The internal pull-up resistor on the D+ line, indicating that the UAC 355xB is connected to the USB bus, can be switched on and off by firmware.

2.2.2. USB Interface

The USB interface does all the low-level USB protocol handling, such as NRZI coding, bit stuffing and CRC computation. A receiver/transceiver logic handles the data traffic between the USB bus and the microcontroller memory.

2.2.3. Microcontroller

The microcontroller is an 8-bit RISC controller which handles the Chapter-9 processing and the decoding of class and vendor-specific USB requests. Detailed information is available in a separate document. The basic configuration is:

– 2 KB RAM

– 12 KB ROM

In addition to that, the UAC 3556B has an 8 KB RAM, which can be used instead of the lower 8 KB ROM for emulation purposes or as a RAM extension to the standard 2 KB RAM.

In the emulation mode, the UAC 3556B loads the 8 KB RAM via I^2C from an external EEPROM, disables the lower 8 KB ROM after that, and restarts the microcontroller, executing the code from RAM.

Another part of the RAM is reserved for download plug-ins. This is available in both UAC 3554B and UAC 3556B, and allows the addition of smaller portions of code to the basic firmware for extended functions or workarounds, if necessary. One example is adding extra functions to the GPIO pins, like control of external components via USB. Downloading of the plug-in can be done either from the USB host with an extra driver or from an external I^2C EEPROM.

2.3. GPIO

There are two groups of different types of GPIOs:

– Input and output pins: GPIO[0…11]

– Control pins: RD, STRB

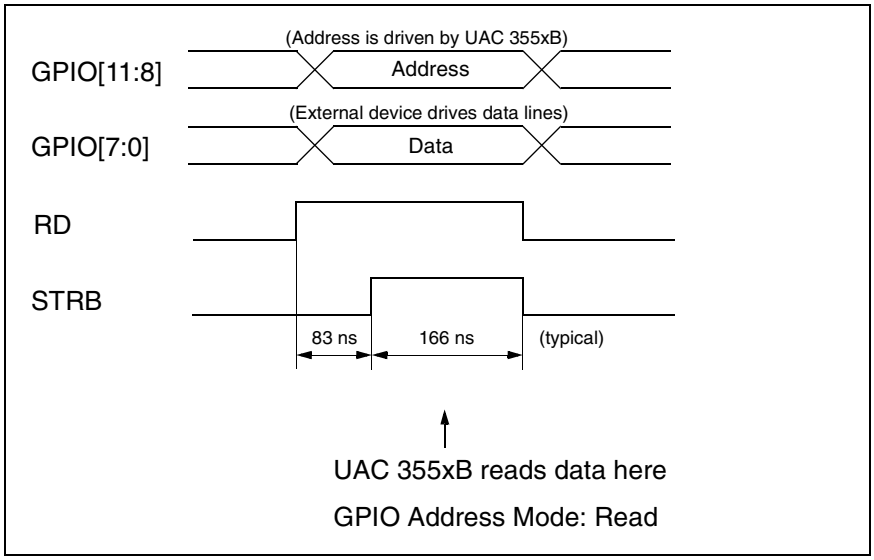


Fig. 2–2: UAC 355xB parallel interface timing (read)

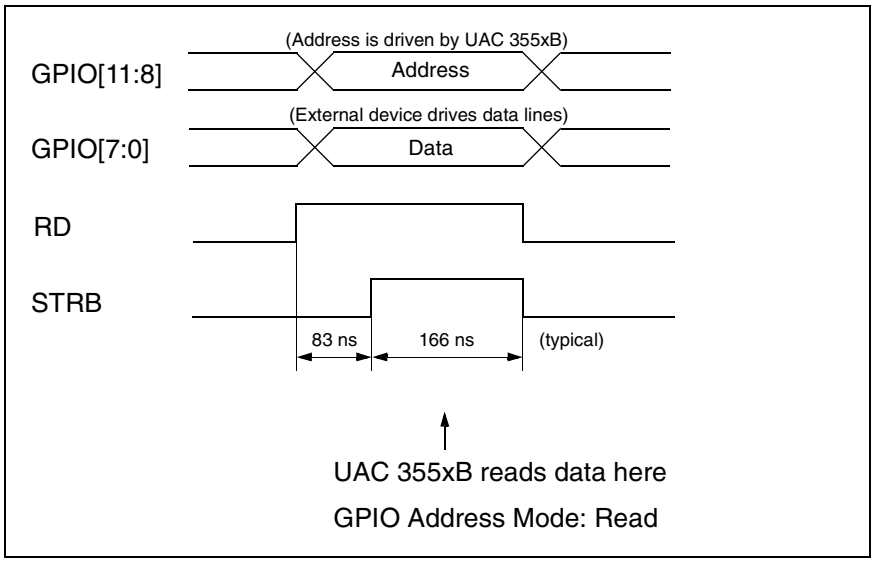


Fig. 2–3: UAC 355xB parallel interface timing (write)

The port pins can also be set into different electrical states:

– weak or strong driver strength

– output or tristate

– internal pull-down on or off

There are two GPIO pins with special alternate functions (see Table 2–1)

– GPIO[10] - Start Timer

– GPIO[11] - PWM Output

A description of these functions can be found in Section 2.4. “General Purpose Timer” on page 9.

2.3.1. GPIO port configurations

The UAC 355xB can set the GPIO port into different configurations.

Standard mode

In this mode the GPIO[0…11] pins are used as normal I/O pins, which can be set or read from the microcontroller.

Address mode

In this mode the GPIO pins can be used in a memory mapped fashion. There is a 16-Byte range of the microcontrollers address space which is transparent to the GPIOs. GPIO[0…7] are mapped to the data bus and GPIO[8…11] are mapped to the lower four bits of the address bus.

Table 2–1: GPIO port configurations

Pin name	Standard mode	Address mode
GPIO[0]	Generic I/O	Generic parallel I/O
GPIO[1]	Generic I/O	Generic parallel I/O
GPIO[2]	Generic I/O	Generic parallel I/O
GPIO[3]	Generic I/O	Generic parallel I/O
GPIO[4]	Generic I/O	Generic parallel I/O
GPIO[5]	Generic I/O	Generic parallel I/O
GPIO[6]	Generic I/O	Generic parallel I/O
GPIO[7]	Generic I/O	Generic parallel I/O
GPIO[8]	Generic I/O	Addr [0]
GPIO[9]	Generic I/O	Addr [1]
GPIO[10]	– Generic I/O – Start timer	Addr [2]
GPIO[11]	– Generic I/O – PWM out	Addr [3]
RD	no function	Shows I/O direction Read (high level) input Write (low level) output - timing diagram
STRB	no function	Strobe pulse, marks valid data

2.4. General Purpose Timer

The UAC 355xB audio codec family incorporates a timer. It is a 16-bit counter with clock prescaler. The clock runs at 12 MHz. The prescaler can be set to divide by 1 to 256.

The current value of the counter can always be read back.

The timer initiates interrupts on reaching the count value MaxA.

The UAC 355xB can start the timer with a “high" level on GPIO[10].

The timer can be switched to PWM generation to configure GPIO[11] as PWM output.

The structure of the timer is shown in Fig. 2–4. The PWM output and timer frequencies can be calculated as shown in Figure 2–5.

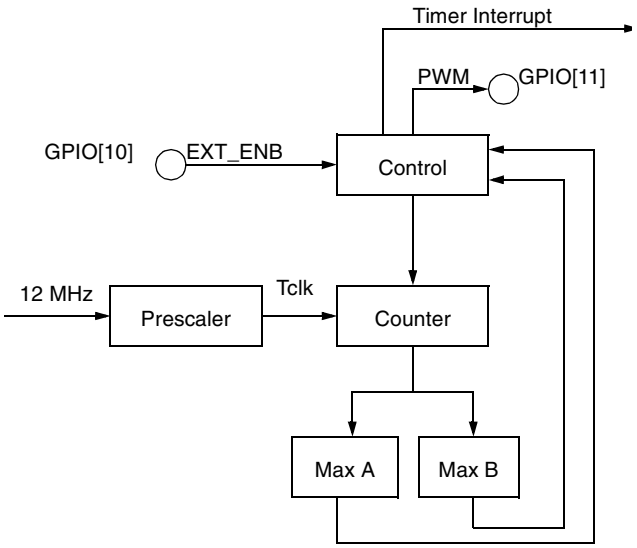


Fig. 2–4: Timer structure

Timer frequency:
Tclk = 12 MHz / Prescale

PWM frequency:
PWM = Tclk / (MaxA + MaxB)

Fig. 2–5: PWM timing

2.5. Audio Interface

2.5.1. Audio Streaming Interface

The audio streaming interface directly connects the USB interface to the APU in order to transmit the digital audio data in both directions for playback and record. The following data formats are supported:

Table 2–2: Audio Formats

Playback	Record
16-bit MONO	8-bit MONO
16-bit STEREO	16-bit MONO
24-bit STEREO	16-bit STEREO

2.5.2. Audio Control Interface

The Audio Control Interface links the microcontroller to the APU and is used to initialize the APU and to transmit audio-related USB control data, such as volume setting, tone control etc.

The Audio Control Interface supports full access to all APU registers via the microcontroller.

2.5.3. Serial Data Output

Used Pins: USBCLK, USBDAT

This interface provides a data path for transferring compressed audio to peripheral ICs, such as Micronas' Dolby Digital decoder MAS 3528E or to an MP3 decoder, e.g., the MAS 3507D or MAS 3509F. This works independently from the normal USB playback. The audio format on the USB-OUT pins is burst I^2S.

Note: If this interface is used, the "Asynchronous I^2S input with optional I^2S output" is not available and vice versa.

This interface operates in different modes:

2.5.4. Direct Streaming

In this mode, there is no preprocessing of the timing, i.e., the data on USBDAT are in phase with the 12 MHz data on the USB bus, which are sent to a specific endpoint. This can be bulk or isochronous data. The data appear as they are sent on the USB bus.

2.5.5. Microcontroller Streaming

In this mode, the microcontroller copies the data from the RAM to a shift register, which is connected to the USBDAT pin. The shift clock can be programmed between 6 MHz and 750 kHz and appears on USBCLK pin.

2.6. The UAC 355xB Serial Audio Interfaces

Used Pins: DAO, DAI, WSI, CLI, USBDAT, USBCLK

The UAC 3556B offers two digital serial interfaces (I2S). They are directly connected to the APU.
The I^2S interfaces operate in 16-bit or 32-bit mode. The master clock (MCLK) is programmable to 18.432 MHz, 24.576 MHz or 36.864 MHz. Delayed word strobe or standard I^2S format can be selected via the programmable delay bit. Word strobe polarity is programmable, too. Detailed timing diagrams can be found in Section 5.6.4. "I^2S Interface Timing Characteristics" on page 46.

2.6.1. Synchronous I^2S Input/Output

Used Pins: DAO, DAI, WSI, CLI

In this mode, the UAC 355xB is master on the I^2S, i.e, it generates WSI and CLI for a fixed 48 kHz sampling rate. External I^2S sources must deliver data synchronous to the output.

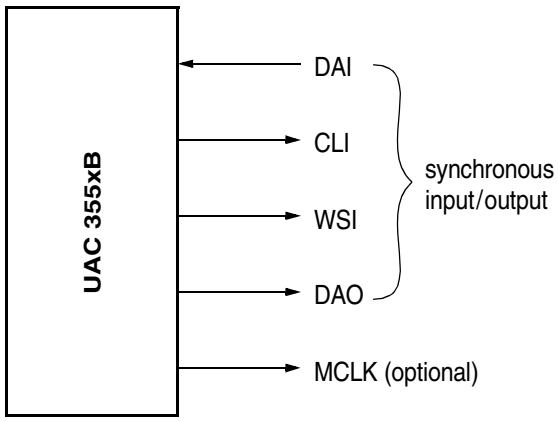


Fig. 2–6: Synchronous I^2S Input/Output

2.6.2. Asynchronous I^2S input

Used Pins: DAI, WSI, CLI

In this mode the UAC 355xB is slave, i.e., asynchronous input is possible at a sampling rate range from 6.4 kHz to 48 kHz. The external I^2S source provides DAI, WSI, and CLI

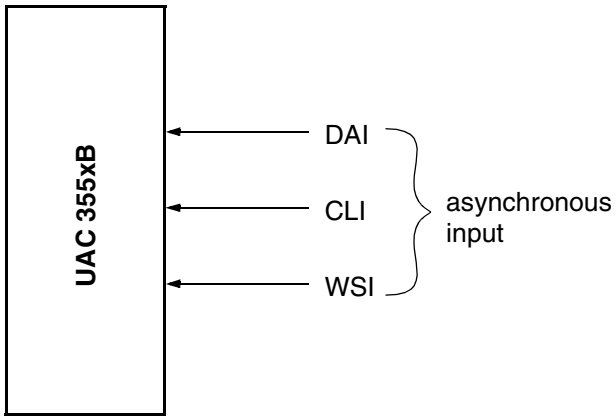


Fig. 2–7: Asynchronous I^2S input

2.6.3. Asynchronous I^2S input with optional I^2S output

Used Pins:
Output:USBDAT, USBCLK, USBWSO
Input: WSI, CLI, DAI

In this mode the I^2S burst interface pins USBDAT, USBCLK and USBWSO can be used for synchronous I^2S output (if the burst interface is not used), as described in Figure 2.6.1. The I^2S input pins WSI, CLI, DAI, however, operate asynchronously as described in Figure 2.6.2.

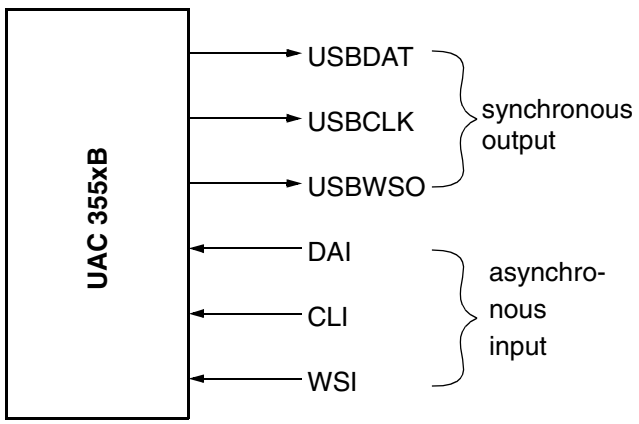


Fig. 2–8: Asynchronous I^2S input with optional I^2S output

2.7. Power Supply

The UAC3554/6B has on-chip voltage regulators providing the optimal supply voltages for the analog and digital sections, thus allowing to power the IC by the USB Bus supply lines, as well as from external supply. They also serve to reduce cross-talk and EMI.

For stable operation, all regulators need external capacitors.

The regulators are:

1. VREG:
   3.4 V regulator for USB-signalling (saving external regulator)
2. AREG0:
   3.5 V regulator for analog back-end
3. AREG1:
   3.5 V regulator for analog circuitry apart from back-end.

Reference voltage for analog signals:

SREF:
1.7 V (optional 2.3 V) reference voltage for analog circuitry.

Note: It is recommended for AVSS0/1, SGND and VSS to be connected. In certain applications, however, it may be better to split signal ground from the other grounds in order to reduce noise.

Five-Volt Mode

If a higher output level is required, the IC can operate in 5 V mode. In this case, the IC is powered from an external 5 V supply: AVDD has to be connected to AREG0 and AREG1 and SREF must be switched to 5 V mode.

2.8. I^2C Bus Interface

Pins: SDA, SCL

The UAC 355xB is equipped with an I^2C bus master/slave interface. Bus format and timing follow the original specification for I^2C (The I^2C Specification V2.1).
It operates with 5 V signalling at 100 kHz or 400 kHz.
Both master and slave mode require support from the microcontroller firmware.

2.8.1. I^2C Master

This mode allows control of external I^2C devices, such as EEPROMs, LCD-Displays etc. This interface is used to download configuration data and firmware from an EEPROM after power-up. The bus protocol (subaddressing and packet length) is defined by firmware and therefore programmable.

Note: Micronas standard firmware (Section 4. “Firmware” on page 21) provides support for USB to I^2C bridging, allowing control of I^2C devices via USB.

2.8.2. I^2C Slave

In I^2C slave mode, the interface provides an interrupt to the microcontroller after detecting the assigned I^2C address (0x48). The corresponding interrupt service routine handles this request and interprets incoming data according to the application.
One example of handling could provide full access to all memory locations.

2.9. Microphone and Line Input

Pins: ADCR, ADCL, MICIN, MICBIAS

The UAC 355xB provides a 2-channel ADC. The A/D converters achieve a signal-to-noise ratio better than 90 dB (typ.) and a bandwidth of 20 kHz (at f_s=48 kHz).

The left channel can be used as microphone or line input, whereas the right channel is always line input. Programmable input gain allows adaption of the input levels to the ADC range.

The UAC 355xB allows direct connection to an electret microphone and provides the microphone bias voltage of 3.1 V (0.5 mA max.) on a separate pin, too. The microphone bias is automatically switched on when the microphone input is selected. The output resistance of the MICBIAS pin is typically 180 Ω.

There is a fixed +21.5 dB gain followed by a programmable gain of 0 dB to +22.5 dB. Table 2–3 shows the microphone voltage versus gain setting and the input impedance (depends on gain setting) for full range ADC input (clipping level).

Table 2–3: Microphone input levels

Microphone Voltage [mV_{PP}] 3 V Mode	Microphone Voltage [mV_{PP}] 5 V Mode	Gain Setting [dB]	Input Impedance [kΩ]
283	377	0	137
238	317	1.5	117
200	267	3	100
168	225	4.5	85
142	189	6	72
119	159	7.5	62
100	134	9	52
84	113	10.5	44
71	95	12	37
60	80	13.5	32
50	67	15	27
42	56	16.5	23
36	47	17	19
30	40	19.5	16
25	34	21	14
21	28	22.5	11

The input gain for the line input is programmable in the range of –3 dB to 19.5 dB. Table 2–4 shows the line input voltage versus gain setting and the input impedance (depends on gain setting) for full range ADC input (clipping level).

Table 2–4: Line input levels

Line Input Voltage [mVpp] 3 V Mode	Line Input Voltage [mVpp] 5 V Mode	Gain Setting [dB]	Input Impedance [kΩ]
3388	4517	–3	85
2851	3801	–1.5	79
2399	3198	0	73
2018	2691	1.5	67
1698	2264	3	61
1429	1905	4.5	55
1202	1603	6	49
1011	1349	7.5	44
851	1135	9	39
716	955	10.5	34
602	803	12	30
507	676	13.5	26
427	569	15	23
359	478	16.5	19
302	403	17	17
254	339	19.5	14

After A/D conversion there is a digital quasi-peak meter providing level information in APU register.
If Mic input is selected, there is the option to switch the signal to both channels. In this case, the left channel is copied to the right channel after the peak meter.

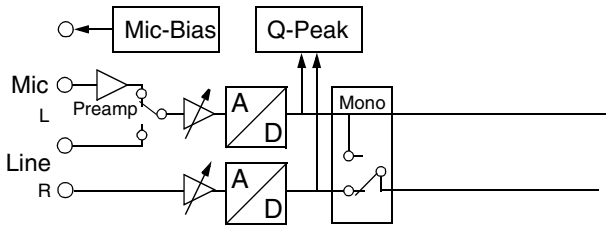


Fig. 2–9: Analog input configuration

2.10. Analog Output

Pins: OUTL, OUTR, OUTS
FOPL, FOPR, FOUTL, FOUTR, FINL, FINR, FOPS

The analog output system comprises the stereo audio DAC, the subwoofer DAC, analog filters, op-amps for external out-of-band-noise filters, analog volume, mute, and the output amplifiers.

2.10.1. Digital-to-Analog Converters

The UAC 355xB uses three multibit sigma delta DACs with high linearity and SNR better than 95 dBA.

2.10.2. Analog Filter

Pins: FOPL, FOPR, FOUTL, FOUTR, FINL, FINR, FOPS

This block contains the op-amps for the optional analog external out-of-band-noise filters. It is recommended to use a second-order filter for the main channels (OUTL, OUTR) (see Section 6. “UAC 355xB Applications” on page 48). It is possible to omit these filters and to save the external components. In this case, the op-amp has to be switched off and the pins FOOTL/R, FINL/R and FOPL/R must be connected. The output signal will contain more out-of-band noise, which is not audible, however.

A first-order filter is required for the subwoofer output in order to attenuate the out-of-band noise caused by the sigma delta DACs.

2.10.3. Analog Volume

The analog volume covers a range from +6 dB to −18 dB with 1.5 dB step size. But this is the analog component of the overall volume system which covers a range from +12 dB to −114 dB with 1 dB step size and additional mute position. It is split into analog and digital volume. This splitting ensures that the DAC performance parameters do not degrade at reduced volume settings. The splitting is embedded in the audio processing and cannot be modified.

Note: Positive volumes will degrade the THD at high input levels.

2.10.4. Line-out/Headphone Amplifier

Pins: OUTL, OUTR

Stereo Mode

The line-out/headphone amplifier output is provided at the OUTL and OUTR pins connected either to stereo headphones or to a power amplifier. The stereo headphones require external serial resistors in both channels. See Section 6. “UAC 355xB Applications” on page 48.

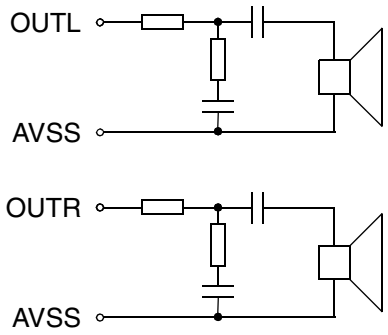


Fig. 2–10: Loudspeaker connection for Stereo mode

Mono Mode

In Mono mode, the DC coupling capacitors and further filter circuitry are not required. In this mode, the output pins OUTL/R operate in bridge mode with complementary signals. Therefore, the maximum output power increases, allowing small speakers to be driven directly.

Fig. 2–11: Loudspeaker connection for Mono mode

2.10.5. Subwoofer Output

Pins: OUTS

The subwoofer output is designed for driving an external amplifier. The audio processing provides a programmable split filter and active bass management algorithms.

Note: If the capacitive load is too high, a serial resistor is required.

2.11.Special I/O

Pins: SOF, SEN, $\overline{\text{SUSPEND}}$, $\overline{\text{RESET}}$

The following sections describe some pins with special functions.

2.11.1. SOF (Start of Frame)

The SOF pin provides a 1 ms periodic signal which is derived from the USB frame rate. It can be used for test purpose or as an USB-synchronous reference for vendor-specific external circuitry.

2.11.2. SEN (Suspend Enable)

Pin: SEN

This is a digital input that prevents the device from entering the low-power mode (Suspend). The UAC 355xB enters a low-power mode if:

– there is J-state on D+, D– lines (USB-Suspend) and V bus high

– V bus is low (USB disconnected)

Note: Both cases must be supported by the firmware

In case of USB-Suspend, the SEN pin is also used as an input for the remote wake-up function.

Table 2–5: SEN pin

SEN	
high	suspend enabled
low	suspend disabled/remote wake-up

2.11.3. Suspend

Pin: $\overline{\text{SUSPEND}}$

The $\overline{\text{SUSPEND}}$ pin is a digital output pin which indicates the low-power mode. It can be used to power down external circuitry, such as power amplifiers in a USB speaker.

Table 2–6: $\overline{\text{SUSPEND}}$ pin

SUSPEND	
high	normal power
low	low power

2.11.4. Reset

Pin: $\overline{\text{RES}}$

The $\overline{\text{RES}}$ pin resets the UAC 355xB. During power-up the $\overline{\text{RES}}$ pin should be low until the clock system is up and running. Then this pin can be released and the UAC 355xB enters normal operating mode.

Note: In low-power mode, the RES pin must not be low to avoid restart of the clock system and therefore entering normal power mode.

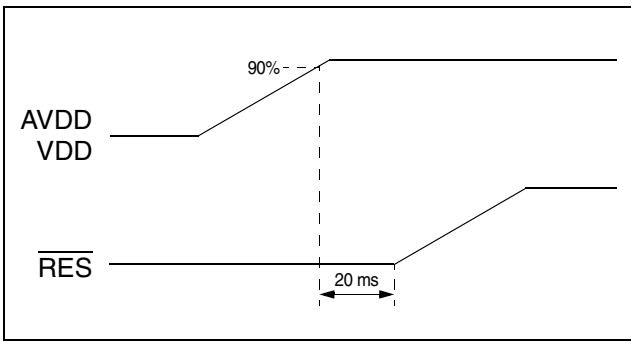


Fig. 2–12: Timing diagram of the reset procedure

2.12. Clock System

Pins: XTI, XTO

The UAC 355xB requires a 12 MHz clock source, which is realized as an on-chip oscillator with external crystal. Also an external oscillator can be used. In this case, the clock has to be connected to XTI (see also Section 6. “UAC 355xB Applications” on page 48). The 12 MHz is the input clock for a PLL circuit which generates all clocks needed within the IC.

The clock for the APU is programmable either to 48 MHz or 72 MHz. In case of 48 kHz, the UAC 355xB consumes less power, but on the other hand a reduced feature-set for the audio processing has to be taken into account (see Fig. 3–1 on page 17).

3. Audio Processing

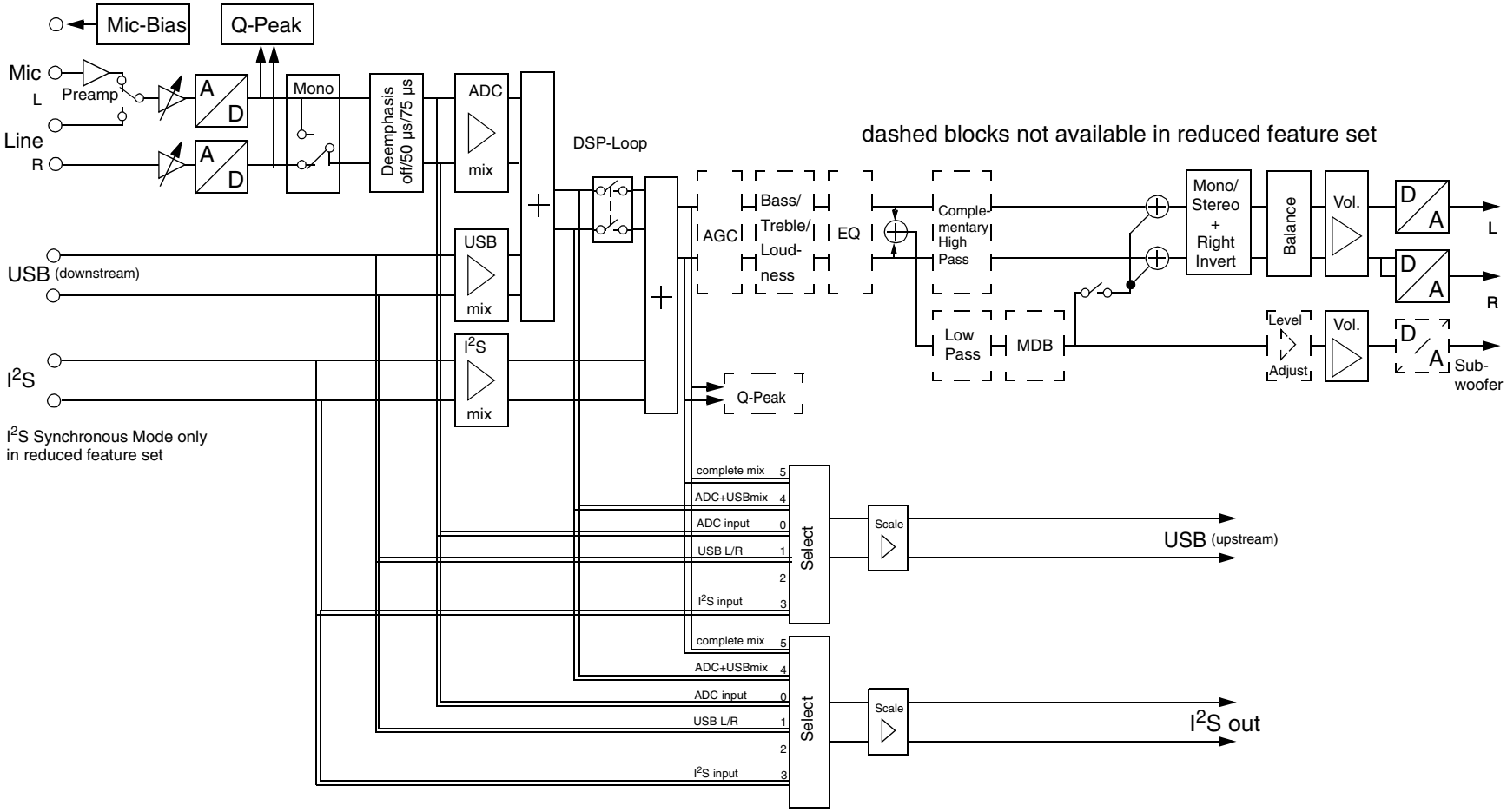


Fig. 3–1: Signal flow in the audio processing unit (APU)

The audio processing is realized by APU firmware. The audio building blocks can be split into USB-independent features such as parametric equalizer, I^2S I/O, and blocks which belong to USB feature units, mixer units, and selection units defined in the USB Device Class Definition for Audio Devices.

The USB feature unit provides basic manipulation of the incoming logical channels and can be controlled by the standard windows mixer tool. The parameters for the USB-independent features are predefined in the internal ROM, in an external EEPROM or a special host application which drives the IC.

The UAC 355xB supports two logical channels (i.e. left and right) and a subwoofer channel which is derived with a split filter from left and right. Multichannel or surround systems, however, can also be realized using more than one UAC 355xB, because phase or delay distortion is eliminated in the device by locking the audio processing to the USB frame rate. An overview of the architecture is given in Fig. 3–1 on page 17.

If the APU works with a 48 MHz clock it is necessary to select the reduced feature mode. The blocks, which are not available in reduced feature mode are shown with dashed lines in Fig. 3–1 on page 17.

3.1. DSP Loop

The DSP-Loop block symbolizes the option to route the audio signal to an external DSP and back into the UAC 355xB via I²S I/O. This allows to add more audio processing algorithms.

3.2. Automatic Gain Control

The Automatic Gain Control (AGC) is one of the building blocks of the feature unit (USB Device Class Definition for Audio Devices 1.0, page 39).

Different sound sources fairly often do not have the same volume level. The Automatic Gain Control solves this problem by equalizing the volume levels within a defined range. Below a threshold level the signals are not affected. The level-adjustment is performed with time constants in order to avoid short-time adjustments due to signal peaks.

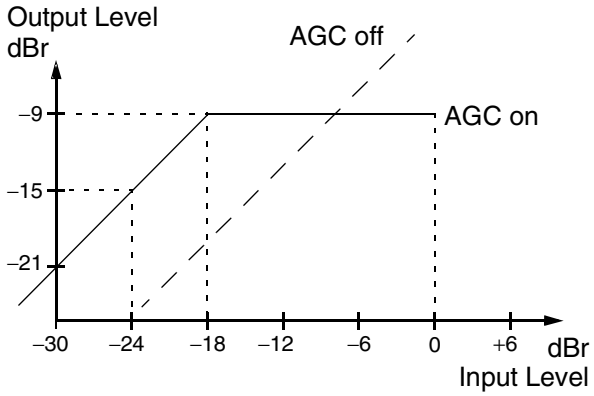


Fig. 3–2: Simplified AGC characteristics

Table 3–1: AGC parameters

Parameter	Settings	Default
Decay time	8 seconds 4 seconds 2 seconds 20 ms	4 seconds

3.3. Quasi-Peak

Two quasi-peak detectors are provided:

1. after the ADCs. This allows the programming of an AGC in the microcontroller[1)] or a VU-meter on the host side.
2. in the DAC channel. This can be used, e.g., for a VU-meter on the host side.

The feature is based on using fast attack and slow decay time constants.

3.4. Bass Control

The bass control provides gain or attenuation to frequency components below a corner frequency of 120 Hz. The bass control works identically on both channels in a range of –12 dB to +12 dB.

3.5. Treble Control

The treble control provides gain or attenuation to frequency components above a corner frequency of 6 kHz. The treble control works identically on both channels in a range of –12 dB to +12 dB.

[1)] not supported by standard microcontroller firmware

3.6. Parametric Equalizer

The parametric equalizer is an audio feature which is not accessed via standard USB controls. It allows the compensation of the frequency response of a speaker. Alternatively, frequency responses can be set to suit individual tastes. The equalizer consists of 5 individually adjustable bands. The control parameters and the parameter range for each band is shown in Table 3–2.

Table 3–2: Equalizer parameters

Parameter	Min	Max
Center Frequency	50 Hz	15 kHz
Gain/Attenuation	–6 dB	+6 dB
Filter Quality (Q)	0.5	3

The adjustment of the equalizer is supported by an application program that allows to set up frequency responses and to download the corresponding filter coefficients into the UAC 355xB. When the frequency response matches the requirements, it can be programmed into the external EEPROM or can be set by a vendor specific device driver. The UAC 355xB is shipped with a flat frequency response.

3.7. Volume, Mute, and Balance Control

The volume control is partly realized in the analog back-end. This preserves high audio quality (SNR) at low volume settings because signal and noise are attenuated in the same way. This is not the case for devices with pure digital volume control. The UAC 355xB uses digital volume control only for the fine tuning. The volume setting is smoothed by an internal ramping algorithm in order to avoid audible clicks during volume change. The splitting between analog and digital volume is handled by the UAC 355xB automatically.

The balance is implemented digitally by attenuating one channel.

The mute control is part of the volume system in the UAC 355xB. It functions simultaneously on both channels and can be switched on and off under USB control. Similar to the volume control, clicks are avoided by a ramping algorithm.

3.8. Subwoofer Output and Bass Management

The subwoofer signal is created by combining the left and the right channels directly behind the equalizer block using the formula (L+R)/2. Due to division by 2, the D/A converter will not be overloaded, even with full-scale input signals. The subwoofer is filtered by a third-order low-pass filter with programmable corner frequency and programmable characteristic followed by a level adjustment. At the main channels a complementary high-pass filter can be switched on. Subwoofer and main output use the same volume.

Please note, that the predefined subwoofer parameters in the internal ROM are set in such a way, that the low frequencies of both channels are summed up and are distributed equally to left and right channel. This reduces the risk of overload of the speakers, but degrades the channel separation for low frequencies. Since the human perception cannot extract information about direction from low frequencies, this is no drawback.

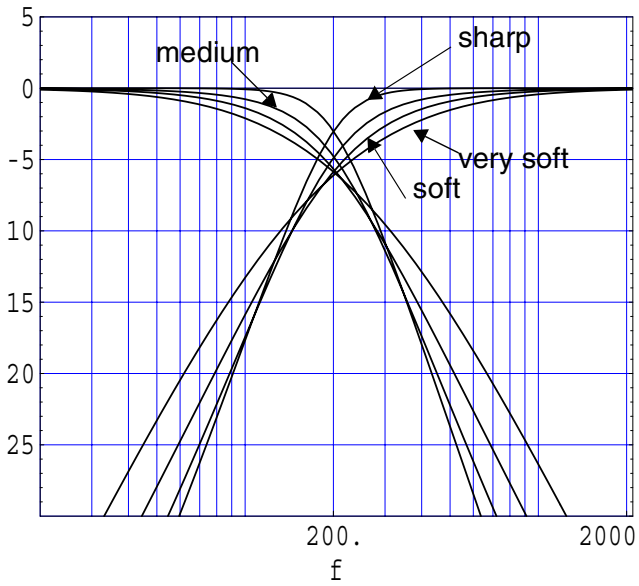


Fig. 3–3: Subwoofer characteristics (e.g. f_c = 200 Hz)

Table 3–3: Subwoofer parameters

Parameter	Settings/ Range	Default
Corner Frequ.	50 to 400 Hz	90 Hz
Characteristic	– sharp edge – medium edge – soft edge – very soft edge	sharp edge

Table 3–3: Subwoofer parameters, continued

Parameter	Settings/ Range	Default
Complementary High-Pass Filter for L/R channel	– L/R unfiltered – L/R high-pass-filtered – Subw. added to high-pass-filtered L/R	Subw. added to high-pass-filtered L/R
Level Adjustment	–60…+12 dB (relative to main volume)	0 dB
Subw. DAC	– off – on	on

3.9. Micronas Dynamic Bass (MDB)

The **M**icronas **D**ynamic **B**ass algorithm (MDB) implements a sophisticated bass boost system, which extends the frequency range of loudspeakers or headphones.

The MDB is placed in the subwoofer path. For applications without a subwoofer, the enhanced bass signal can be added back onto the left/right channels. Micronas Dynamic Bass combines two effects: dynamic amplification and adding harmonics.

Several parameters allow tuning the characteristics of MDB according to the loudspeaker, the cabinet, and personal preferences. For more detailed information on how to set up MDB, Micronas will provide an appropriate Application Note.

Table 3–4: MDB parameters

Parameter	Range	Default if disabled	Default if enabled
Effect Strength	off…max	off	medium
Harmonic Content	0…100%	0%	50%
Center Frequency	20…300 Hz	90 Hz	90 Hz
Amplitude Limit	–32…0 dBFS	0 dBFS (=no limit)	0 dBFS (=no limit)
Subwoofer Settings	two sets for MDB off/on available, for parameters see Table 3–3		

3.9.1. Dynamic Amplification

Since the human impression of loudness depends on the frequency, a dynamic compression of the low frequencies adapts the sound to the human perception.

In order to prevent clipping and to adapt the system to the signal amplitude which is really present at the output of the device, the MDB contains a definable limit. The output signal amplitude is monitored and if it comes close to the limit, the gain is reduced automatically. Clipping effects are avoided.

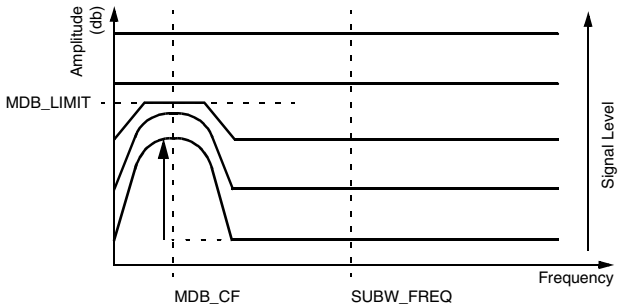


Fig. 3–4: Dynamic amplification

3.9.2. Adding Harmonics

MDB exploits the psychoacoustic phenomenon of the ‘missing fundamental’. Adding harmonics of the frequency components below the cutoff frequency gives the impression of actually hearing the low frequency fundamental. In other words: Although the loudspeaker system is not capable of generating such low frequencies, the listener has the impression that it reproduces them.

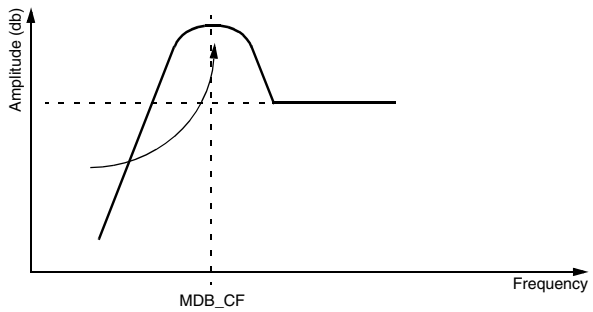


Fig. 3–5: Adding harmonics

4. Firmware

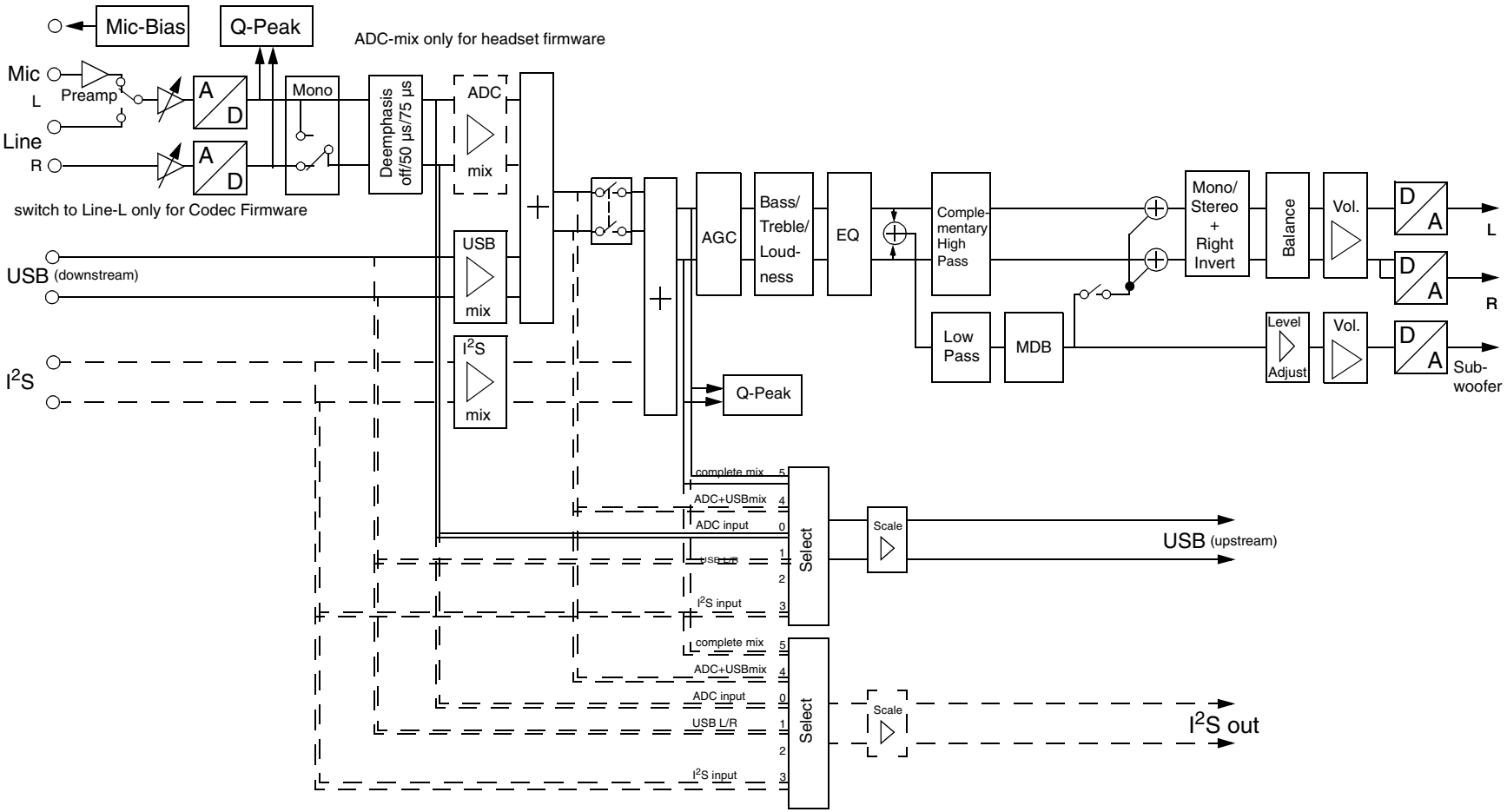


Fig. 4–1: Signal flow in the audio processing unit controlled by the codec/headset firmware using standard OS driver

The previous chapters describe the UAC 355xB from the hardware point of view. The complete functionality, however, is defined by the microcontroller firmware. This firmware tailors the device to a specific application.

Micronas offers two standard firmware versions embedded in the ROM.

– UAC 3555B: Standard Codec

– UAC 3554B: Standard Headset

Note: It is possible to customize many parameters (IDs, strings, equalizer setting etc.) by means of an external EEPROM.

Both firmware versions are very similar. Differences are mentioned in the following chapters.

4.1. Features

The main features of the standard firmware versions are:

– USB playback and record with independent sample rates

– Sample rates from 6.4 kHz to 48 kHz

– Microphone or Line input
(only mic for UAC 3554B)

– Audio baseband processing incl. dynamic bass management and subwoofer split filter

– Basic audio control by GPIO-HID

– Suspend mode and remote wake-up support

– I^2C master/slave support

– Bootloader permitting download of configuration data, plug-ins or complete firmware (only for UAC 3556B) after power-on

– Plug-in support (downloadable firmware extensions from external EEPROM or WIN driver).

Most of the functions are defined in the device and configuration descriptor. The following chapters provide all noteworthy information, which is buried in this descriptors. It is assumed that the reader is familiar with the basic USB notation (USB Spec 2.01/ www.usb.org).

4.2. Device Descriptor

The device descriptor contains the downloadable IDs and the index for several strings.

Table 4–1: Programmable Device Descriptor Items

Item	Default UAC 3555B	Default UAC 3554B
idVendor	0x074D	0x074D
idProduct	0x3554	0x3554
bcdDevice	0x000x[1)]	0x000x[1)]
iManufacturer	0x01	0x01
iProduct	0x02	0x02
iSerialNumber	0x00	0x00
[1)] Changes with firmware revisions		

Associated to the string index there are three programmable strings. The ROM firmware defines only two:

Table 4–2: Strings

String	Default UAC 3555B	Default UAC 3554B
Manufacturer String	Micronas	Micronas
Product String	UAC 3555B	UAC 3554B

4.3. Configuration Descriptor

The configuration descriptor contains information on the bus/self-powered and remote wake-up capabilities. The UAC 355xB allows all combinations of these features. There is also a string index, allowing to associate a string to this configuration. The default string is a date code (time of code assembly). These items are programmable:

Table 4–3: Programmable Configuration Descriptor Items

Item	Default - UAC 3555B	Default - UAC 3554B
iConfig	0x01	0x01
bmAttributes	0xe0 (self-powered, remote wake-up)	0xa0 (bus-powered, remote wake-up)
MaxPower	0x00 (0 mA)	0x32 (100 mA)

The configuration descriptor also provides all information concerning the audio flow in the Class Specific Audio Control Interface. Fig. 3–1 on page 17 shows the graphical representation for the codec firmware.

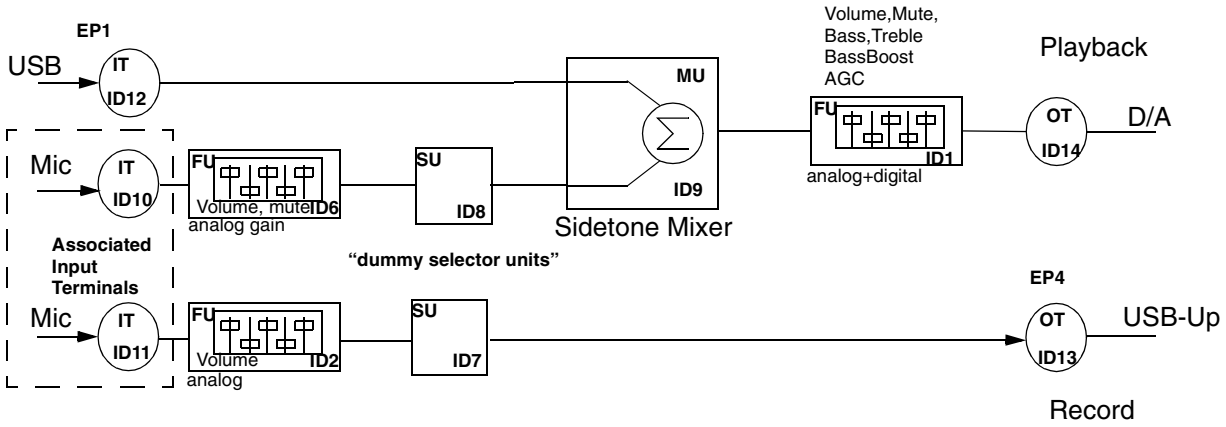


Fig. 4–2: Standard headset audio signal flow

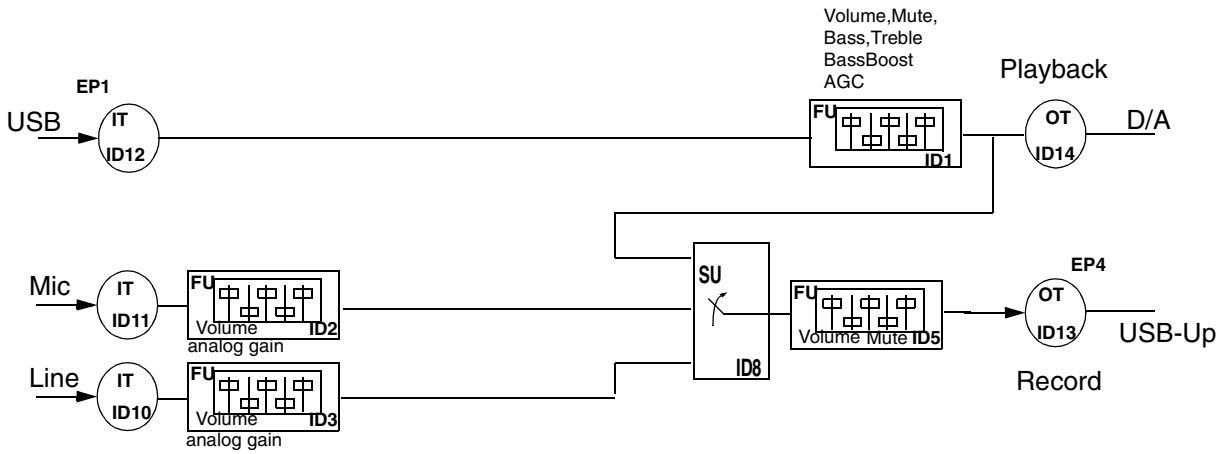


Fig. 4–3: Standard codec audio signal flow

These are the audio structures and how they appear to the USB host. Without any additional drivers the Microsoft Windows operating system provides sliders in the mixing tool to control volume setting, selectors etc. Using a vendor specific application, however, it is possible to extend this to the full signal routing capabilities (see Section 3.1. on page 18).

Static modifications (without sliders), like

– adding a sidetone path (analog-in to analog-out) to the codec firmware

– adding I^2S I/O

can be achieved by plug-ins from external EEPROM or Windows device driver.

The switching units SU7 and SU8 in the headset firmware are dummy units and allow the operating system to parse the descriptor correctly.

The mapping of this audio structure to the overall audio processing in the APU is shown in Fig. 4–1 on page 21. The dashed lines show signal paths which cannot be activated by standard Windows drivers and need support of vendor-specific drivers and applications (driver available from Micronas), especially for I^2S input/output.

Note: BassBoost enables a dynamic bass management algorithm with programmable (external EEPROM) characteristics.

The next part of the configuration descriptor defines the audio format for playback and record. This is not programmable.

Table 4–4: Supported audio formats

Playback	Record
16-bit Mono	8-bit Mono
16-bit Stereo	16-bit Mono
24-bit Stereo	16-bit Stereo

The UAC 355xB accepts all sample rates from 6.4 kHz to 48 kHz independently for playback and record.

The final portion of the configuration descriptor defines the HID functions:

The codec firmware uses the GPIO pins to connect keys which are related to the USB HID class. The standard configuration defines the GPIO0 to GPIO3 as input pins for the audio control shown in Table 4–5.

Table 4–5: Standard key configuration

Pin	Function
GPIO0	Volume Up
GPIO1	Volume Down
GPIO2	Mute on-off toggle
GPIO3	BassBoost on-off toggle

Codec Firmware

GPIO[4..11] pins are not assigned to HID functions and can be used by a vendor specific driver or plug-in. Each pin can be configured as input or output pin with programmable pull down resistor and weak or strong driver strength.

GPIO[4...7] are used as media control keys:

Table 4–6: Media control keys

Pin	Function
GPIO4	Next Track
GPIO5	Previous Track
GPIO6	Stop
GPIO7	Play/Pause

With the use of this pins, the Windows Media Player can be controlled directly.

The keys are polled every 1 ms by the microcontroller and the corresponding key codes are transmitted to the host on request when a key enters “high” state. The hosts polling rate is 8 ms. This parameter, however, is part of the configuration set, which can be downloaded from an external I^2C EEPROM.

Headset Firmware

In addition to the basic audio control there is a local mic-mute, controlled by GPIO[4]. A button connected to VDD allows to toggle between mic mute and unmute. For indication of the mute status an LED can be connected to GPIO[11]. This LED will stay solid if mic is NOT muted and will blink in 500ms rate if the mic is muted. Sidetone level is also muted with this function. However, the mute state is NOT reported to WIN OS and therefore the mute indicator in the WIN mixer will not change by this local mic mute. The WIN mixer can overwrite the local sidetone mute, i.e., switch sidetone on again, even if the recording path is still muted.
GPIO[5...10] are not used in the headset.

4.3.1. Audio Class Requests

The codec firmware supports all audio class requests which are required by the audio flow shown in Fig. 4–2 and Fig. 4–3. The MIN/MAX/RES setting follow the limits which are defined in the audio processing apart from the main volume setting (FU1). In this case the overall range from –114 dB to +6 dB is limited to –40 dB to +3 dB (plus mute position) in order to fit the audible range to the volume slider in the WIN mixer.

4.4. Vendor-Specific Requests

These requests provide functions which extend standard controlling of the operating system. Micronas provides a driver for Windows-operating systems which supports:

– SET MEM
This request allows writing all RAM and Register locations on the chip.

– GET MEM
This request allows reading all memory locations on the chip. Block read is supported.

– SET I^2C
This vendor request allows driving the I^2C-master in the codec firmware. It allows writing to external I^2C devices.

– GET I^2C
This request supports I^2C master reading from external devices.

4.4.1. Bootloader

The bootloader is a part of the firmware which allows communication with an external I^2C EEPROM. The bootloader runs immediately after power-on. At this time the device is not connected to the USB bus. When the bootloader is finished, the pull-up resistor is switched on the D+ line. If no external EEPROM, according to the configuration shown in Table 4–8 is found, the UAC 355xB continues with the internal ROM code. After download of a complete firmware (UAC 3556B only), the bootloader resets the device and the code that was just downloaded is executed.

The UAC 355xB can have different EEPROMS connected to the I^2C bus. The UAC 355xB works as an I^2C bus master at this point in time. Depending on EEPROM size, the EEPROM can hold different content.

Various I^2C EEPROM configurations can be used by means of bootstrap options at the pins USBDAT, USBCLK, and USBWSO:

Table 4–7: Supported I^2C EEPROM types

EEPROM size	Purpose
2 kbit	Configuration only
4…32 kbit	Configuration Plug-in software
64 kbit	Configuration On reset loadable firmware
128 kbit	Configuration On reset loadable firmware Plug-in software

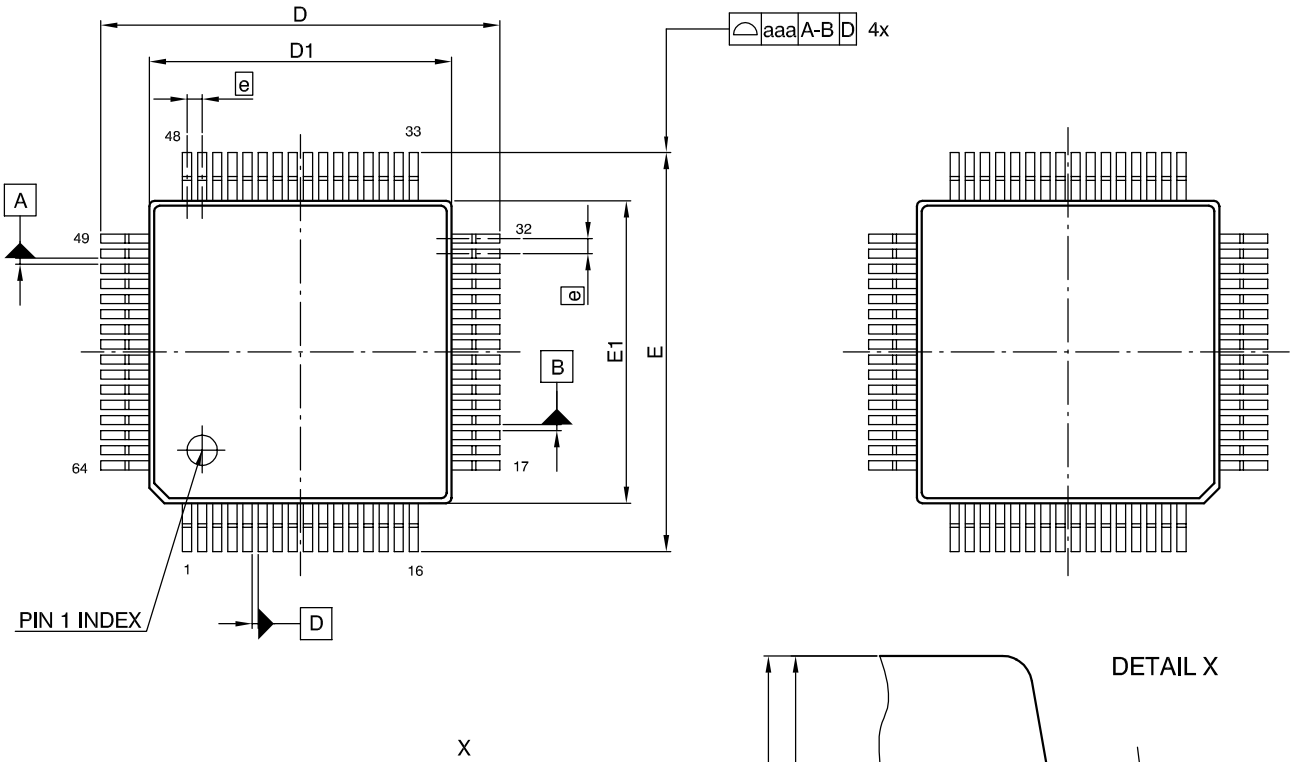
Note: UAC 3554B and UAC 3555B cannot load external firmware.

Table 4–8: I^2C-Mode of external EEPROM

USBWSO	USBDAT	USBCLK	Address Subaddress	Purpose
1	1	don't care		internal ROM only I^2C master disabled
1	0	don't care	0x50 1 byte subaddressing (UAC 3554B and UAC 3555B only)	Configuration data Plug-in software 100 kHz I^2C master
0	1	0	0x51 2 byte subaddressing	Configuration data On reset loadable firmware Plug-in software 400 kHz I^2C
0	1	1	0x52 2 byte subaddressing	Configuration data On reset loadable firmware Plug-in software 400 kHz I^2C
0	0	0	0x51 2 byte subaddressing	Configuration data On reset loadable firmware Plug-in software 100 kHz I^2C
0	0	1	0x52 2 byte subaddressing	Configuration data On reset loadable firmware Plug-in software 100 kHz I^2C

5. Specifications

5.1. Outline Dimensions



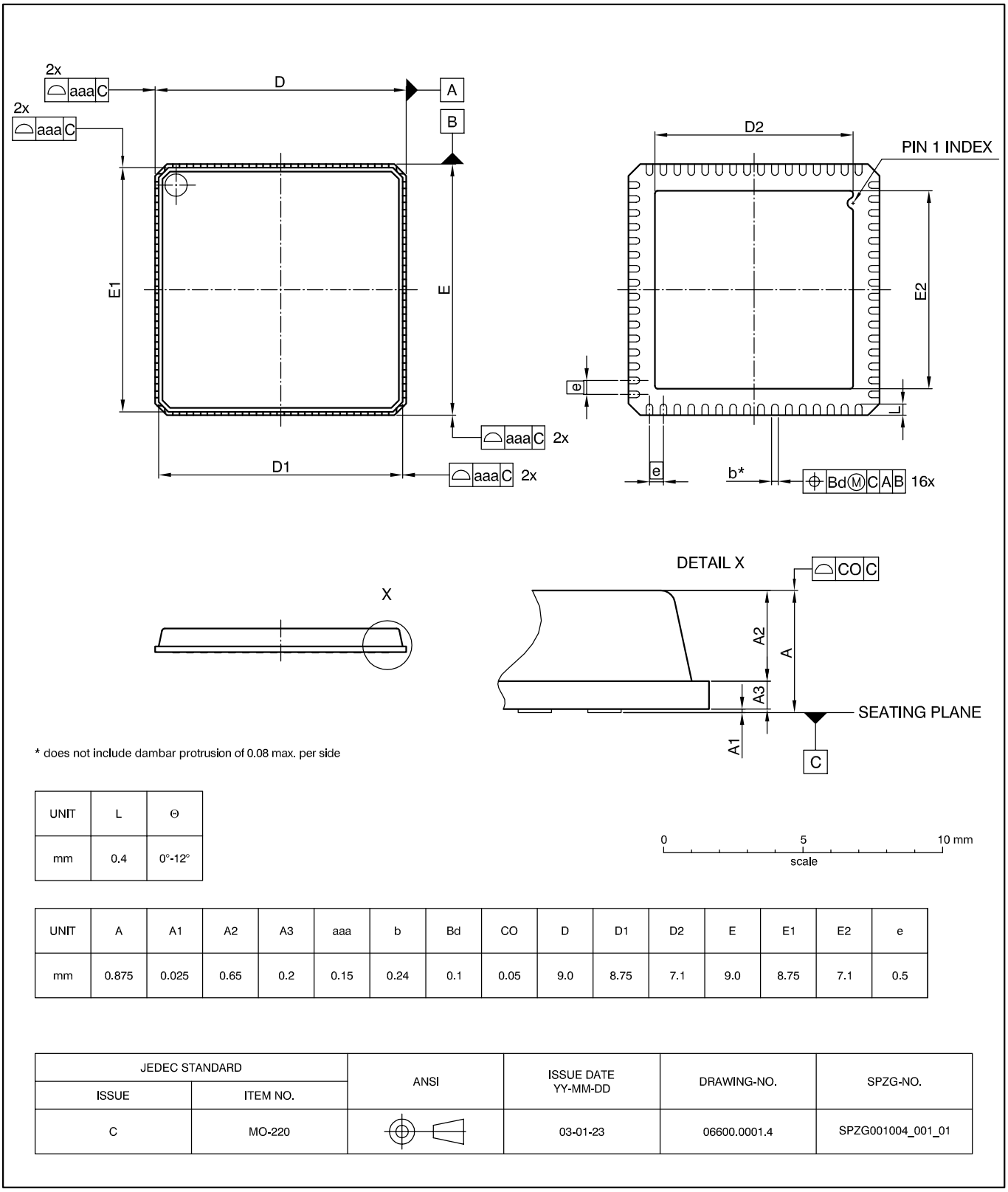
UNIT	L2	Θ
mm	1.60	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	max 2.45	0.25 0.00	2.20 1.80	0.25	0.27 0.17	0.2	0.23 0.11	0.1	13.2	10.0	13.2	10.0	0.5	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-03-25	06611.0001.4	SPZG001011_001_01

Fig. 5–1:
Plastic Metric Quad Flat Package, 64 leads, $10 \times 10 \times 2$ mm^3
(PMQFP64-2)
Weight approximately 0.5 g



* does not include dambar protrusion of 0.08 max. per side

UNIT	L	Θ
mm	0.4	0°-12°

UNIT	A	A1	A2	A3	aaa	b	Bd	CO	D	D1	D2	E	E1	E2	e
mm	0.875	0.025	0.65	0.2	0.15	0.24	0.1	0.05	9.0	8.75	7.1	9.0	8.75	7.1	0.5

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
C	MO-220		03-01-23	06600.0001.4	SPZG001004_001_01

Fig. 5–2:
Plastic Quad Flat Non-leaded package, 64 pins, $9 \times 9 \times 0.85$ mm^3, 0.5 mm pitch
(PQFN64-1)
Weight approximately 0.23 g

5.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant
VSS = if not used, connect to VSS
OBL = obligatory; connect as described in circuit diagram
VDD = connect to VDD

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
1	NC		LV	Not Connected
2	XTI	IN	OBL	Quartz Oscillator Pin 1
3	XTO	OUT	OBL	Quartz Oscillator Pin 2
4	AREG1	OUT/IN	OBL	Regulator Output for analog parts except amplifiers (supply voltage input for 5 V mode)
5	AVSS1	IN	OBL	VSS 1 for analog parts except amplifiers
6	AVSS0	IN	OBL	VSS 0 for audio output amplifiers
7	OUTL	OUT	LV	Audio Output: headphone / speaker Left
8	OUTR	OUT	LV	Audio Output: headphone / speaker Right
9	AREG0	OUT	OBL	Regulator Output for audio output amplifiers (supply voltage input for 5 V mode)
10	AVDD	IN	OBL	analog VDD
11	RD[1)]	OUT	LV	GPIO Read
12	STRB[1)]	OUT	LV	GPIO Strobe
13	DAI	IN	VSS	I^2S Data Input
14	WSI[1)]	IN/OUT	LV	I^2S Word Strobe
15	CLI[1)]	IN/OUT	LV	I^2S Bit Clock
16	DAO[1)]	OUT	LV	I^2S Data Output
17	ADR3/GPIO 11/ PWM[1)]	IN/OUT	LV	HID IO 11
18	ADR2/GPIO 10[1)]	IN/OUT	LV	HID IO 10
19	ADR1/GPIO 9[1)]	IN/OUT	LV	HID IO 9
20	ADR0/GPIO 8[1)]	IN/OUT	LV	HID IO 8
21	GPIO 7[1)]	IN/OUT	LV	HID IO 7
22	GPIO 6[1)]	IN/OUT	LV	HID IO 6
23	GPIO 5[1)]	IN/OUT	LV	HID IO 5
24	GPIO 4[1)]	IN/OUT	LV	HID IO 4
25	GPIO 3[1)]	IN/OUT	LV	HID IO 3
26	GPIO 2[1)]	IN/OUT	LV	HID IO 2

[1)] Switchable driver (weak/strong)

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
27	GPIO 1[1)]	IN/OUT	LV	HID IO 1
28	GPIO 0[1)]	IN/OUT	LV	HID IO 0
29	SDA[1)]	IN/OUT	LV	I^2C Data
30	SCL[1)]	IN/OUT	LV	I^2C Clock
31	TRDY	OUT	LV	Test Output Pin
32	VBUS	IN	OBL[2)]	Sense USB Bus
33	NC		LV	Not Connected
34	NC		LV	Not Connected
35	VREG	OUT	OBL	Capacitor for internal supply
36	DMINUS	IN/OUT	OBL[2)]	USB DATA MINUS
37	DPLUS	IN/OUT	OBL[2)]	USB DATA PLUS
38	VSS	IN	OBL	Digital VSS
39	VDD	IN	OBL	Digital VDD
40	MCLK[1)]	OUT	LV	I^2S Master Clock (384 x 48 kHz)
41	USBCLK[1)]	IN/OUT	LV	Direct ISO-Endpoint Output Clock
42	USBWSO[1)]	IN/OUT	LV	Direct ISO-Endpoint Output Word Strobe
43	USBDAT[1)]	IN/OUT	LV	Direct ISO-Endpoint Output Data
44	TEST	IN	VSS	Test Enable
45	$\overline{\text{RES}}$	IN	VDD	Power On Reset, active low
46	$\overline{\text{SUSPEND}}$	OUT	LV	Low-Power Mode Indicator
47	SOF	OUT	LV	1 ms Start-Of-Frame Signal
48	SEN	IN	VSS	Suspend Enable
49	NC		LV	Not Connected
50	FOUTL	OUT	OBL	Output to left external filter
51	FOPL	IN/OUT	OBL	Filter Op Amp Inverting Input, left
52	FINL	IN/OUT	OBL	Input for FiltoutL
53	FOUTR	OUT	OBL	Output to right filter op amp
54	FOPR	IN/OUT	OBL	Right Filter op amp inverting input
55	FINR	IN/OUT	OBL	Input for FILTOUTR
56	OUTS	OUT	LV	Analog Output Subwoofer

[1)] Switchable driver (weak/strong)
[2)] For non-USB codec applications leave D+/– vacant and connect VBUS pin to V_{DD}

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
57	FOPS	OUT	OBL	Output to Subwoofer external filter
58	NC		LV	Not Connected
59	ADCR	IN	LV	Line Input Right
60	ADCL	IN	LV	Line Input Left
61	MICBIAS	OUT	LV	Supply Voltage for Microphone
62	MICIN	IN	LV	Microphone Input
63	SGND	IN	OBL	Signal Reference Ground
64	SREF	IN/OUT	OBL	Signal Reference voltage

5.3. Pin Descriptions

5.3.1. Power Supply Pins

The UAC 355xB combines various analog and digital functions which may be used in different modes. For optimized performance, major parts have their own power supply pins. All VSS power supply pins must be connected.

VDD (39)
VSS (38)
The VDD and VSS power supply pair are connected internally with all digital parts of the UAC 355xB.

AVDD (10)
AVDD is the supply pin for the voltage regulators at AREG0 (9) and AREG1 (4).

AVSS0 (6)
AVSS0 is the ground connection for the headphone/ loudspeaker amplifier.

AVSS1 (5)
AVSS1 is the ground connection for the analog audio processing parts, except the headphone/loudspeaker amplifiers.

SREF (64)
Reference for analog audio signals. This pin is used as reference for the internal op amps. This pin must be blocked against SGND with a 3.3 µF capacitor.

Note: The pin has a typical DC level of 1.725 V. It can be used as reference input for external op amps when no current load is applied.

SGND (63)
Reference ground for the internal band-gap and biasing circuits. **This pin should be connected to a clean ground potential!** Any external distortions on this pin will affect the analog performance of the UAC 355xB.

AREG0 (9)
Voltage regulator output for headphone/loudspeaker amplifiers supply. Connect an external ceramic capacitor to stabilize the regulator output.

AREG1 (4)
Voltage regulator output for analog audio processing parts supply, except the headphone/loudspeaker amplifiers. Connect an external ceramic capacitor to stabilize the regulator output.

5.3.2. Analog Audio Pins

FOUTL (50)
FOPL (51)
FINL (52)
FOUTR (53)
FOPR (54)
FINR (55)
FOPS (57)
Filter op amps are provided in the analog baseband signal paths. These inverting op amps are freely accessible for external use by these pins.

The FOUTL/R pins are connected with the buffered output of the internal switch matrix. The FOPL/R pins are directly connected with the inputs of the inverting filter op amps. The FINL/R pins are connected to the outputs of the op amps.

ADCL (60)
ADCR (59)
Line Input pins.

MICIN (62)
MICBIAS (61)
Microphone input pin and microphone power supply pin.

OUTL (7)
OUTR (8)
OUTS (56)
These pins are connected to the internal output amplifiers. OUTL/R can be used for either line-out or stereo headphones. OUTS is the subwoofer output of line-out type.

Caution: A short-circuit at these pins for more than a momentary period may result in destruction of the internal circuits.

5.3.3. Interface Pins

DMINUS (36)
DPLUS (37)
Differential USB port pins. The DPLUS pin has an internal switchable pull-up resistor. Both pins must be connected to the USB bus via a series resistor.

VBUS (32)
Sense USB Bus.

USBCLK (41)
Direct ISO Endpoint Output Clock.

USBWSO (42)
Direct ISO Endpoint Word Strobe.

USBDAT (43)
Direct ISO Endpoint Output Data.

CLI (15)
Clock line for the I^2S bus. In master mode, this line is driven by the UAC 355xB; in slave mode, an external I^2S clock has to be supplied.

DAO (16)
Output of digital serial sound data of the UAC 355xB on the I^2S bus.

DAI (13)
Input of digital serial sound data to the UAC 355xB via I^2S bus.

WSI (14)
Word strobe line for the I^2S bus. In master mode, this line is driven by the UAC 355xB; in slave mode, an external I^2S word strobe has to be supplied.

MCLK (40)
I^2S master clock pin.

SCA (29)
Via this pin, the I^2C bus data is written to or read from the UAC 355xB.

SCL(30)
Via this pin, the I^2C bus clock signal has to be supplied.

5.3.4. Other Pins

XTI (2)
XTO (3)
The XTI pin is connected to the input of the internal crystal oscillator; the XTO pin to its output. Both pins should be directly connected to the crystal and two ground-connected capacitors (see application diagram).

Note: Do not drive external clock circuits via XTI/XTO.

SEN (48)
Digital input that prevents the device from entering the low-power mode. This pin is also used to signal remote wake-up.

TEST (44)
Test enable. This pin is for test purposes only and must always be connected to VSS.

VREG (35)
Voltage regulator output for USB transceiver supply. Connect an external ceramic capacitor to stabilize the regulator output.

$\overline{\text{RES}}$ (45)
A Low signal at this pin resets the chip.

GPIO 0…ADR/GPIO 11/PWM
(28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17)
These pins are configurable to be either input or output and can be used to connect audio function keys or signalling LEDs.

RD (11)
GPIO read pin.

STRB (12)
GPIO strobe pin.

$\overline{\text{SUSPEND}}$ (46)
This pin indicates that the host PC sets the USB bus to the suspend mode state.

SOF(47)
Start of Frame Signal. 1 ms signal that can be used for external application circuits.

TRDY (31)
Test Output Pin. This pin is intended for test purposes only and must not be connected.

5.4. Pin Configuration

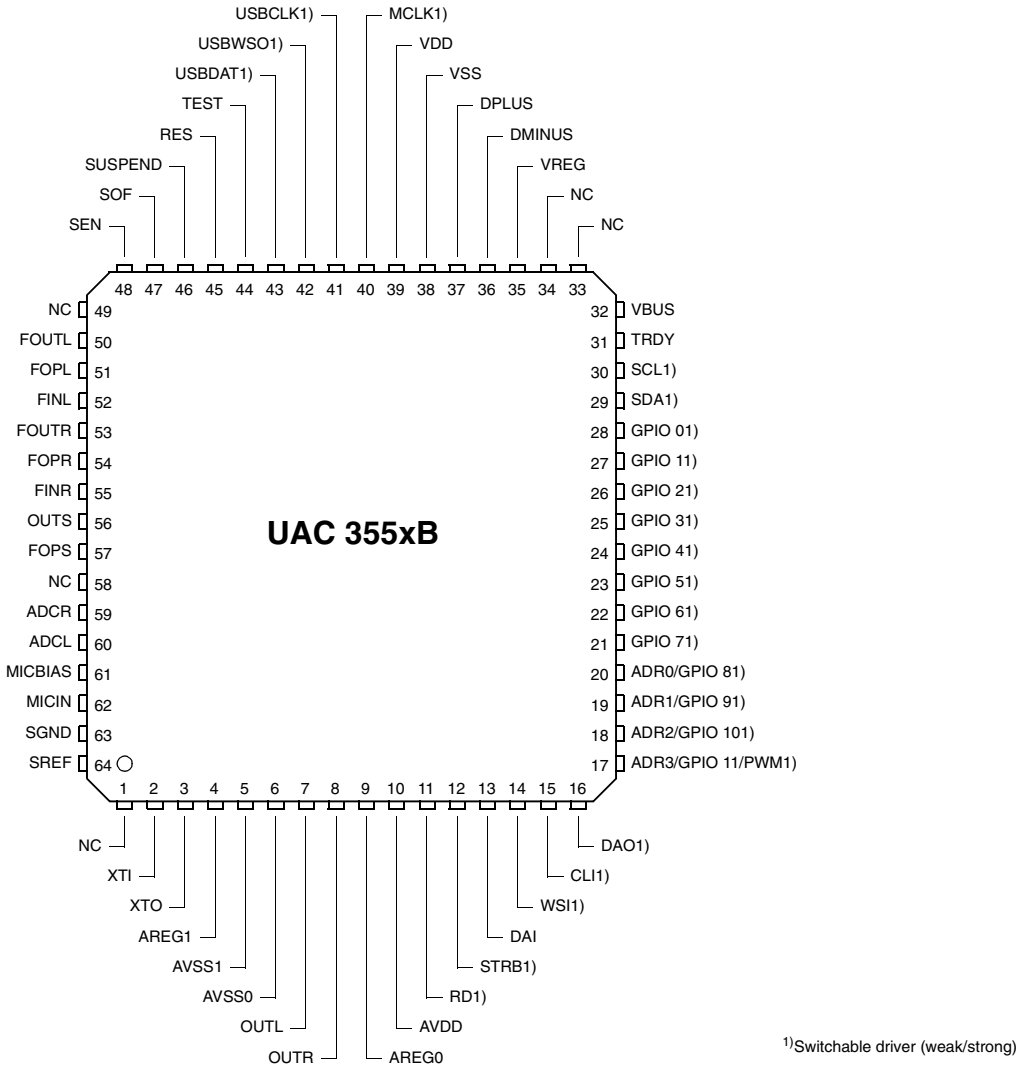


Fig. 5–1: PMQFP64 and PQFN64 package

5.5. Pin Circuits

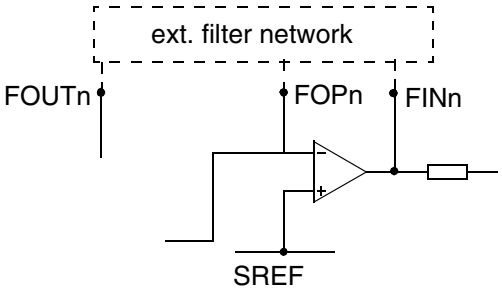


Fig. 5–1: Pins FINR, FOPR, FINL, FOPL

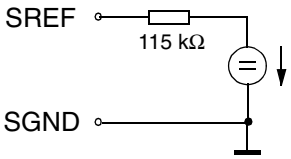


Fig. 5–2: Pins SREF, SGND

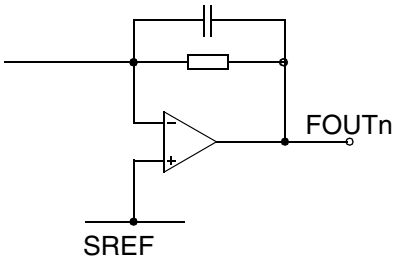


Fig. 5–3: Output Pins FOUTL, FOUTR

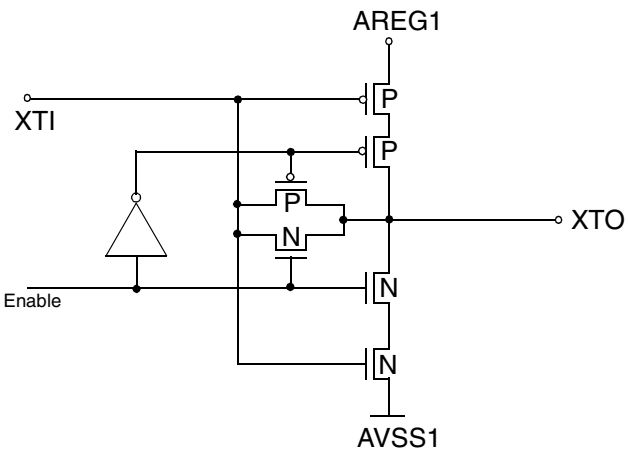


Fig. 5–4: Clock oscillator XTI, XTO

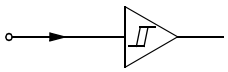


Fig. 5–5: Input Pins $\overline{\text{RES}}$, TEST, SEN, DAI

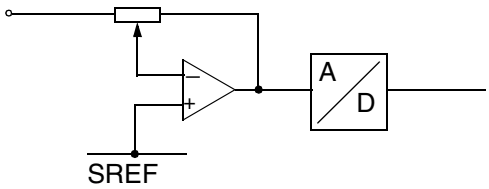


Fig. 5–6: Analog input pins MIC, MICBIAS, ADCL, ADCR

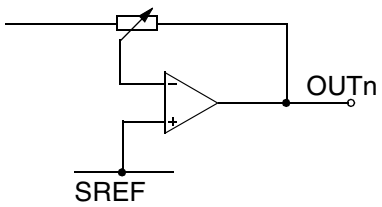


Fig. 5–7: Output Pins OUTL, OUTR

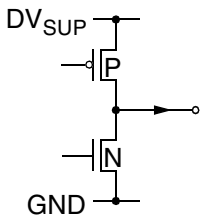


Fig. 5–8: Digital Output Pins SOF, $\overline{\text{SUSPEND}}$, TRDY

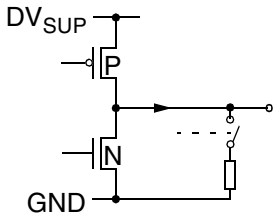


Fig. 5–9: Digital Output Pins MCLK, RD, STRB, DAO

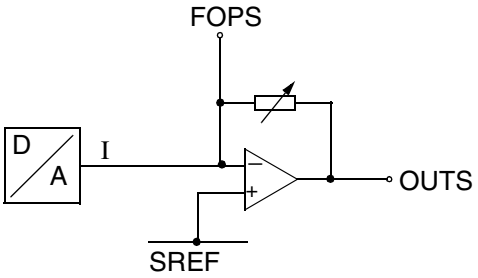


Fig. 5–10: Subwoofer Output Pin OUTS and Output to Subwoofer External Filter FOPS

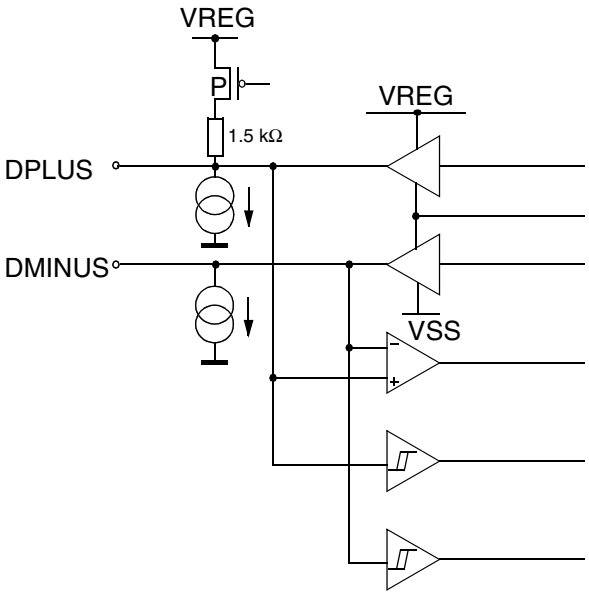


Fig. 5–11: Digital Input/Output Pins DMINUS, DPLUS, VREG

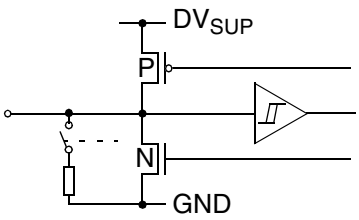


Fig. 5–12: Input/Output Pins GPIO0...GPIO11, WSI, CLI, USBCLK, USBWSO, USBDAT

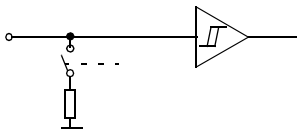


Fig. 5–13: Input Pin VBUS

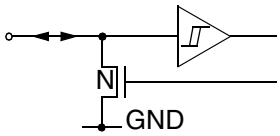


Fig. 5–14: Input/Output Pins SDA, SCL

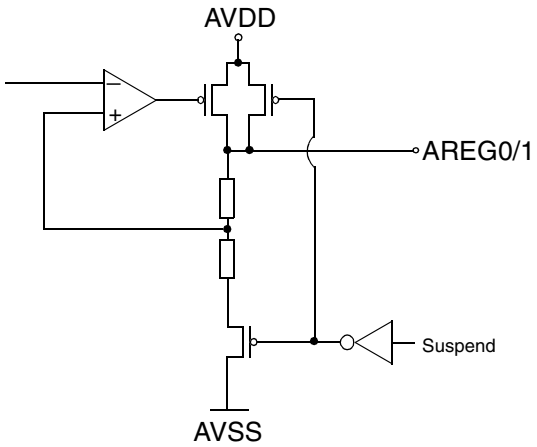


Fig. 5–15: Analog Voltage Supply Pins AVDD, AVSS, AREG0/1

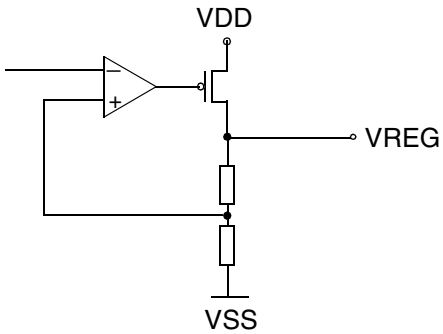


Fig. 5–16: Digital Voltage Supply Pins VDD, VSS, VREG

5.6. Electrical Characteristics

5.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		0	70	°C
T_{C1}	Case Operating Temperature for PQFN64-1 package		–	95	°C
T_{C2}	Case Operating Temperature for PMQFP64-2 package		–	105	°C
T_S	Storage Temperature		–40	125	°C
P_{TOT}	Power Dissipation			650	mW
V_{SUPA}	Analog Supply Voltage[1)]	AVDD	–0.3	6	V
V_{SUPA}	Analog Supply Voltage[2)]	AVDD, AREG0/1	–0.3	6	V
V_{SUPD}	Digital Supply Voltage	VDD	–0.3	6	V
ΔV_{GRND}	Voltage Differences between different Grounds	AVSS0, AVSS1, VSS	–0.5	+0.5	V
V_{Idig}	Input Voltage, all digital inputs		–0.3	V_{SUPD} + 0.3	V
I_{Idig}	Input Current, all digital inputs[4)]		–20	+20	mA
I_{Odig}	Output Current, all digital outputs		–50	+50	mA
V_{Iana}	Input Voltage, all analog inputs		–0.3	$V_{VAREG0/1}$+ 0.3	V
I_{Iana}	Input Current, all analog inputs[4)]		–5	+5	mA
I_{Oaudio}	Output Current, audio output[3)4)]	OUTL/R	–0.2	0.2	A
I_{AREG0}	Output Current, analog regulator[4)]	AREG0	–500	+20	mA
I_{AREG1}	Output Current, analog regulator[4)]	AREG1	–50	+20	mA

[1)] Internal regulators used
[2)] If internal regulators are not used, connect AVDD to AREG0/1.
[3)] These pins are **not** short-circuit proof!
[4)] Positive value means current flowing into the circuit

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

5.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Temperature Ranges and Supply Voltages						
T_A	Ambient Temperature Range		0		70	°C
V_{SUPA}	Analog Audio Supply Voltage	AVDD	4.1	5.0	5.6	V
C_{SUPA}	Capacitor at analog supply pins to ground	AVDD		220		nF
V_{SUPD}	Digital Supply Voltage	VDD	4.1	5.0	5.6	V
C_{SUPD}	Capacitor at digital supply pin to ground	VDD		100		nF
C_{SUPUSB}	Capacitor at VBUS pin to ground	VBUS		22		nF
Analog Reference						
C_{SREF1}	Analog Reference Capacitor	SREF	1	3.3		µF
C_{SREF2}	Ceramic Capacitor in parallel	SREF		100		nF
Analog Audio Inputs						
C_{inAD}	DC-Decoupling Capacitor at A/D converter inputs	ADCL/R		390		nF
C_{inMI}	DC-Decoupling Capacitor at microphone input	MICIN		100		nF
Analog Audio Filter Inputs and Outputs						
Z_{AFLO}	Analog Filter Load Output[1)]	FOUTL/R	7.5		6	kΩ pF
Z_{AFLI}	Analog Filter Load Input[1)]	FINL/R	5.0		7.5	kΩ pF
$C_{FILTSUBW}$	Filter Capacitor for Subwoofer output	FOPS		2.2		nF
Analog Audio Outputs						
Z_{AOL_HP}	Output Load Headphone (16 Ω series resistor required)	OUTL/R	16	32 100		Ω pF
$Z_{AOLSUBW}$, Z_{Line_out}	Output Load Subwoofer (if the max. capacitive load is exceeded, a decoupling resistor of 220 Ω is mandatory) DC-decoupling capacitor at sub-woofer output	OUTS, FINL/R	10	 470	15	kΩ pF nF
[1)] Please refer to Section 6. “UAC 3556/3554B Applications” on page 46						

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Crystal Characteristics[1]						
T_{AC}	Ambient Temperature Range		0		70	°C
F_P	Load Resonance Frequency at C_{load} = 22 pF[2]	XTI		12		MHz
V_{ACLK}	Clock Amplitude	XTI, XTO	0.5		V_{REG1} –0.5	V_{PP}
$\Delta F/F_s$	Accuracy of Adjustment		–500		500	ppm
$\Delta F/F_s$	Frequency Variation versus Temperature		–500		500	ppm
R_{EQ}	Equivalent Series Resistance			12	30	Ω
C_0	Shunt (parallel) Capacitance			3	5	pF
Voltage Regulator						
C_{VREG}	Voltage Regulator Capacitor (ceramic, X5R)	VREG	330	1000		nF
C_{AREG0}	Voltage Regulator Capacitor (ceramic, X5R)	AREG0	330	470	600	nF
C_{AREG1}	Voltage Regulator Capacitor (ceramic, X5R)	AREG1	150	220	270	nF
Transceiver						
R_{USB}	Input Series Resistance	DPLUS/ DMINUS		24 (±5%)		Ω

[1] For device characteristics please refer to page 40
[2] C_{load} should typically be 22 pF (+30% / –10%), e.g., Y5U. Refer to application circuit (see Fig. 6–3 on page 50).

5.6.3. Characteristics

At T_A = 0 °C to 70 °C, V_{SUPD} = 4.1 V to 5.6 V, V_{SUPA} = 4.1 V to 5.6 V. Typical values at T_A = 20 °C, $V_{SUPD} = V_{SUPA}$ = 5.0 V, quartz frequency = 12 MHz, duty cycle = 50%, bass/treble: 0 dB, **M**icronas **D**ynamic **B**ass: off, AGC: off, equalizer: off (positive current flowing into the IC), 3 V Mode, reduced feature set, if not otherwise specified.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Supply							
I_{VDD}	Current Consumption[1]	VDD		57 45	70	mA	72 MHz APU clock 48 MHz APU clock
				30	80	µA	Suspend
Digital Input Pin							
I_I	Input Leakage Current	GPIO[11:0], SEN, RES, VBUS, DAI, WSI, CLI			±1	µA	$V_{GND} \le V_I \le V_{SUP}$
V_{IL}	Input Low Voltage				0.4	V	
V_{IH}	Input High Voltage		V_{SUPD} −0.4V			V	
Digital Output Pin							
V_{OH}	Output High Voltage	GPIO[11:0] SUSPEND, SOF, RD, STRB, WSI, CLI, DAO, SDA, SCL,MCLK	V_{SUPD} − 0.4			V	Pins set to output I_{out}=8 mA
V_{OL}	Output Low Voltage				0.4	V	
I_{O_max}	Max. Output Current				1[3] 8[2)3]	mA	output set to “weak” output set to “strong”
Analog Supply							
I_{AVDD}	Current Consumption Analog Audio	AVDD		12	15	mA	all analog blocks on, Mute
				120	135	µA	Suspend
				25		mA	$R_L \ge 32\ \Omega$ (external 16 Ω series resistor required) Volume = 0 dB, Input signal 1kHz at 0 dB_{FS}
$PSRR_{AA}$	Power Supply Rejection Ratio for Analog Audio Outputs (internal regulators active)	AVDD,[4] OUTL/R/S		95		dB	1 kHz sine wave at 100 mV_{rms}
				55		dB	≤ 100 kHz sine wave at 100 mV_{rms}

[1] no load attached to GPIOs.
[2] max. output current for driving LEDs is 20 mA.
[3] the sum of these digital output pin currents must not exceed 100 mA. Higher currents might damage the device.
[4] not tested in production.

Please consider power limitations due to USB specification.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Microphone Bias							
$V_{MICBIAS}$	Open Circuit Voltage Microphone Bias	MICBIAS	2.9	3.0	3.1	V	
$I_{MICBIAS}$	Output Current Microphone Bias	MICBIAS			0.5	mA	
$R_{OUTMICB}$	Output Resistance Microphone Bias	MICBIAS	100	180	210	Ω	
$PSRR_{MICB}$	Power Supply Rejection Ratio for Microphone Bias	AVDD,[4] MICBIAS		100		dB	internal regulators active, at maximum load current (0.5 mA), 1 kHz sine wave at 100 mV_{rms}
Analog Supply Voltage Regulators							
V_{AREG}	Output Voltage	AREG0/1, AVSS0/1	3.3	3.5	3.7	V	
Reference Frequency Generation							
V_{DCXTI}	DC Voltage at Oscillator Pins	XTI/O		0.5* V_{Areg1}		V	
C_{LI}	Input Capacitance at Oscillator Pin	XTI		3		pF	
C_{LO}	Input Capacitance at Oscillator Pin	XTO		3		pF	
$V_{XTALOUT}$	Voltage Swing at Oscillator Pins (peak-peak)	XTI/O	0.6 * V_{Areg1}		1.0 * V_{Areg1}	V	
T_{OSC_rise}	Oscillator Start-Up Time				10	ms	after min. V_{SUPA} is reached
USB Transceiver							
V_{REG}	Regulator Voltage	VREG	3.25	3.4	3.55	V	C_L=1 µF
R_O	Driver Output Resistance including the 24 Ω external serial resistor	D+/D–	28		43	Ω	static, LOW or HIGH
t_r / t_f	Rise and Fall Times	D+/D–	4		20	ns	C_L=50 pF, driver mode
MA_TRTF	Rise/Fall Time Matching	D+/D–	90		110	%	C_L=50 pF, driver mode
V_{XOVER}	Crossover Voltage	D+/D–	1.3	1.65	2.0	V	C_L=50 pF, driver mode
V_{CM_DREC}	Differential Receiver Common-Mode Range	D+/D–	0.8		2.5	V	
V_{T_SREC}	Single-ended Receiver Threshold Voltage	D+/D–	0.8		2.0	V	
R_{pu}	Switchable Pull-up Resistor	VREG, D+		1.5		kΩ	USB connected

[4] not tested in production

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Audio							
V_{SREF}	Signal Reference Voltage	SREF	1.6	1.725	1.8	V	R_L >> 10 MΩ, referred to SGND
V_{AI}	Analog Line Input Clipping Level (at input volume 0 dB)	ADCL/R		2.4		V_{pp}	
V_{MI}	Microphone Input Clipping Level (at minimum input volume, i.e., 0 dB)	MICIN		283		mV_{pp}	
V_{AO}	Analog Output Voltage AC	OUTL/R		2.4		V_{pp}	BW = 20 Hz...22 kHz, $R_L \geq 10k\Omega$, volume = 0 dB, Input 1 kHz at 0 dB_{FS} digital (I^2S)
V_{AOS}	Analog Output Voltage AC	OUTS		2.35		V_{pp}	BW = 20 Hz...22 kHz, $R_L \geq 10$ kΩ, volume = 0 dB, Input 100 Hz at 0 dB_{FS} digital (I^2S),
R_{inAI}	Analog Line Input Resistance	ADCL/R	60	85	120	kΩ	at minimum input volume, i.e., –3 dB
			10	14	20		at maximum input volume, i.e., +19.5 dB
R_{inMI}	Microphone input resistance	MICIN	98	137	200	kΩ	at minimum input volume, i.e., 0 dB
			8	11	16		at maximum input volume, i.e., +22.5 dB
R_{inAO}	Analog output resistance[4]	OUTL/R		3	6	Ω	volume=0 dB
R_{inSO}	Analog output resistance subwoofer[4]	OUTS		3		Ω	volume=0 dB
SNR_{AI}	Signal-to-noise ratio of line input[2]	ADCL/R	88	92		dB(A)	BW = 20 Hz...22 kHz, A-weighted, Input 1 kHz at V_{AI}–20 dB, volume= 0 dB, digital output (I^2S)
SNR_{MI}	Signal-to-noise ratio of microphone input[3]	MICIN	80	85		dB(A)	BW = 20 Hz...22 kHz, A-weighted, Input 1 kHz at V_{MI}–20 dB, volume= 0 dB, digital output (I^2S)
THD_{AI}	Total harmonic distortion of analog inputs	ADCL/R MICIN		–94 –88	–90 –80	dB	BW = 20 Hz...22 kHz, volume = 0 dB, Input 1 kHz at –3 dB_{FS} = V_{AI}– 3 dB resp., V_{MI}–3 dB, digital output (I^2S)

[2] related to 0 dB_{FS} input level
[3] applying a signal of 280 mV_{pp} at the Microphone input delivers a 0 dB_{FS} signal at the ADC output (volume=0 dB)
[4] not tested in production

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$XTALK_{AI}$	Crosstalk attenuation left/right channel for analog inputs	ADCR/L - ADCL/R, MICIN ADCL-MICIN		–95 –76	–85 –70	dB	BW = 20 Hz...22 kHz, volume = 0 dB, Input 1 kHz at –3 dB_{FS}, digital output (I^2S)
$PSRR_{A0}$	Power Supply Rejection Ratio	AVDD, OUTL/R		88[4]		dB	1 kHz sine wave at 100 mV_{rms}
		AVDD, OUTL/R		54[4]		dB	≤ 100 kHz sine wave at 100 mV_{rms}
$PSRR_{AI}$	Power supply rejection ratio for analog audio inputs	AVDD, ADCL/R MICIN		80[4]		dB	1 kHz sine at 100 mV_{rms}, 3 V Mode, digital output (I^2S)
				66[4]		dB	≤ 10 kHz sine at 100 mV_{rms}, 3 V Mode, digital output (I^2S)
$R_{D/A}$	D/A Pass Band Ripple	OUTL/R		0.1[4]		dB	0...20 kHz (with 2nd-order post filter)
$A_{D/A}$	D/A Stop Band Attenuation			40[4]		dB	31 kHz...164 kHz (with 2nd-order post filter)
THD_{HP}	Total Harmonic Distortion	OUTL/R		–90	–85	dB	BW = 20 Hz...22 kHz, R_L ≥10 kΩ, Volume = 0 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
THD_{HP}	Total Harmonic Distortion	OUTL/R		–70		dB	BW = 20 Hz...22 kHz, unweighted, R_L ≥ 32 Ω, Volume = 0 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
THD_{SUBW}	Total Harmonic Distortion	OUTS		–80	–72	dB	BW = 20 Hz...22 kHz, R_L ≥10 kΩ, Volume = 0 dB, Corner Frequency set to 400Hz, Input 100 Hz at –3 dB_{FS} digital (I^2S)
SNR_{AO1}	Signal-to-Noise Ratio[2]	OUTL/R	90	97		dB (A)	BW = 20 Hz...22 kHz, A-weighted, R_L ≥10 kΩ, Volume = 0 dB, Input 1 kHz at – 20 dB_{FS} digital (I^2S)
SNR_{AO2}	Signal-to-Noise Ratio[2]	OUTL/R	95	102		dB (A)	BW = 20 Hz...22 kHz, A-weighted, R_L ≥10 kΩ, Volume = –40 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)

[2] related to 0 dB_{FS} input level
[3] applying a signal of 100 mV_{rms} at the Microphone input delivers a 0 dBFS signal at the ADC output (volume=0 dB)
[4] not tested in production

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Lev_{Mute}	Mute Level L/R	OUTL/R		–110		dB	BW = 20 Hz...22 kHz unweighted, no digital input signal, Volume = Mute
$G_{INL/R}$	Gain from ADC Inputs to Outputs	ADCL/R, OUTL/R	–0.5	0	0.5	dB	$R_L \geq 10$ kΩ, Volume = 0 dB; I nput = –3 dB_{FS} =V_{AI}–3 dB
P_{HP}	Output Power (Speaker/Headphone)[4]	OUTL/R		10		mW_{eff}	R_L = 32 Ω, 16Ω series resistance, Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
P_{HP}	Output Power in Bridge Mode (Mono Speaker/ Headphone)[4]	OUTL/R		180		mW_{eff}	R_L = 16 Ω, no series resistors, right channel inverted and output set to mono (Bridge Mode) Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
VOL_{AO}	Output Volume Setting Range	OUTL/R	–90		0	dB	
$dVOL_{AO}$	Output Volume Step Size	OUTL/R		1		dB	
VOL_{GA}	Output Volume Error	OUTL/R	–0.5	0	0.5	dB	
VOL_{dGA}	Analog Output Volume Step Size Error	OUTL/R	–0.5	0	0.5	dB	
$XTALK_{HP}$	Crosstalk Left/Right Channel (Headphone)	OUTL/R		–95	–80	dB	R_L = 32 Ω, 3 V Mode, Volume = 0 dB, Input = –3 dB_{FS} digital (I^2S)
[2] related to 0 dB_{FS} input level [4] not tested in production							

Different Characteristics in Five-Volt Mode

$V_{MICBIAS}$	Open Circuit Voltage Microphone Bias	MICBIAS	3.9	4.0	4.1		
V_{SREF}	Signal Reference Voltage	SREF	2.25	2.3	2.35	V	R_L >> 10 MΩ, referred to SGND
V_{AI}	Analog Line Input Clipping Level (at input volume 0 dB)	ADCL/R		3.2		V_{pp}	
V_{MI}	Microphone Input Clipping Level (at minimum input volume, i.e., 0 dB)	MICIN		370		mV_{pp}	
V_{AO}	Analog Output Voltage AC	OUTL/R		3.2		V_{pp}	BW = 20 Hz...22 kHz, $R_L \geq$10 kΩ, volume = 0 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
V_{AOS}	Analog Output Voltage AC	OUTS		3.1		V_{pp}	BW = 20 Hz...22 kHz, $R_L \geq$10 kΩ, volume = 0 dB, Input 100 Hz at 0 dB_{FS} digital (I^2S)

THD_{HP}	Total Harmonic Distortion	OUTL/R		–93	–85	dB	BW = 20 Hz...22 kHz, $R_L \geq 10k\Omega$, Volume = 0 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
SNR_{AO1}	Signal-to-Noise Ratio[2)]	OUTL/R	90	99		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10k\Omega$, Volume = 0 dB, Input 1 kHz at – 20 dB_{FS} digital (I^2S)
SNR_{AO2}	Signal-to-Noise Ratio[2)]	OUTL/R	95	109		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10k\Omega$, Volume = –40 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
P_{HP}	Output Power (Speaker/Headphone)	OUTL/R		17		mW_{eff}	R_L = 32 Ω, 16 Ω series resistance, Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
P_{HP}	Output Power in Bridge Mode (Mono Speaker/Headphone)	OUTL/R		320		mW_{eff}	R_L = 16 Ω, no series resistors, right channel inverted and output set to mono (bridge mode) Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
[2)] related to 0 dB_{FS} input level [4)] not tested in production							
Different Characteristics for Full-Feature Set (see Fig. 2–1 on page 6), Three-Volt Mode							
SNR_{AO1}	Signal-to-Noise Ratio[2)]	OUTL/R	88	95		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10k\Omega$, Volume = 0 dB, Input 1 kHz at – 20 dB_{FS} digital (I^2S)
SNR_{AO2}	Signal-to-Noise Ratio[2)]	OUTL/R	93	100		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10$ kΩ, Volume = –40 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
SNR_{AS1}	Signal-to-Noise Ratio[2)] Subwoofer	OUTS	75	85		dB	BW = 20 Hz...22 kHz, unweighted, $R_L \geq 10$ kΩ, Volume = 0 dB, Corner Frequency set to 400 Hz, Input 100 Hz at –20 dB_{FS} digital (I^2S)
SNR_{AS2}	Signal-to-Noise Ratio[2)] Subwoofer	OUTS		105		dB	BW = 20 Hz...22 kHz, unweighted,$R_L \geq 10k\Omega$, Volume = –40 dB, corner frequency set to 400 Hz, Input 100 Hz at –3 dB_{FS} digital (I^2S)
Lev_{Mute}	Mute Level Subwoofer	OUTS		–77		dB	BW = 20 Hz...400 Hz unweighted, no digital input signal, corner frequency set to 400 Hz, Volume = Mute

5.6.4. I^2S Interface Timing Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{s_I2S}	I^2S Input Setup Time before Rising Edge of Clock	CLI DAI USBCLK USBDAT	10			ns	
t_{h_I2S}	I^2S Input Hold Time after Rising Edge of Clock		40			ns	
t_{d_I2S}	I^2S Output Delay Time after Falling Edge of Clock	CLI WSI DAO USBCLK USBWSI USBDAT			30	ns	C_L=30 pF
t_{o_I2S}	I^2S Output Setup Time before Rising Edge of Clock	CLI DAO USBCLK USBDAT	4			ns	C_L=30 pF

The interfaces can be used in three different modes.

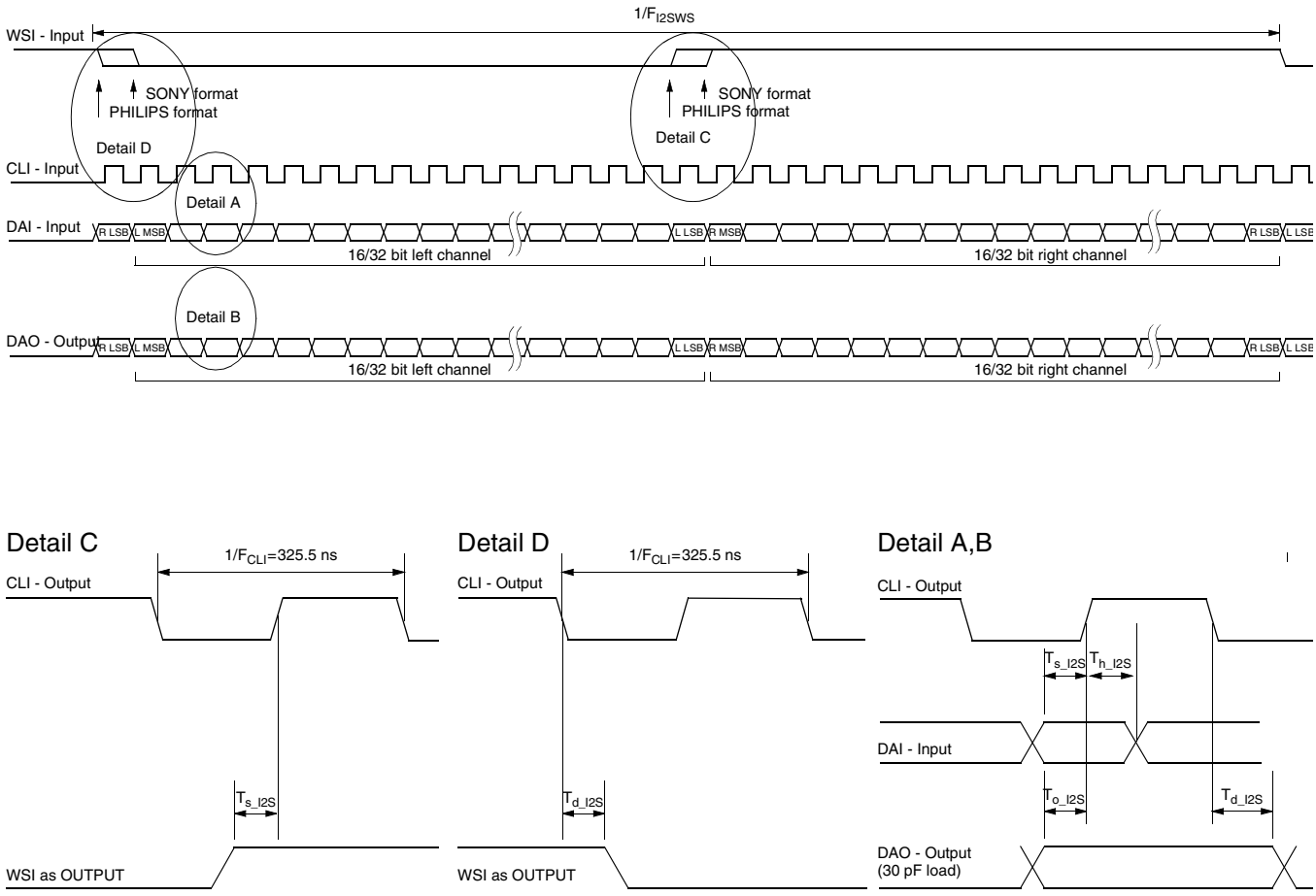


Fig. 5–1: Timing: synchronous I^2S input / output

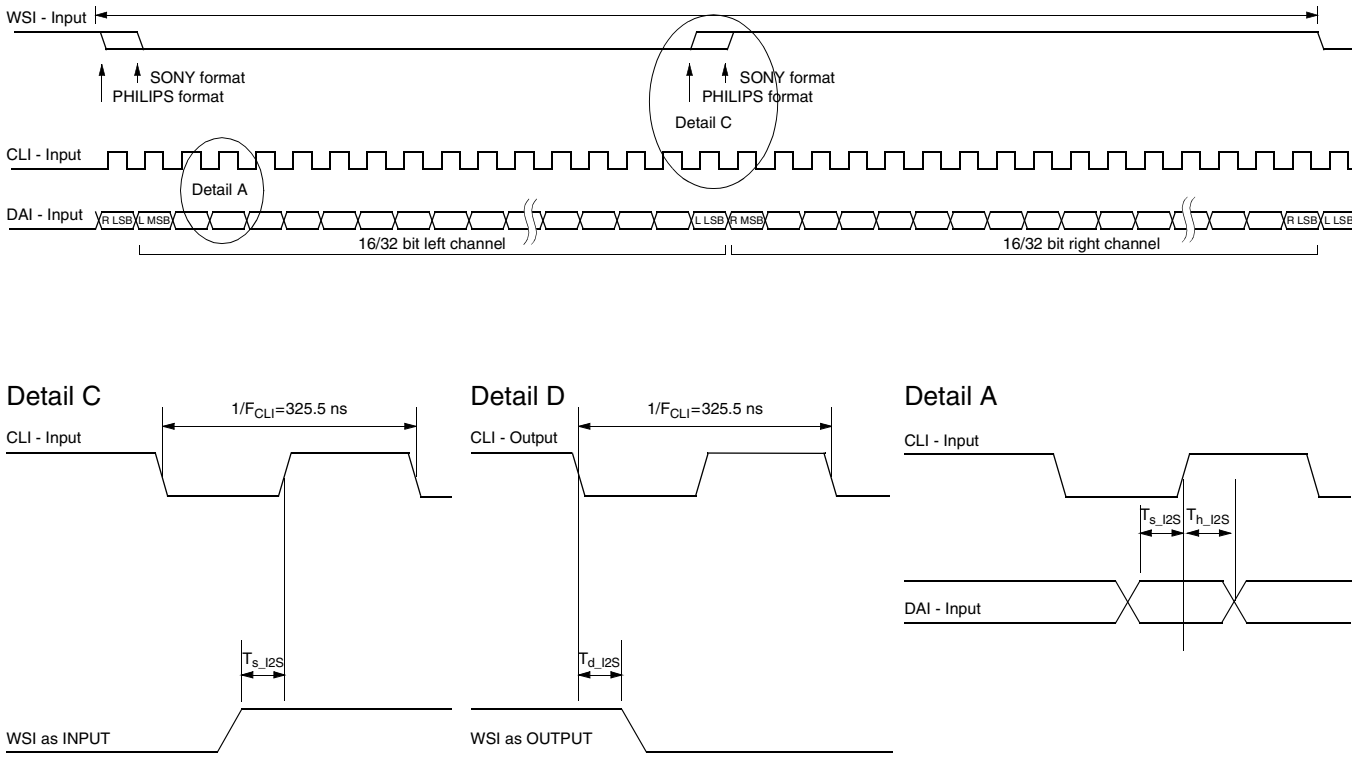


Fig. 5–2: Timing asynchronous I^2S input

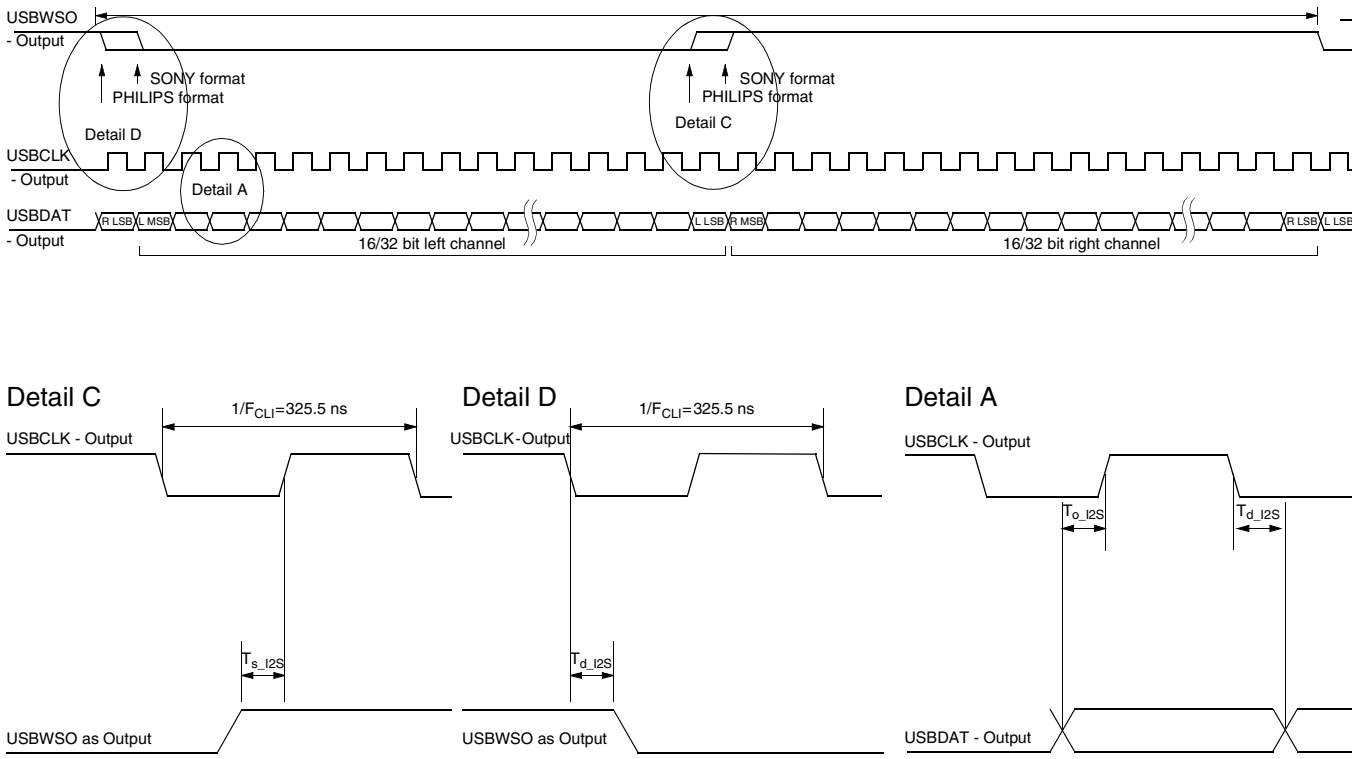


Fig. 5–3: Timing synchronous I^2S Output

6. UAC 355xB Applications

6.1. Recommended Low-Pass Filters for Analog Outputs

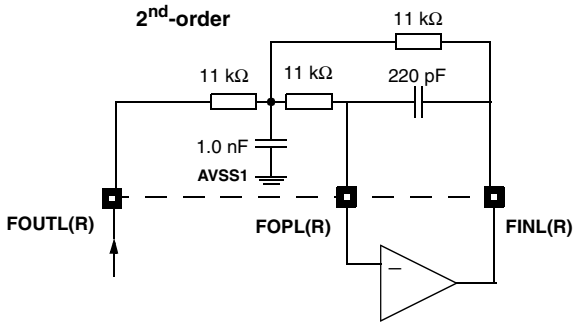


Fig. 6–1: 2nd-order low-pass filter

If the filter is not used, then FOUTL(R), FOPL(R), and FINL(R) are to be connected (dashed line) and the internal op-amp must be switched off.

Table 6–1: Attenuation of 2nd-order low-pass filter

Frequency	Gain
24 kHz	–1.5 dB
30 kHz	–3.0 dB

Note: First or third-order low-pass is also possible, but then the frequency response degrades.

6.2. External Clocking via XTI

AC-coupling of the clock signal

The input level should be in the range of 0.5 to 2.5 V_{PP}. for a load capacitance of 22 pF at XTO.

DC-coupling of the clock signal

The DC input level must be 0.5 × V_{AREG1} which is typically 1.75 V. The input level should not exceed 0.5 to 2.5 V_{PP}.

See also Section 2.12. on page 16.

6.3. Typical Applications

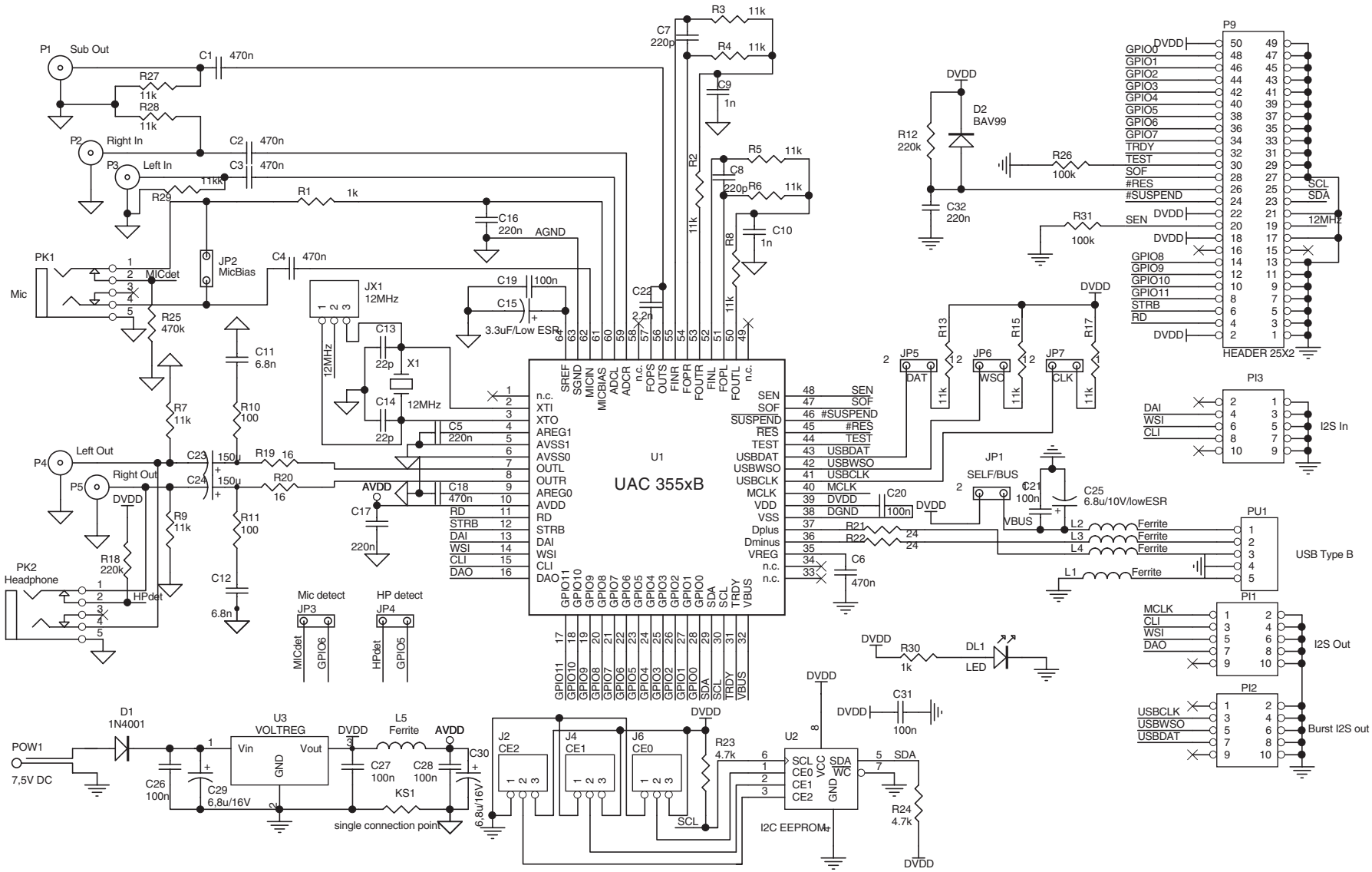


Fig. 6–2: Circuit for a typical codec application

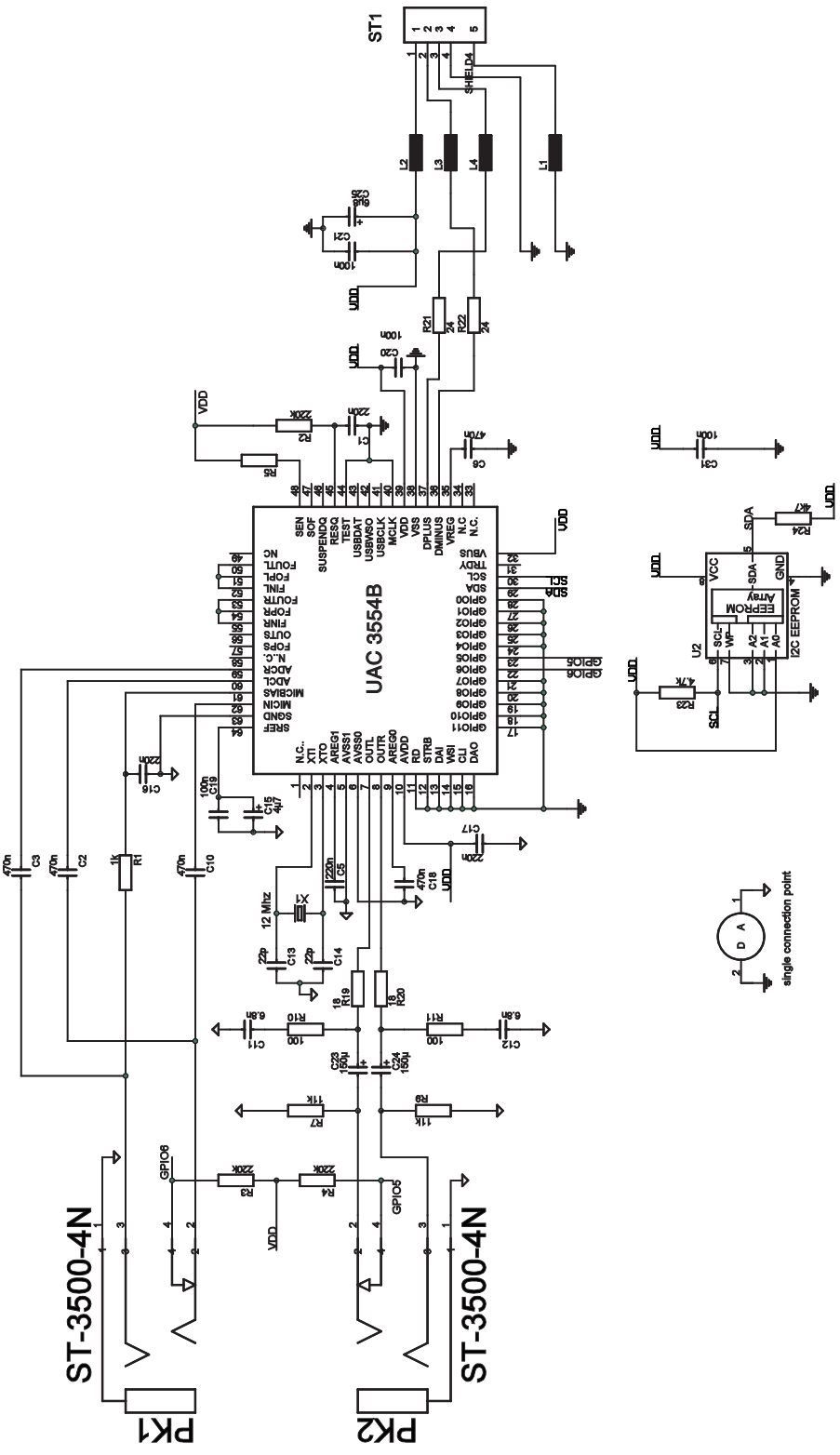


Fig. 6–3: Circuit for a headset application

7. Data Sheet History

1. Data Sheet: “UAC 355XB Universal Serial Bus (USB) Codecs”, April 15, 2003, 6251-544-1DS. First release of the data sheet.

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