National Semiconductor

μA212AT 1200/300 bps Full Duplex Modem

General Description

The μA212AT single-chip modem IC performs all signal processing functions required for a Bell 212A/103 compatible modem. Handshaking protocols, and mode control functions are provided by a general purpose single-chip μC. The μA212AT and μC, along with several components to handle the control and telephone line interfaces, provide a high performance, cost-effective solution for an intelligent Bell 212A-compatible modem design.

The modem chip performs the modulation, demodulation, filtering and certain control and self-test functions required for a Bell 212A-compatible modem, as well as additional functional enhancements. Switched capacitor filters provide channel isolation, spectral shaping and fixed compromise equalization for both high and low speed modes.

A novel switched-capacitor modulator and a digital coherent demodulator provide 1200 bps QPSK operation while a separate digital FSK modulator and demodulator handle the 0-300 bps requirement. The μA212AT includes an integral DTMF tone generator on-chip. The receive filter and energy detector may be configured for call progress tone detection (dialtone, busy, ringback, voice), providing the front end for a smart dialer.

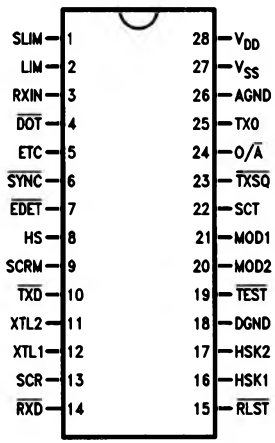
The μA212AT is fabricated in an advanced Double-Poly Silicon-Gate CMOS process.

Features

- Functions as a 212A and 103 compatible modem
- Performs all signal processing functions
- Interfaces to single chip μC which handles handshaking protocols and mode control functions
- DTMF tone generation
- Pin and firmware compatible with the μA212A (without integral DTMF) for easy upgrade
- Call progress tone detection for smart dialer applications
- On chip oscillator uses standard 3.6864 MHz crystal
- Few external components required
- Operates from +5V and −5V supplies
- Low operating power: 35 mW typical
- 28-lead ceramic DIP, 28-lead plastic DIP, and 28-lead surface mount packages
- μA212AT designer's kit is available

Connection Diagram

28-Lead DIP



TL/H/9430–1

Top View

28-Lead PLCC

(Pin numbers same as 28-lead DIP)

Order Number μA212ATDC, μA212ATQC
See NS Package Number N28B

***Molded Dual-In-Line Package**
Order Number μA212ATQC
See NS Package Number V28A

***Ceramic Dual-In-Line Package**
Order Number μA212ATDC
See NS Package Number F28B

*For most current package information contact product marketing.
For most current order information, contact you local sales office.

Absolute Maximum Ratings*

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{DD} to DGND or AGND	+7.0V
V_{SS} to DGND or AGND	−7.0V
Voltage at Any Input	V_{DD} +0.3V to V_{SS} −0.3V
Voltage at Any Digital Output	V_{DD} +0.3V to DGND −0.3V
Voltage at Any Analog Output	V_{DD} +0.3V to V_{SS} −0.3V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

*Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics unless otherwise noted: V_{DD} = 5.0V, V_{SS} = −5.0V, DGND = AGND = 0V, T_A = 25°C; all digital signals are referenced to DGND, all analog signals are referenced to AGND

ENERGY DETECTOR

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Data Mode					
V_{thon}	OFF/ON Threshold	Voltage Level at RXIN		6.5		mV_{rms}
V_{thoff}	ON/OFF Threshold	Pin In Data Mode		5.2		
t_{on}	Energy Detect Time	At $\overline{EDET}$ Pin	105	155	205	ms
t_{off}	Loss of Energy Detect Time		10	17	24	ms
	Dialer Mode					
V_{thon}	OFF/ON Threshold (Dialtone)	Voltage Level at RXIN		10		mV_{rms}
V_{thon}	ON/OFF Threshold (Busy/Ringback)	Pin In Dialer Mode		4.6		
t_{on}	Energy Detect in the Dialer Mode (Detecting Call Progress Tones)	At $\overline{EDET}$ Pin	25	30	35	ms
t_{off}	Energy Detect in the Dialer Mode (Detecting Call Progress Tones)		30	36	42	ms

ANALOG LINE INTERFACE

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{line} (Note 1)	Output Level at TXO: Data Mode		0.66	0.71	0.76	V_{rms}
V_{tonh} (Note 1)	Output Level at TXO: DTMF HIGH Group		1.02	1.1	1.18	V_{rms}
V_{tonl} (Note 1)	Output Level at TXO: DTMF LOW Group		0.84	0.9	0.97	V_{rms}
$V_{\overline{TXSQ}}$	Output Level at TXO: $\overline{TXSQ}$ Active			0.3		mV_{rms}
P_{ext}	Extraneous Frequency Output Relative to DTMF power	Any DTMF Digit			−20	dB
V_{oo}	Output Offset	At TXO		5.0		mV
V_{RXIN}	Talker Echo and Received Signal	At RXIN			1.56	V_{PEAK}
Z_{RXIN}	Input Impedance			100		kΩ

Note 1: Output level at TXO will vary directly with V_{DD} supply.

CLOCK INTERFACE

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{clock}	Clock Frequency			3.6864		MHz
T_{clock}	Clock Frequency Tolerance		−.01		+.01	%
V_{exth}	External Clock Input HIGH	XTAL2 Driven and XTL1 Grounded	4.5			V
V_{extl}	External Clock Input LOW				0.5	V

Electrical Characteristics unless otherwise noted: V_{DD} = 5.0V, V_{SS} = −5.0V, DGND = AGND = 0V, T_A = 25°C; all digital signals are referenced to DGND, all analog signals are referenced to AGND (Continued)

DIGITAL INTERFACE

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Voltage LOW				0.6	V
V_{IH}	Input Voltage HIGH		2.2			V
V_{OL}	Output Voltage LOW	I_L = 1.6 mA			0.6	V
V_{OH}	Output Voltage HIGH	I_L = −2.0 mA	3.0			V
I_{IL}	Input Current LOW	DGND ≤ V_{IN} ≤ V_{IL}, All Digital Inputs			−100	μA
I_{IH}	Input Current HIGH	V_{IH} ≤ V_{IN} ≤ V_{DD}	+50			μA

POWER INTERFACE

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operating Current	No Analog Signals		4.3	10	mA
I_{SS}	Operating Current	No Analog Signals		−2.7	−5.0	mA

TRANSMIT (ASYNC/SYNC) AND RECEIVE (SYNC/ASYNC) BUFFERS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
M	Input Character Length	Start Bit + Data Bits + Stop Bit	8		11	Bits
R_{txchar}	Input Intracharacter Signaling Rate	At $\overline{TXD}$ Pin	1170	1200	1212	bps
L_{break}	Input Break Sequence Length	At $\overline{TXD}$ Pin	M			Bits
L_{brkseq}	Transmitted Break Sequence Length	At TXO Pin	2M + 3			Bits
L_{txchar}	Output Intracharacter Signaling Rate	At $\overline{RXD}$ Pin		1219.05		bps

CARRIER FREQUENCIES AND SIGNALING RATES

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{cxr} (ORIG)	HS Cxr Freq. (Orig. Mode)	HS = 1, O/$\overline{A}$ = 1		1200		Hz
F_{cxr} (ANS)	HS Cxr Freq. (Ans. Mode)	O/$\overline{A}$ = 0		2400		Hz
Baud	Dibit Rate			600		Baud
F_{mark} (ORIG)	Mark Frequency, Originate Mode (1270)	HS = 0, O/$\overline{A}$ = 1, $\overline{TXD}$ = 1		1269.42		Hz
F_{space} (ORIG)	Space Frequency, Originate Mode (1070)	$\overline{TXD}$ = 0		1066.67		Hz
F_{mark} (ANS)	Mark Frequency, Answer Mode (2225)	HS = 0, O/$\overline{A}$ = 0, $\overline{TXD}$ = 1		2226.09		Hz
$F_{anstone}$	Answer Tone (2225)	$\overline{TEST}$ = 1, HSK1 = HSK2 = 0		2226.09		Hz
F_{space} (ANS)	Space Frequency, Answer Mode (2025)	HS = 0, O/$\overline{A}$ = 0, $\overline{TXD}$ = 0		2021.05		Hz
F_{tonl}	DTMF Low Frequency Tone Group	Dialer Mode $\overline{TEST}$ = HSK1 = HSK2 = 0		698.2 771.9 853.3 942.3		Hz
F_{tonh}	DTMF High Frequency Tone Group	Dialer Mode $\overline{TEST}$ = HSK1 = HSK2 = 0		1209.4 1335.7 1476.9 1634.0		Hz
T_{ol}	Tolerance of Above Frequencies/Signaling Rates		−0.01		+0.01	%
bps	Data Rate	Low-Speed Mode	0		300	bps

Electrical Characteristics unless otherwise noted: V_{DD} = 5.0V, V_{SS} = −5.0V, DGND = AGND = 0V, T_A = 25°C; all digital signals are referenced to DGND, all analog signals are referenced to AGND (Continued)

SYSTEM PERFORMANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BER (High-Band Receive)	**Bit Error Rate:** SNR required for BER = 10^{-5} @ 1200 bps on a 3002–C0 line, with 5 kHz white noise referred to 3 kHz. Values shown are for originate mode. (**Note:** P_{line} values assume 4 dB net gain from line to RXIN. Net gain varies with DAA type and design). (See *Figures 2, 3*)	P_{line} = −34 dBm P_{line} −44 dBm		10 11		dB dB
	Telegraph Isochronous Distortion	Back-to-Back, 300 bps (Low-Speed Mode)		10		% Peak
F_{OS}	**Frequency offset:** Incoming Carrier Frequency Offset Acquirable by 1200 bps Receiver	Zero Errors in 10^5 Bits, Originate/Answer Modes, Flat, C0 and C2 Lines. P_{line} = −40 dBm		±6		Hz

Pin Descriptions

Pin No.	Pin Name	Description
1 2	SLIM LIM	Connect external capacitor between pins 1 and 2 (Note 3).
3	RXIN	Line signal to modem; usually from 2-wire/4-wire hybrid. AC coupling is recommended. (Note 3)
4	$\overline{DOT}$	Test pattern. In Data ($\overline{TEST}$ = 1) or Analog Loop modes, substitutes a dotting pattern for $\overline{TXD}$ and overrides $\overline{SYNC}$, MOD1 and MOD2. If HS = 1, provides a 1200 bps dotting pattern (600 Hz square wave), and places RCVR and XMTR in SYNC mode with internal clock source. If HS = 0, provides a 155 bps dotting pattern. 1 = normal transmit data path, 0 = dotting.
5	ETC	External Transmit Clock. 1200 Hz external clock providing XMTR timing in SYNC mode, selected by MOD1, MOD2 pins. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Provided on SCT pin if selected.
6	$\overline{SYNC}$	Selects CHAR ASYNC or BIT SYNC mode. 1 = ASYNC mode: enables XMIT & RCV buffers, sets character length according to MOD1, MOD2 pins. 0 = SYNC mode: disables buffers, selects TX clock source according to MOD1, MOD2 pins. Active only if HS = 1.
7	$\overline{EDET}$	Energy Detect. In data mode, $\overline{EDET}$ = 0 if valid signal above threshold is present for 155 ms ±50 ms, $\overline{EDET}$ = 1 if signal below threshold for >17 ms ±7 ms. In dialer mode, follows on/off variations of call-progress tones, when $\overline{TXSQ}$ = 0.
8	HS (Note 1)	Selects modem speed. 1 selects 1200 bps. 0 selects 300 bps.
9	SCRM	Scrambler. "0" disables scrambler and descrambler for testing purposes.
10	$\overline{TXD}$	XMIT Data. Serial data from host or UART. Disconnected when digitally looped, or in dialer, dotting answer tone or force continuous mark or space modes.
11 12	XTL2 XTL1	Frequency control. 3.6864 MHz Pierce crystal oscillator. XTL2 can be driven by external 5V logic, with XTL1 grounded. XTL2 can drive external logic through AC coupled buffer.
13	SCR	Serial Clock Receive. In SYNC mode, 1200 Hz bit clock recovered from RCVD signal. May be pin-selected (MOD1, MOD2) as local transmit clock (SLAVE mode); provided on SCT pin if selected. $\overline{RXD}$ changes on negative edge, sampled on positive edge. Undefined in ASYNC mode.
14	$\overline{RXD}$	RCVD Data. Serial data to host, internally clamped to mark (=1) when modem is in digital loop or $\overline{EDET}$ in inactive (=1).

Pin Descriptions (Continued)

Pin No.	Pin Name	Description
15	$\overline{RLST}$	Remote Loop Status, used in RDL mode. Responding modem: sets $\overline{RLST}$ = 0 upon receipt of unscrambled mark for 154 ms–231 ms. Initiating modem: asserts $\overline{RLST}$ = 0 upon receipt of scrambled mark for 231 ms–308 ms. (See Table III).
16 17 19	HSK1 HSK2 $\overline{TEST}$	When the $\overline{TEST}$ pin is inactive (high), HSK1 and HSK2 select oneof four transmit conditions, for use when programming the Handshake sequences. (See Table I). When $\overline{TEST}$ is active (low), the HSK1 and HSK2 pins select one of three test conditions, or, alternatively, the dialer mode used for call progress tone detection and DTMF tone generation.
18	DGND	Digital Ground
20 21	MOD2 (Note 1) MOD1 (Note 1)	Selects character length (ASYNC) or TX clock (SYNC). In ASYNC mode, selects 8-, 9-, 10- or 11-bit character length; in SYNC mode, selects internal, external or recovered RCV clock as XMTR data clock source. Active only if HS = 1. (See Table I)
22	SCT	Serial Clock Transmit. 1200 Hz clock output providing XMTR timing in SYNC mode. SCT source (INT., EXT., SLAVE) selected by MOD1, MOD2 pins. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Internal clock provided in ASYNC mode.
23	$\overline{TXSQ}$ (Note 2)	Squelch XMTRS in data mode. 0 = Both XMTRS off; 1 = turns on XMTR selected by HS pin. In dialer mode, 0 = DTMF generator OFF/Call progress detection. 1 = DTMF generator ON.
24	O/$\overline{A}$ (Note 1)	Orig/Answer Mode Select. Assigns channels to XMTRS/RCVRS. 1 = Originate mode, 0 = Answer mode.
25	TXO	Transmit line signal from modem; usually to 2-wire/4-wire line hybrid input. AC coupling is recommended (Note 3).
26	AGND	Analog Ground
27	V_{SS}	Negative power supply V_{SS} = −5.0V
28	V_{DD}	Positive power supply V_{DD} = +5.0V

Note 1: For µA212AT in dialer mode with $\overline{TXSQ}$ = 1, O/$\overline{A}$, HS, MOD1 and MOD2 select the desired DTMF tone pair.

Note 2: The µA212AT is pin and function compatible with the µA212A (without integral DTMF); in upgrade applications, insure proper state of $\overline{TXSQ}$ as indicated. See Technical Bulletin M–1.

Note 3: Capacitors in signal paths should be ≥ 0.033 µF and have ~ zero voltage coefficients.

Functional Description*

Refer to *Figure 1.*

TRANSMITTER

The transmitter consists of high-speed and low-speed modulators, a transmit buffer and scrambler, and a transmit filter and line driver. In high-speed asynchronous mode, serial transmit data from the host or UART enters the transmit buffer, which synchronizes the data to the internal 1200 bps clock. Data which is underspeed relative to 1200 bps periodically has the last stop bit sampled twice resulting in an added stop bit. Similarly, overspeed input data periodically has unsampled—and therefore deleted—stop bits. The MOD1 and MOD2 pins choose 8-, 9-, 10- or 11-bit character lengths. In synchronous mode the transmit buffer is disabled. The transmitter clock source may be chosen by MOD1 and MOD2: internal, external or derived from the recovered received data. A scrambler precedes encoding to ensure that the line spectrum is sufficiently distributed to avoid interference with the in-band supervisory single-frequency signaling system employed in most Bell System toll trunks. The randomized spectrum also facilitates timing recovery in the receiver. The scrambler is characterized by the following recursive equation:

$$Y_i = X_i \oplus Y_{i-14} \oplus Y_{i-17}$$

where X_i is the scrambler input bit at time i, Y_i is the scrambler output bit at time i and ⊕ denotes the XOR operation.

212A-type modems achieve full-duplex 1200 bps operation by encoding transmitted data by bit-pairs (dibits), thereby halving the apparent data rate. The resultant reduced spectral width allows both frequency channels to coexist in a limited bandwidth telephone channel with practical levels of filtering. The four unique dibits thus obtained are gray-coded and differentially phase modulated onto a carrier at either 1200 Hz (originate mode) or 2400 Hz (answer mode). Each dibit is encoded as a phase change relative to the phase of the preceding signal dibit element:

Dibit	Phase Shift (deg)
00	+90
01	0
11	−90
10	180

At the receiver, the dibits are decoded and the bits are reassembled in the correct sequence. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator after the scrambler. The lowspeed transmitter generates phase-coherent FSK using one of two programmable tone generators. Answer mode mark (2225 Hz) is also utilized as answer tone in both low- and high-speed operation.

In Dialer mode, both tone generators are employed to generate DTMF tone pairs. The summed modulator outputs drive a lowpass filter which serves as a fixed compromise amplitude and delay equalizer for the phone line and reduces output harmonic energy well below maximum specified levels. The filter output drives an output buffer amplifier with low output impedance. At the TXO pin, the buffer provides 700 mVrms in data mode, for a nominal −9 dBm level at the line, assuming 2 dB loss in the data access arrangement.

*For additional information ask for Applications Note ASP-1 "Theory of Operation—µA212A" and Technical Bulletins M1, M3 & M4.

Functional Description* (Continued)

DTMF TONE GENERATION

The μA212AT includes on-chip DTMF generation, using two programmable tone generators. Dialer mode must be selected ($\overline{TEST}$ = HSK1 = HSK2 = 0) for DTMF dialing. The O/$\overline{A}$, HS, MOD1 and MOD2 pins are used to select the required digit according to the encoding scheme shown in Table II, and the tones are turned on and off by the logic level on $\overline{TXSQ}$. The generated tones meet the applicable CCITT and EIA requirement for tone dialing. DTMF output levels are 0.9 Vrms (low group) and 1.1 Vrms (high group).

RECEIVER

The received signal from the line-connection circuitry passes through a lowpass filter which performs anti-aliasing and compromise amplitude and delay equalization of the incoming signal. Depending upon mode selection (originate/answer) the following mixer either passes or down converts the signal to the 1200 Hz bandpass filter. In analog loopback mode, the receiver originate and answer mode assignments are inverted, which forces the receiver to operate in the transmitter frequency band. The 1200 Hz bandpass filter passes the desired received signal while attenuating the adjacent transmitted signal component reflected from the line (talker echo). The chosen passband shape converts the spectrum of the received high-speed signal to 100% raised cosine to minimize intersymbol interference in the recovered data. Following the filter is a soft limiter and a signal energy detector. An external capacitor is used to eliminate offset between the soft limiter output and the following limiter.

The energy detector provides a digital indication that energy is present within the filter passband at a level above a preset threshold. At least 2 dB of hysteresis is provided between on and off levels to stabilize the detector output. In dialer mode, the detector output is used to provide logic level indication of the presence of call progress tones.

The limiter output drives the QPSK demodulator and the carrier and clock recovery phase-locked loops. The low-speed FSK demodulator shares part of the clock recovery loop. The QPSK demodulator and carrier loop form a digital coherent detector. This technique offers a 2 dB advantage in error performance compared to a differential demodulator. The demodulator outputs are in-phase (I) and quadrature (Q) binary signals which together represent the recovered dibit stream. The dibit decoder cirucit utilizes the recovered clock signal to convert this dibit stream to serial data at 1200 bps.

The recovered bit stream is then descrambled, using the inverse of the transmit scrambler algorithm. In synchronous mode the descrambler output is identically the received data, while in asynchronous mode the descrambler output stream is selectively processed by the receive buffer. Underspeed data presented to the transmitting modem passes essentially unchanged through the receive buffer.

Overspeed data, which had stop bits deleted at the transmitter, has those stop bits reinserted by the receive buffer. (Generally, stop bit lengths will be elastic). The receive buffer output is then presented to the receive data pin ($\overline{RXD}$) at a nominal intracharacter rate of 1219.05 bps.

MASTER CLOCK/OSCILLATOR/DIVIDER CHAIN

The μA212AT may be controlled by either a quartz crystal operating in parallel mode or by an external signal source at 3.6864 MHz. The crystal should be connected between XTL1 and XTL2 pins, with a mica or high-Q ceramic 30 pF capacitor from each pin to digital ground (See *Figure 1*). An external circuit may be driven from XTL2. In this case, AC coupling to a high impedance load should be used. Note that total capacitance to ground from XTL2, including such an external circuit, should be 30 pF. Crystal requirements; $R_S < 150\Omega$, C_L = 18 pF, parallel mode, tolerance (accuracy, temperature, aging) less than ±75 ppm. An external TTL drive may be applied to the XTL2 pin, with XTL1 grounded. Internal divider chains provide the timing signals required for modulation, demodulation, filtering, buffering, encoding/decoding, energy detection and remote digital loopback. Timing for line connect and disconnect sequences (handshaking) derives from the host controller, ensuring maximum applications flexibility.

Control Considerations

The host controller, whether a dedicated microcontroller or a digital interface, controls the μA212AT as well as the line connect circuit and other IC's. On-chip timing and logic circuitry has been specifically designed to simplify the development of control firmware.

OPERATING AND TEST MODES

Table I indicates the operating and test modes defined by eight control pins. The μA212AT (together with the host controller) supports analog loopback, and local and remote digital loopback modes. Analog loopback forces the receiver to the transmitter channel. The controller forces the line control circuit on-hook but continues to monitor the ring indicator. This mode is available for low-speed, high-speed synchronous and high-speed asynchronous operation. In local digital loop, the modem I.C. isolates the interface, slaves the transmit clock to SCR (high-speed mode), and loops received data back to the transmitter. In remote digital loop, local digital loop is initiated in the far-end modem by request of the near-end modem, if the far-end modem is so enabled. The μA212AT includes the handshake sequences required for this mode; the controller merely monitors $\overline{RLST}$ and controls remote loopback according to Table III. Remote loop is only available in high-speed mode.

Control Considerations (Continued)

Answer Tone — In this mode, 2225 Hz answer tone is transmitted provided $\overline{TXSQ}$ is inactive high (= 1). Receive data rate is selected as normal with the HS pin. This permits the data rate of the originating modem to be determined while answer tone is continuously transmitted.

Force Continuous Mark — Disconnects $\overline{TXD}$ pin from the transmitter and forces the signal internally to a mark (logic 1).

Force Continuous Space — Disconnects $\overline{TXD}$ pin from the transmitter and forces the signal internally to a space (logic 0).

Analog Loop — Receiver is forced to the transmitter channel. With modem on-hook (disconnected from line) signal from TXO is reflected through hybrid to RXIN.

Local Digital Loop — Forces synchronous mode, and internally loops received data to transmitter and SCR to SCT. Transmitted data ($\overline{TXD}$) and clock (ETC) are ignored. SCR and SCT are provided. $\overline{RXD}$ is forced to 1.

Remote Digital Loop — Initiating modem: If RDL is initiated ($\overline{TEST}$ = 0, HSK1 = 1, HSK2 = 0), $\overline{TXD}$ is isolated, $\overline{RXD}$ is clamped to a 1 and unscrambled mark is transmitted. When high speed scrambled dotting pattern is detected, scrambled mark is transmitted. Upon receipt of scrambled mark from responding modem, $\overline{RLST}$ is set to 0.

Responding modem: Upon receipt of unscrambled mark when in data mode ($\overline{TEST}$ = HSK1 = HSK2 = 1), $\overline{RLST}$ is set to 0. Upon detecting this the controller responds by setting $\overline{TEST}$ and HSK2 to 0, and the μA212AT sets synchronous mode, isolates $\overline{TXD}$, clamps $\overline{RXD}$ to 1, and transmits a 1200 bps scrambled dotting pattern. Upon receipt of a scrambled mark signal, the μA212AT internally loops received data and clock to the transmitter and resets (See Table III).

Dialer Mode — The μA212AT provides DTMF tone generation and energy indication at $\overline{EDET}$ pin to identify call progress tones, i.e. dial, busy and ringback. The DTMF digit is selected by the levels on O/$\overline{A}$, HS, MOD1 and MOD2 according to Table II. Tone generation is turned on and off by the level on $\overline{TXSQ}$. 1 = on, 0 = off.

Block Diagram

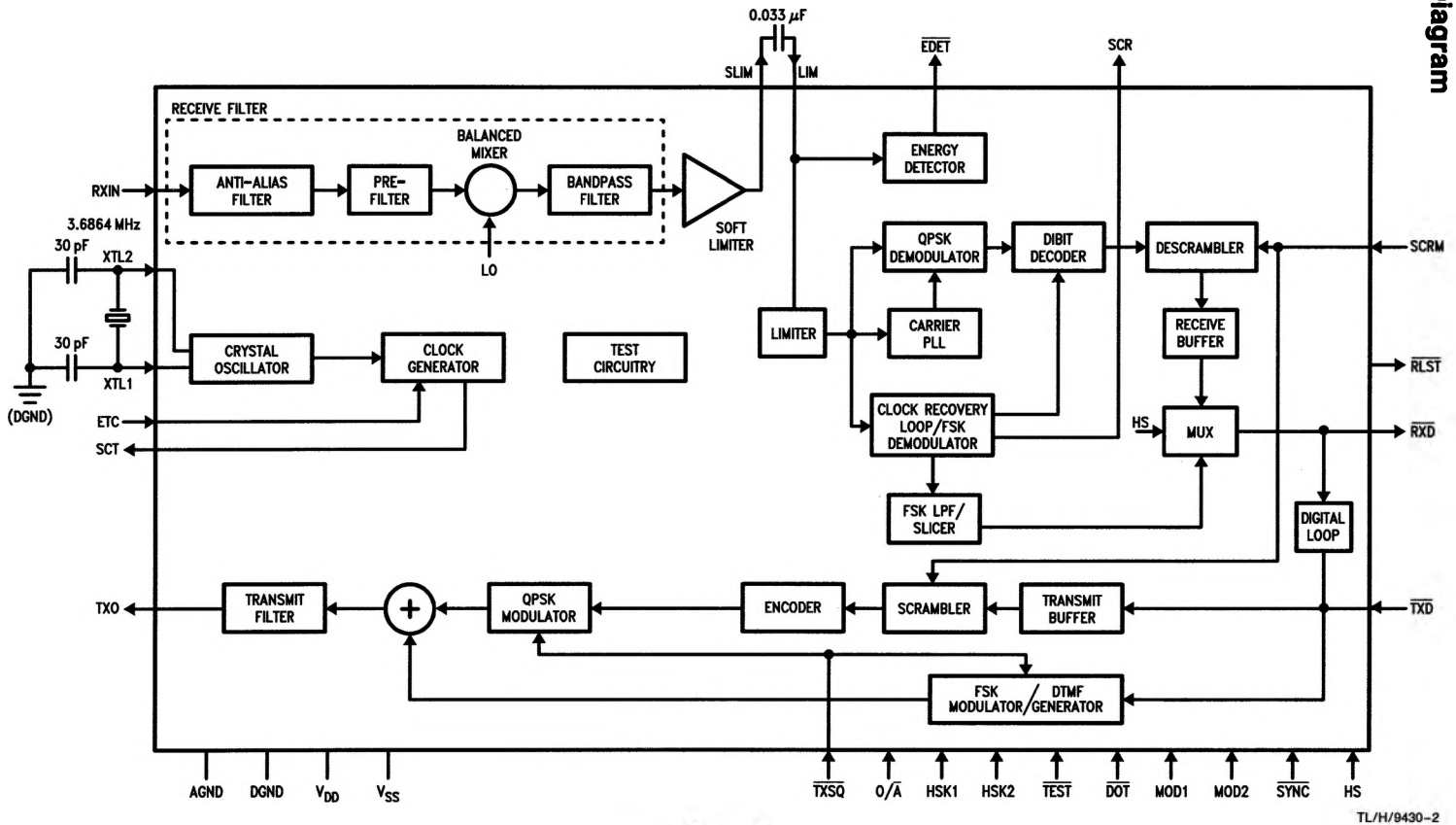


FIGURE 1

TABLE I. Operating and Test Modes

$\overline{DOT}$	HS	$\overline{SYNC}$	MOD1	MOD2	$\overline{TEST}$	HSK1	HSK2	Description	SCT
0	—	X	X	X	1	X	X	Dotting Pattern (155 or 1200 bps)	INT
1	—	—	—	—	1	0	0	Answer Tone	*
1	—	—	—	—	1	0	1	Force Continuous Mark	*
1	—	—	—	—	1	1	0	Force Continuous Space	*
1	1	1	0	0	1	1	1	ASYNC, 8-Bit	INT
1	1	1	0	1	1	1	1	ASYNC, 9-Bit	INT
1	1	1	1	1	1	1	1	ASYNC, 10-Bit	INT
1	1	1	1	0	1	1	1	ASYNC, 11-Bit	INT
1	1	0	1	1	1	1	1	SYNC, Internal	INT
1	1	0	1	0	1	1	1	SYNC, Slave	SCR
1	1	0	0	1	1	1	1	SYNC, External	ETC
—	—	—	—	—	0	0	1	Analog Loop	*
1	—	X	X	X	0	1	1	Local Digital Loop	SCR
1	1	—	—	—	0	1	0	Remote Digital Loop Initiate	*
1	1	X	X	X	0	1	0	Respond to Far End Request for RDL	SCR
1	X	X	X	X	0	0	0	Dialer Mode (See Table II)	*
1	0	X	X	X	—	—	—	Low-Speed Mode	INT

Key:

SCT—TX Buffer and PSK Modulator Clock

SCR—Receive Clock

ETC—External Clock Input

INT—Internal 1200 Hz Clock

X—Don't Care (except avoid $\overline{SYNC}$ = MOD1 = MOD2 = 0)

— —Set as appropriate for desired operating condition.

*—As set by $\overline{SYNC}$, MOD1, MOD2.

TABLE II. DTMF Encoding

O/A	HS	MOD1	MOD2	DTMF Digit
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	*
1	0	1	1	#
1	1	0	0	A
1	1	0	1	B
1	1	1	0	C
1	1	1	1	D

Note: $\overline{TEST}$, HSK1 and HSK2 must be = 0 for DTMF to operate. (See Table I.)

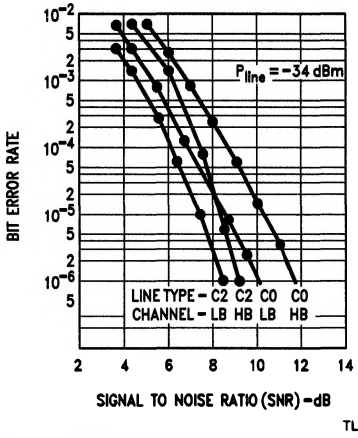


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FIGURE 2. Bit Error Rate vs Signal-to-Noise Ratio

Note: BER measured in synchronous mode, using an AEA S3A channel simulator.

TABLE III. Remote Digital Loopback (RDL) Command Sequences

Modem Action	Controller Action	$\overline{\text{TEST}}$	HSK1	HSK2	$\overline{\text{RLST}}$
Data Mode		1	1	1	1
Initiate RDL: Disable scrambler Disconnect $\overline{\text{TXD}}$ Force 1 on $\overline{\text{RXD}}$ Transmit unscrambled mark (U.M.) Recognize Dotting for 231–308 ms Enable scrambler Transmit scrambled mark (S.M.) Recognize S.M. for 231–308 ms Connect $\overline{\text{TXD}}$ Unclamp $\overline{\text{RXD}}$ "RDL ESTABLISHED"	"INITIATE RDL"	0 0	1 1	0 0	1 0
Response to far end request: U.M. recognized for 154–231 ms "RDL REQUESTED" Disconnect $\overline{\text{TXD}}$ Force 1 on $\overline{\text{RXD}}$ Force Sync Slave Mode Transmit Dotting S.M. recognized Internally loop Receiver to Transmitter "RDL ESTABLISHED"	"RDL RESPONSE OK"	1 0 0	1 1 1	1 0 0	0 0 1
Terminate RDL: Reset to Data Mode	$\overline{\text{TXSQ}}$ active 80 ms	1 1	1 1	1* 1	0 1

*$\overline{\text{TEST}}$ = HSK1 = HSK2 = 1 may be asserted at any time after "RDL ESTABLISHED" and before terminating.

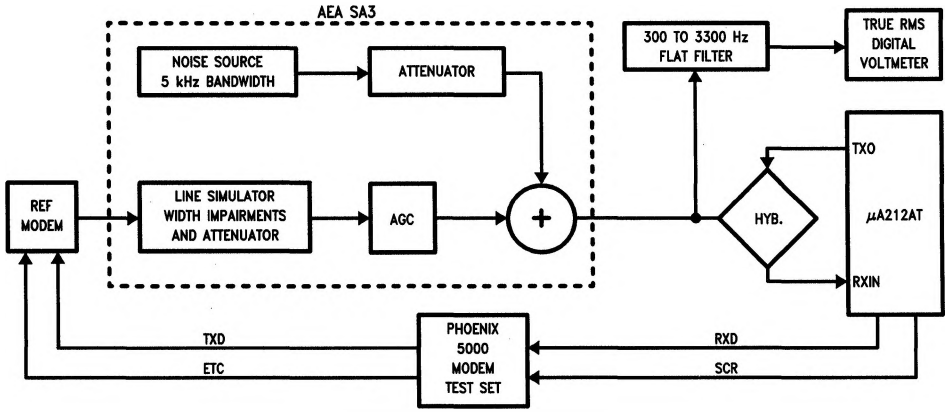

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FIGURE 3. 2-Wire Bit Error Test Setup