AM/FM-PLL

Description

The U4288BM is an integrated circuit in BICMOS technology for frequency synthesizers. It performs all the functions of a PLL radio tuning system and is controlled by software via a serial 3-wire bus. The device is designed for frequency synthesizer applications where a very fast response time of the loop is required, e.g., RDS (TMC), RBDS, AUDIS.

Features

- Reference oscillator up to 16 MHz
- FM minimum-step frequency 5 kHz
- AM minimum-step frequency 1 kHz
- Very fast response time of the FM-loop due to the sub PLL concept (between two preselected frequencies)
- Separately programmable reference dividers for sub PLL0 and sub PLL1 (for different step frequencies)
- Reference frequencies of the main PLL can be switched directly via an external pin or 3-wire bus
- Suitable for conventional AM or AM up-down conversion
- All functions can be controlled by software via a serial 3-wire bus
- 4 programmable switching outputs
- Separate input for US weather-band tuning

Block Diagramm

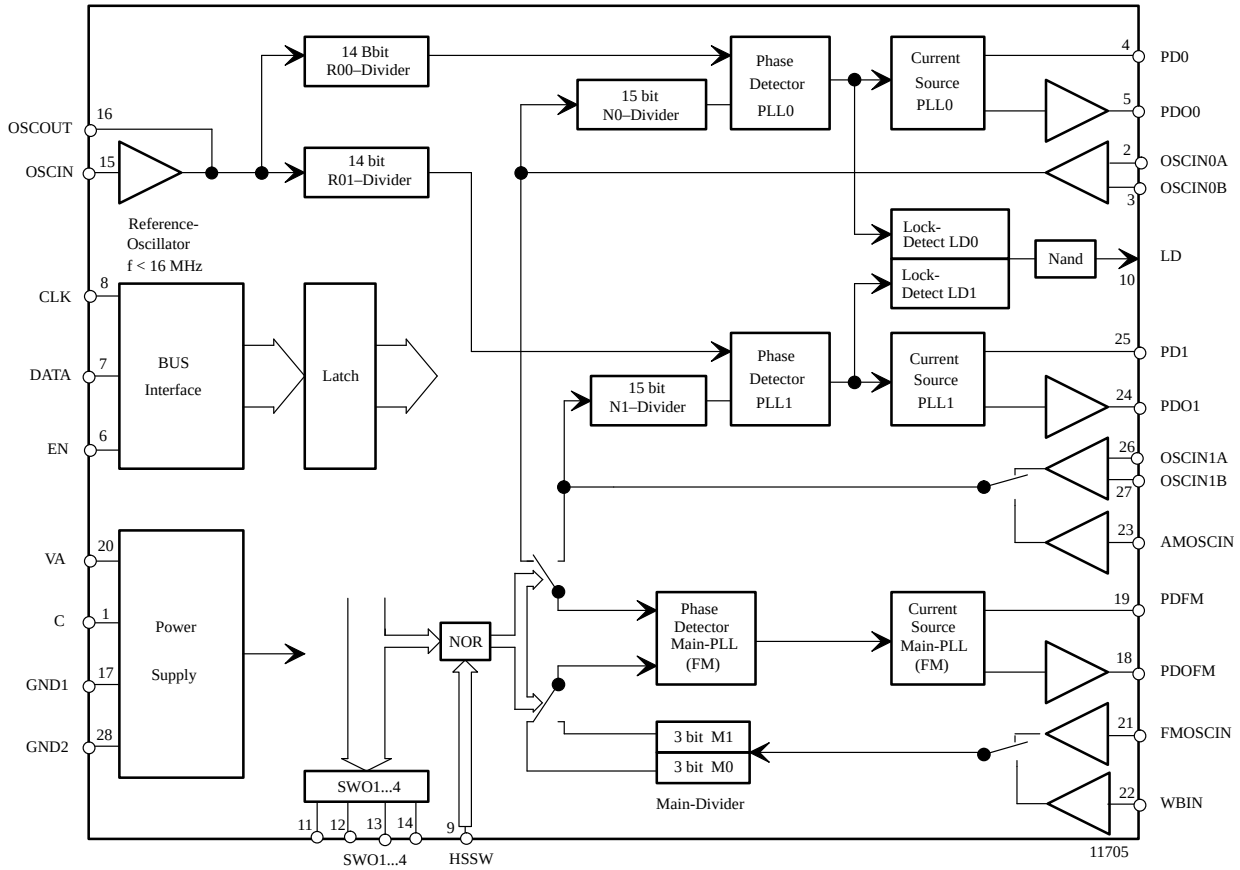


Figure 1. Block diagram

Pin Description

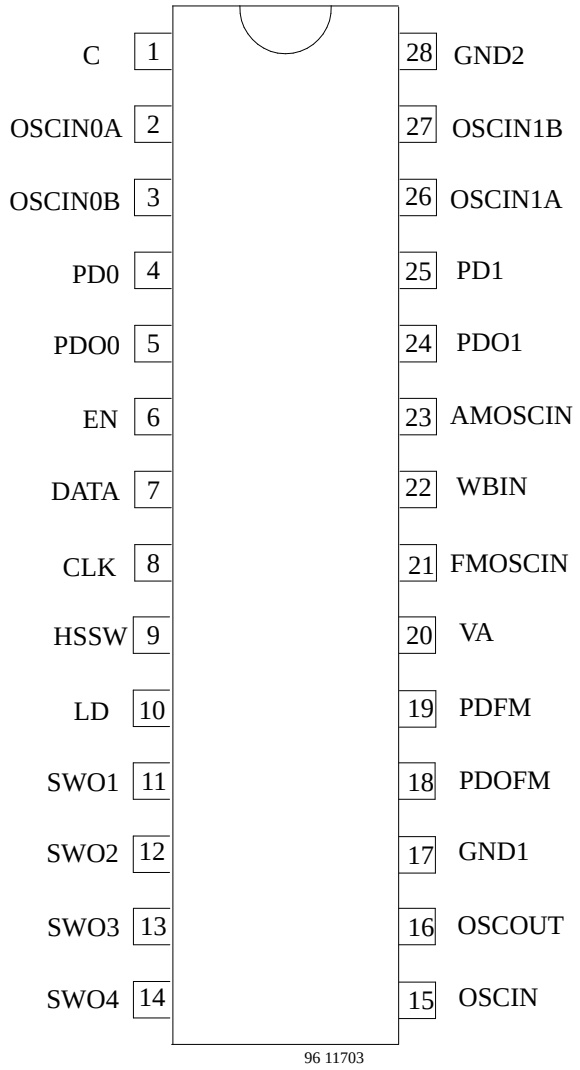


Figure 2. Pinning

Pin	Symbol	Function
1	C	Capacitor internal supply voltage
2	OSCIN0A	Suboscillator PLL0 input A
3	OSOIN0B	Suboscillator PLL0 input B
4	PD0	Current output PLL0
5	PDO0	Analog output PLL0
6	EN	Enable
7	DATA	Data
8	CLK	Clock
9	HSSW	High-speed switch mode
10	LD	Lock detection for sub PLL0 and sub PLL1
11	SWO1	Switching output 1
12	SWO2	Switching output 2
13	SWO3	Switching output 3
14	SWO4	Switching output 4
15	OSCIN	Reference-oscillator input (< 16 MHz)
16	OSCOUT	Reference-oscillator output
17	GND1	Ground 1 (analog)
18	PDOFM	Analog output FM
19	PDFM	Current output FM
20	VA	Analog supply voltage
21	FMOSCIN	FM-oscillator input
22	WBIN	Weather-band input
23	AMOSCIN	AM-oscillator input for conventional mode
24	PDO1	Analog output PLL1
25	PD1	Current output PLL1
26	OSCIN1A	Suboscillator PLL1 input A
27	OSCIN1B	Suboscillator PLL1 input B
28	GND2	Ground 2 (digital)

OSCIN, OSCOUT

A crystal resonator (up to 16 MHz) is connected between OSCIN and OSCOUT in order to generate the reference frequency. The complete application circuit is shown in figure 7.
If a reference voltage is available, it can be applied at OSCIN. The minimum voltage should be 100 mV_{RMS}. In this case, pin OSCOUT must be open.

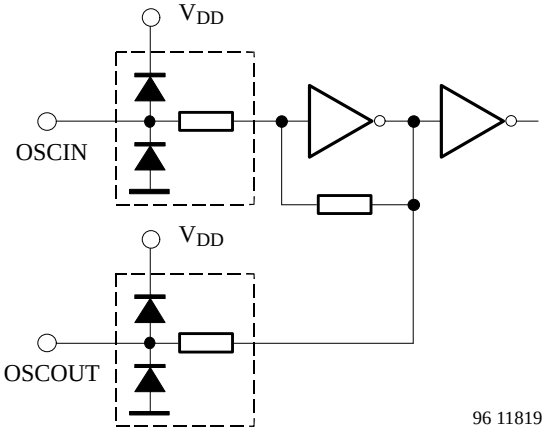


Figure 3.

EN, DATA, CLK

All functions can be controlled by software via a 3-wire bus consisting of Enable, Data and Clock. The bus is designed for microcontrollers which operate with 3 V or 5 V supply voltage. Details of the data transfer protocol are shown in figures 4, 5 and 6.

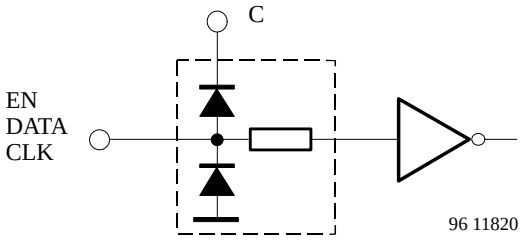


Figure 4.

SWO1, SWO2, SWO3, SWO4

All switching outputs are “open drain’’ and can be set and reset by software. Details are described in the data transfer protocol.

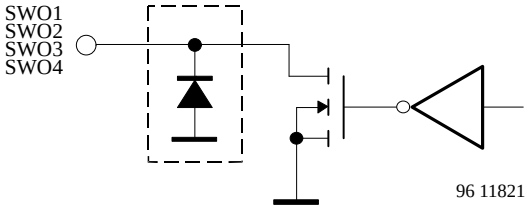


Figure 5.

C

A capacitor is connected on pin C for smoothing the supply voltage which is generated internally.

HSSW

The reference frequency for the main PLL can be switched by applying to a control voltage at HSSW. If the control voltage is low, sub PLL1 is activated as the reference frequency. However, that the reference frequency can only be switched at HSSW if the bit HSS is set low by software.

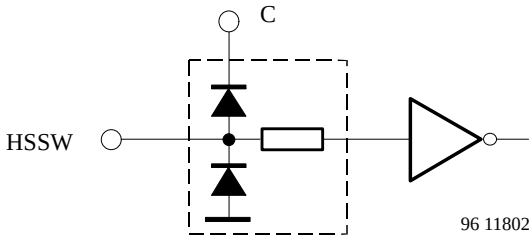


Figure 6.

LD

The lock detector is an open-drain output indicating the status of sub PLL0 and sub PLL1. If both sub PLLs are locked in, the output will be high. Otherwise the output is low.

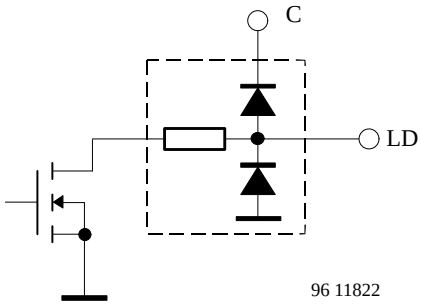


Figure 7.

PD0

PD0 is the current charge-pump output of the sub PLL0. The current can be chosen by setting the bits IPD0 1/2 and IPD0 3/4. The loop filter has to be designed corresponding to the chosen charge pump current and the internal reference frequency. A recommendation can be found in the application circuit.

PDO0

PDO0 is the loop amplifier output of the sub PLL0. The bipolar output stage is a rail-to-rail amplifier.

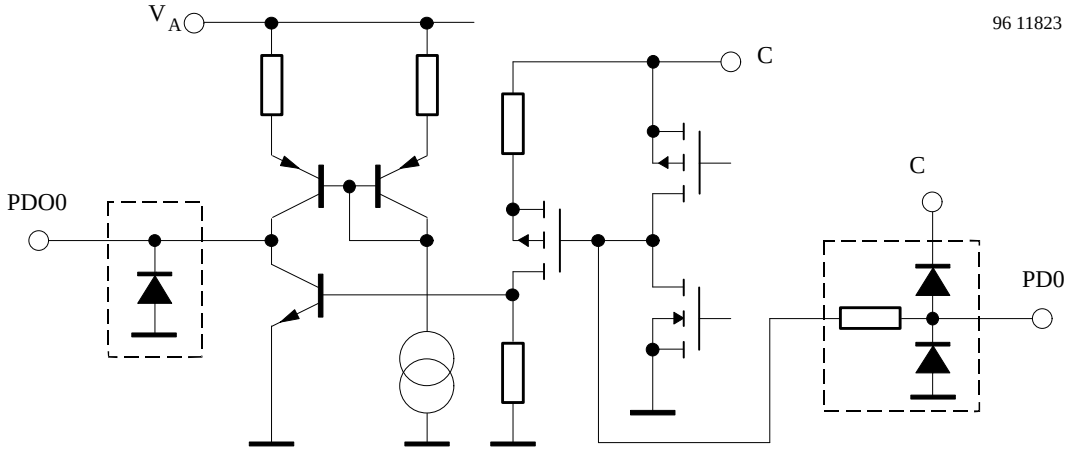


Figure 8.

PD1

PD1 is the current charge pump output of the sub PLL1. The current can be chosen by setting the bits IPD1 1/2 and IPD1 3/4. The loop filter has to be designed corresponding to the chosen charge pump current and the internal reference frequency. A recommendation can be found in the application circuit.

PDO1

PDO1 is the loop amplifier output of the sub PLL1. The bipolar output stage is a rail-to-rail amplifier.

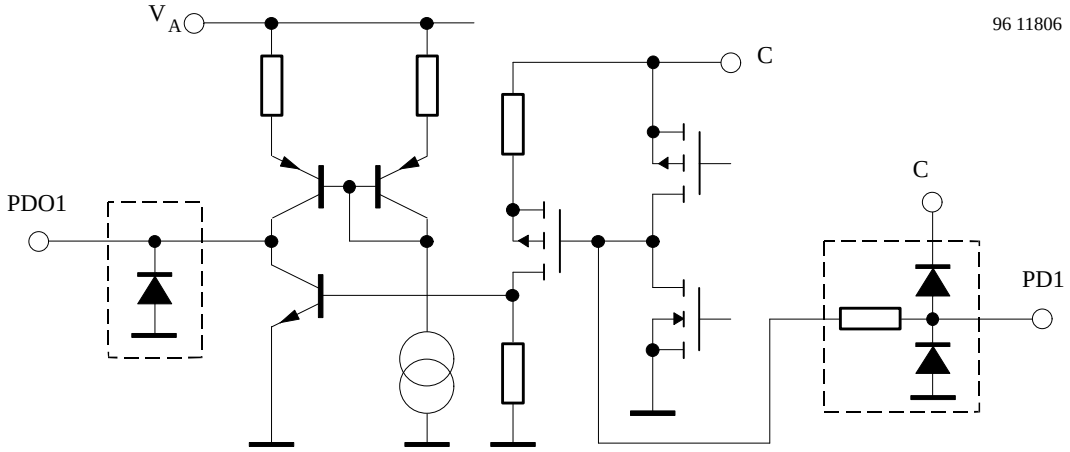


Figure 9.

PDFM

PDFM is the current charge pump output of the main PLL. The current can be chosen by setting the bits IPDM 1/2 and IPDM 3/4. The loop filter has to be designed corresponding to the chosen charge pump current and the internal reference frequency. A recommendation can be found in the application circuit.

PDOFM

PDOFM is the loop amplifier output of the main PLL. The bipolar output stage is a rail-to-rail amplifier.

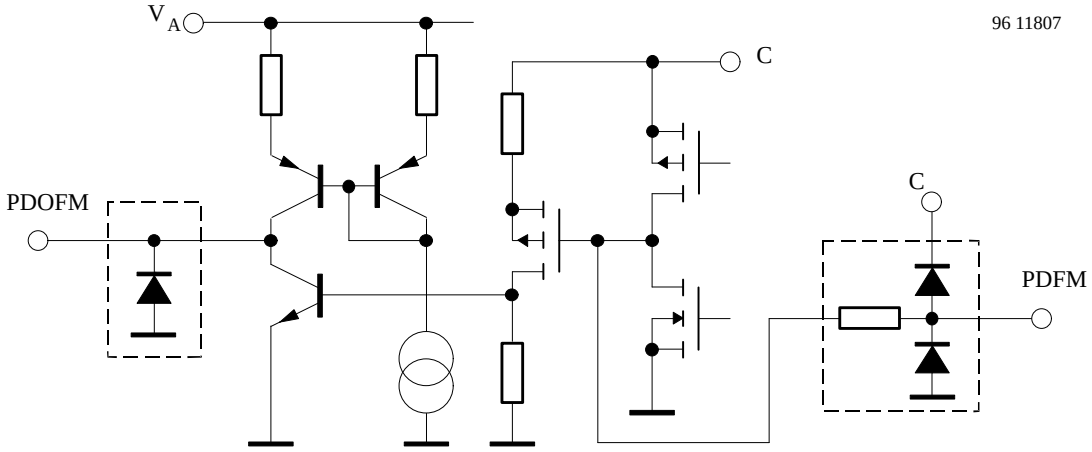


Figure 10.

FMOSCIN

FMOSCIN is the pre-amplifier input for the FM-oscillator signal.

AMOSCIN

AMOSCIN is the pre-amplifier input for AM-oscillator signal (Conventional AM-mode)

WBIN

WIBIN is the pre-amplifier input for the weather-band oscillator signal.

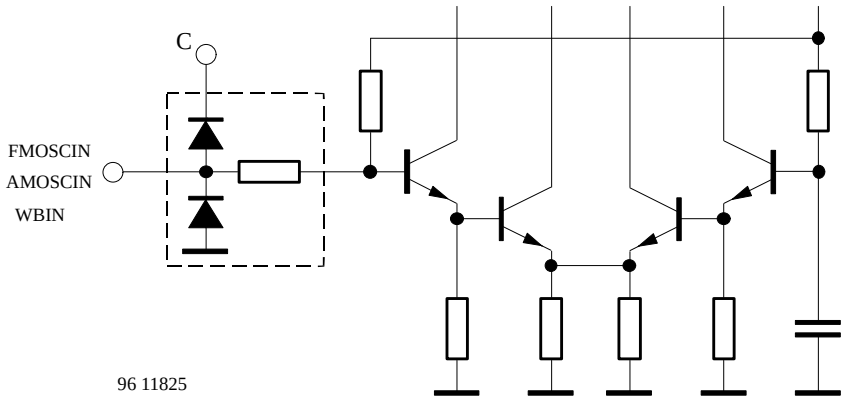


Figure 11.

OSCIN0A, OSCIN0B

The tank of the sub VCO0 is connected between OSCIN0A and OSCIN0B (see application circuit below).
The complete VCO is designed with a symmetrical structure.

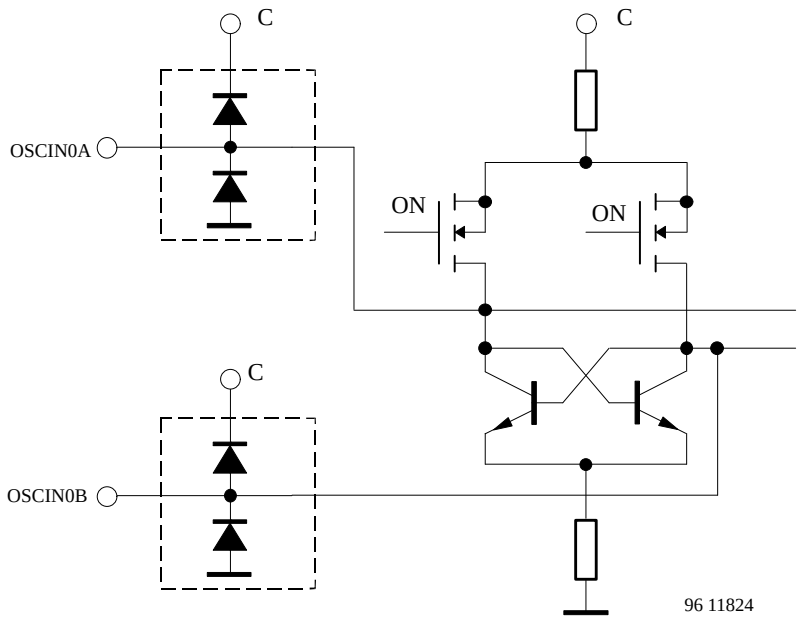


Figure 12.

OSCIN1A, OSCIN1B

The tank of sub VCO1 is connected between OSCIN1A and OSCIN1B (see application circuit below).
The complete VCO is designed with a symmetrical structure.

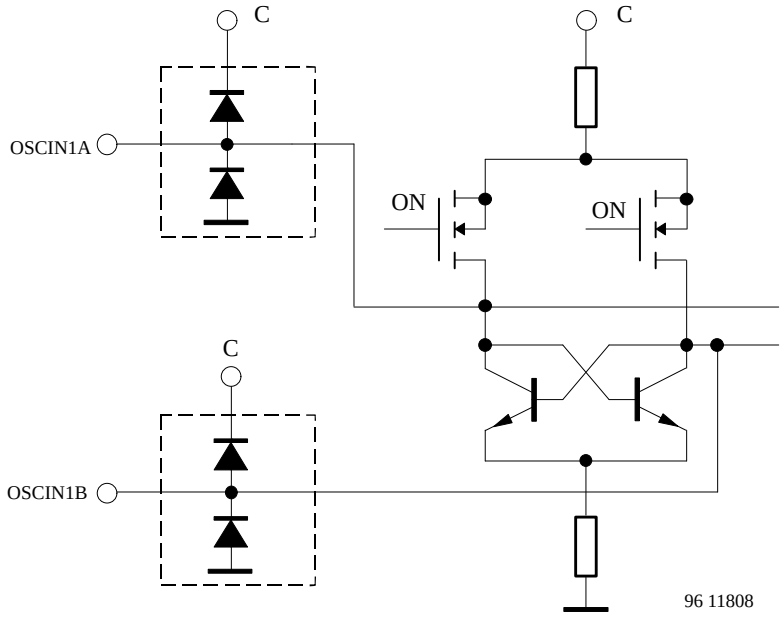


Figure 13.

Functional Description

The U4288BM is designed for radio frequency synthesizer applications, where a very fast response time of the loop and small fine tuning steps are required. Such a very fast response time of the PLL can only be achieved by using of high reference frequencies. Therefore, the U4288BM works with two sub PLLs. The oscillator frequency of each sub PLL serves as a reference frequency for the main PLL and each sub PLL which allow fine tuning steps of 5 kHz for FM and 1 kHz for AM.

There is also a lock detector output indicating the status of sub PLLs. If sub PLL0 and sub PLL1 is locked out, the output is low. If sub PLL0 and sub PLL1 are locked in, the output is high and can be switched between sub PLL0 and sub PLL1 via a the external pin or via the 3-wire bus.

All functions of the U4288BM can be controlled by software via a serial 3-wire bus consisting of Enable, Clock and Data.

The format and procedure for the data transfer from the microcomputer to the PLL are shown in figures 4, 5 and 6. The bus interface of the PLL is designed in such a way that all requested data have to be transferred by means of 8-bit, 16-bit or 24-bit commands. Due to this 8-bit structure, the serial output interface of a micro-computer can be used for the data transfer.

The status of sub PLL0 can be transferred by means of a 24-bit command and a 16-bit command. The 24-bit command contains information aon the reference divider R00, the switching outputs, charge-pump current and phase detector polarity and 2-bit address (00). The 16-bit command contains information from the 15-bit N0-divider and 1-bit address.

The status of sub PLL1 can be transferred by means of a 24-bit command and a 16-bit command. The 24-bit command contains information about the reference divider R01, the chosen band (AM, FM, weather band), charge pump current and phase detector polarity and 2-bit address (01). The 16-bit command contains information of 15-bit N1-divider and 1-bit address.

The status of the main PLL can be transferred by means of four 8-bit commands. Status 1 contains information on the main dividers M0 and M1 and 2-bit address.

Status 2 contains information on the charge pump current and phase detector polarity, analog test, high speed switch and 2-bit address. Status 3 serves only for the internal test mode.

SUB PLL0

The charge pump current can be chosen by setting the bits IPD0 1/2 and IPD0 3/4 as follows:

I / µA	IPD0 1/2	IPD0 3/4
25	0	0
100	0	1
500	1	0
2000	1	1

The phase detector can be chosen by setting of bit PDM +/– as follows:

Polarity	PDM +/–
Negative	0
Positive	1

Please note that the polarity for the TEMIC application circuit must be negative.

The switching outputs SWO1, SWO2, SWO3 and SWO4 can be set and reset as follows:

	SWO1	SWO2	SWO3	SWO4
Low	0	0	0	0
High	1	1	1	1

SUB PLL1

The charge pump current can be chosen by setting the bits IPD1 1/2 and IPD1 3/4 as follows:

I / µA	IPD1 1/2	IPD1 3/4
25	0	0
100	0	1
500	1	0
2000	1	1

The phase detector can be chosen by setting bit PDM +/– as follows:

Polarity	PDM +/–
Negative	0
Positive	1

Please note that the polarity for the TEMIC application circuit must be negative.

The information regarding the chosen band (AM, FM or weather band) has to be set as follows:

	AM / FM	WB
FM	0	0
AM	1	0
WB	0	1

Main PLL

Status 1: The main divider 0 can be chosen by setting the bits M0-2^2, M0-2^1 and M0-2^0 as follows:

Divided by	M0-2^2	M0-2^1	M0-2^0
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

The main divider 1 can be chosen by setting the bits M1-2^2, M1-2^1 and M1-2^0 as follows:

Divided by	M1-2^2	M1-2^1	M1-2^0
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Recommendation for RDS application: M0 = 4, M1 = 5

Figure 3 shows the oscillator frequency range of the sub PLLs for M0 = 4, M1 = 5 and the corresponding frequencies for the main PLL and the sub PLLs.

Status 2: The charge pump current can be chosen by setting the bits IPDM 1/2 and IPDM 3/4 as follows:

I / µA	IPDM 1/2	IPDM 3/4
25	0	0
100	0	1
500	1	0
2000	1	1

The phase detector can be chosen by setting bit PDM +/– as follows:

Polarity	PDM +/–
Negative	0
Positive	1

The oscillator frequency of sub PLL0 ($f_{SUBOSC0}$) and the oscillator frequency of sub PLL1 ($f_{SUBOSC1}$) serve as reference frequencies for the main PLL.

The reference frequency (f_{ref} main) for the main PLL can be switched by setting bit HSS as follows:

(f_{ref} main = $f_{SUBOSC0}$ or $f_{SUBOSC1}$)

	HSS
$f_{SUBOSC0}$	0
$f_{SUBOSC1}$	1

If HSS is controlled by software via the 3-wire bus, the input HSSW (Pin 9) has to be connected to GND.

Status 4: It is used only for internal test purpose.

f_{FMOSC}: 98.2 MHz to 118.7 MHz

M1 = 4	
f_{SUBOSC}: 24.55 MHz to 29.695 MHz	
f_{STEP}/kHz	$f_{STEP/SUB}$/kHz
5.0	1.25
12.5	3.125
25.0	6.25
50.0	12.5
100.0	25.0
M0 = 5	
f_{SUBOSC}: 19.64 MHz to 23.74 MHz	
$f_{STEP/MAIN}$/kHz	$f_{STEP/SUB}$/kHz
5.0	1.0
12.5	2.5
25.0	5.0
50.0	10.0
100.0	20.0

Example:

f_{FMOSC1} = 98.2 MHz

f_{FMOSC2} = 118.7 MHz

$f_{STEP/MAIN}$ = 50 kHz

f_{OSC} = 4 MHz

SUB PLL1:

M1 = 4, $f_{STEP/SUB1}$ = 12.5 kHz

$$\underline{R01} = \frac{f_{OSC}}{f_{STEP/SUB1}} = \frac{4\ MHz}{12.5\ kHz} = \underline{320}$$

$$\underline{N1} = \frac{f_{FMOSC1}}{M0 \times f_{STEP/SUB1}} = \frac{98.2\ MHz}{4 \times 12.5\ kHz} = \underline{1964}$$

SUB PLL0:

M0 = 5, $f_{STEP/SUB0}$ = 10 kHz

$$\underline{R00} = \frac{f_{OSC}}{f_{STEP/SUB0}} = \frac{4\ MHz}{10\ kHz} = \underline{400}$$

$$\underline{N0} = \frac{f_{FMOSC2}}{M1 \times f_{STEP/SUB0}} = \frac{118.7\ MHz}{5 \times 10\ kHz} = \underline{2374}$$

Conventional AM:

f_{AMOSC} = 594 kHz, $f_{STEP/AM}$ = 1 kHz, f_{OSC} = 4 MHz

$$\underline{R01} = \frac{f_{OSC}}{f_{STEP/AM}} = \frac{4\ MHz}{1\ kHz} = \underline{4000}$$

$$\underline{N1} = \frac{f_{AMOSC}}{f_{STEP/AM}} = \frac{594\ kHz}{1\ kHz} = \underline{594}$$

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Analog supply voltage Pin 20 with 220 Ω seriell resistance 2 minutes[1)]	V_A V_A	8 to 15 24	V V
Input voltage Pins 6, 7, 8 and 9	V_I	–0.3 to 5.2	V
Output drain voltage Pins 11, 12, 13 and 14	V_{OD}	15	V
Output current Pins 11, 12, 13 and 14	I_O	–1 to +5	mA
Ambient temperature range	T_{amb}	–30 to +85	°C
Storage temperature range	T_{stg}	–40 to +125	°C
Junction temperature	T_j	125	°C
Electrostatic handling	$\pm V_{ESD}$	tbd	V

[1)] corresponding our application circuit (figure 7)

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	90	K/W

Electrical Characteristics

V_A = 8.5 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Analog supply voltage	Pin 20	V_A	8.0	8.5	12	V
Analog supply current	Pin 20	I_A		tbd		mA
OSCIN						
Input voltage	f = 0.1 to 15 MHz, Pin 20	V_{OSC}	100			mV
FMOSCIN						
Input voltage	f = 70 to 120 MHz, Pin 21 f = 120 to 160 MHz	V_{FMOSC} V_{FMOSC}	40 150			mV_{rms} mV_{rms}
AMOSCIN						
Input voltage	f = 0.6 to 35 MHz, Pin 23	V_{AMOSC}	40			mV_{rms}
WIBIN						
Input voltage	f = 120 to 180 MHz, Pin 22	V_{WB}	150			mV
3-wire bus EN, DA, CLK						
Input voltage HIGH LOW	Pins 6, 7 and 8	V_{BUS}	 2.0		 1.0	 V V
Clock frequency	Pin 8				1.0	MHz
Period of CLK HIGH LOW	Pin 8	 t_H t_L	 250 250			 ns ns
Rise time EN, DA, CLK	Pins 6, 7 and 8	t_R			400	ns
Fall time EN, DA, CLK	Pins 6, 7 and 8	t_F			100	ns
Set-up time		t_S	100			ns
Hold time EN	Pins 6 and 7	t_{HEN}	250			ns
Hold time DA	Pins 7 and 8	t_{HDA}	0			ns

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
OSCIN0A, OSCIN0B						
Oscillator voltage	f = 19 to 30 MHz, Pins 2 and 3, see application circuit page 15	V_{OSC}		tbd		mV_{rms}
OSCIN1A, OSCIN1B						
	f = 19 to 30 MHz Pins 26, 27					
PD0, PD1						
Output current 1 Output current 2 Output current 3 Output current 4 Leakage current	 Pins 4 and 25	$\pm I_{PD}$ $\pm I_{PDL}$		25 100 500 2000	 20	µA µA µA µA nA
PDFM						
Output current 1 Output current 2 Output current 3 Output current 4 Leakage current	Pin 19	$\pm I_{PDFM}$ I_{PDFML}		25 100 500 2000	 20	µA µA µA µA nA
PDO0, PDO1						
Saturation voltage LOW HIGH	Pins 5 and 24 I = 15 mA V_{SATH-} (V_A-V_{PDOFM})	 V_{SATL} V_{SATH}		 200	 400 500	 mV mV
PDOFM						
Saturation voltage LOW HIGH	Pin 18 I = 15mA V_{SATH-} (V_A-V_{PDOFM})	 V_{SATL} V_{SATH}		 200	 400 500	 mV mV
HSSW						
Input voltage LOW HIGH	Pin 9	V_{HSSW}	 2.0		 1.0	 V V
LD (open drain)						
Output voltage LOW	Pin 10 I = 1 mA	V_{LD}			 500	 mV
SWO1, SWO2, SWO3,SWO4 (open drain)						
Output voltage LOW Output leakage current HIGH	Pins 11, 12, 13 and 14 I = 1 mA $V_{11} = V_{12} = V_{13} = V_{14}$ = 8.5 V	 V_{SWOL} I_{OHL}		 100	 400 100	 mV nA

Data Transfer for 3-Wire Bus

MSB		Byte 3					LSB	MSB	Byte 2							MSB	Byte 1						LSB
Addr.		Status 0														R00-divider							
0	0	IPD0 1/2	IPD0 3/4	PD 0 +/–	SWO 4	SWO 3	SWO 2	SWO 1	x	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

MSB		Byte 2					LSB	MSB	Byte 1						LSB
Addr.		N0-divider													
0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

MSB		Byte 3					LSB	MSB	Byte 2						LSB	MSB	Byte 1						LSB
Addr.		Status 1															R01-divider							
0	1	IPD1 1/2	IPD1 3/4	PD1 +/–	AM FM	WB	x	x	x	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

MSB		Byte 2					LSB	MSB	Byte 1						LSB
Addr.		N1-divider													
1	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Main PLL

MSB		Byte 1					LSB
Addr.		Status 1					
0	0	M0 2^{2}	M0 2^{1}	M0 2^{0}	M1 2^{2}	M1 2^{1}	M1 2^{0}

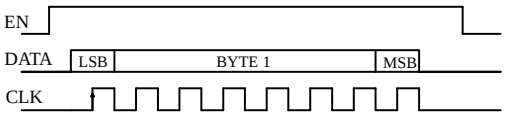
Addr		Status 2					
0	1	HSS	x	IPDM 1/2	IPDM 3/4	PDM +/–	TSTAN

Addr.		Status 3 only for test-mode					
1	1	T1	T2	T3	T4	T5	T6

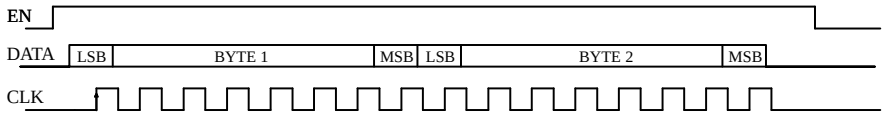
Figure 14.

8-bit command

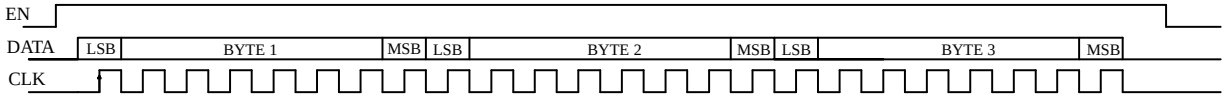
96 11803



16-bit command



24-bit command



e.g., Sub-PLL0

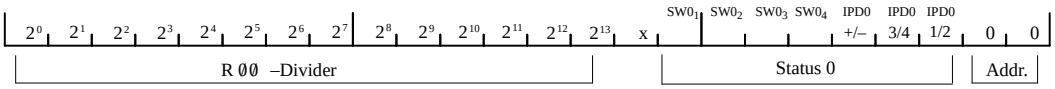


Figure 15.

Bus-Timing

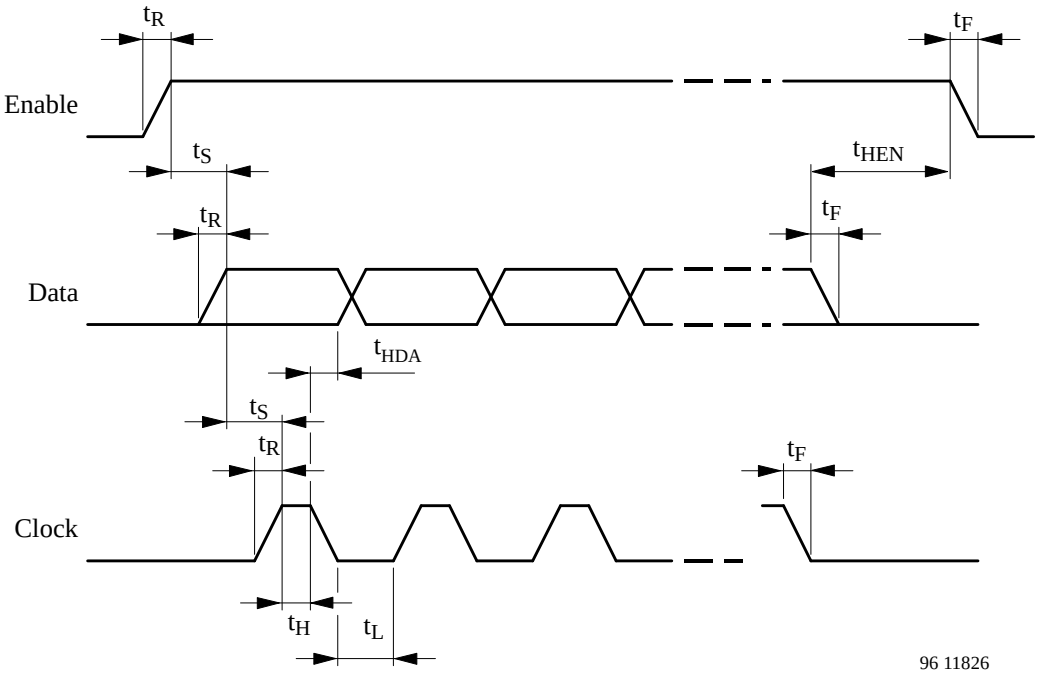


Figure 16.

Block Diagram with External Circuit

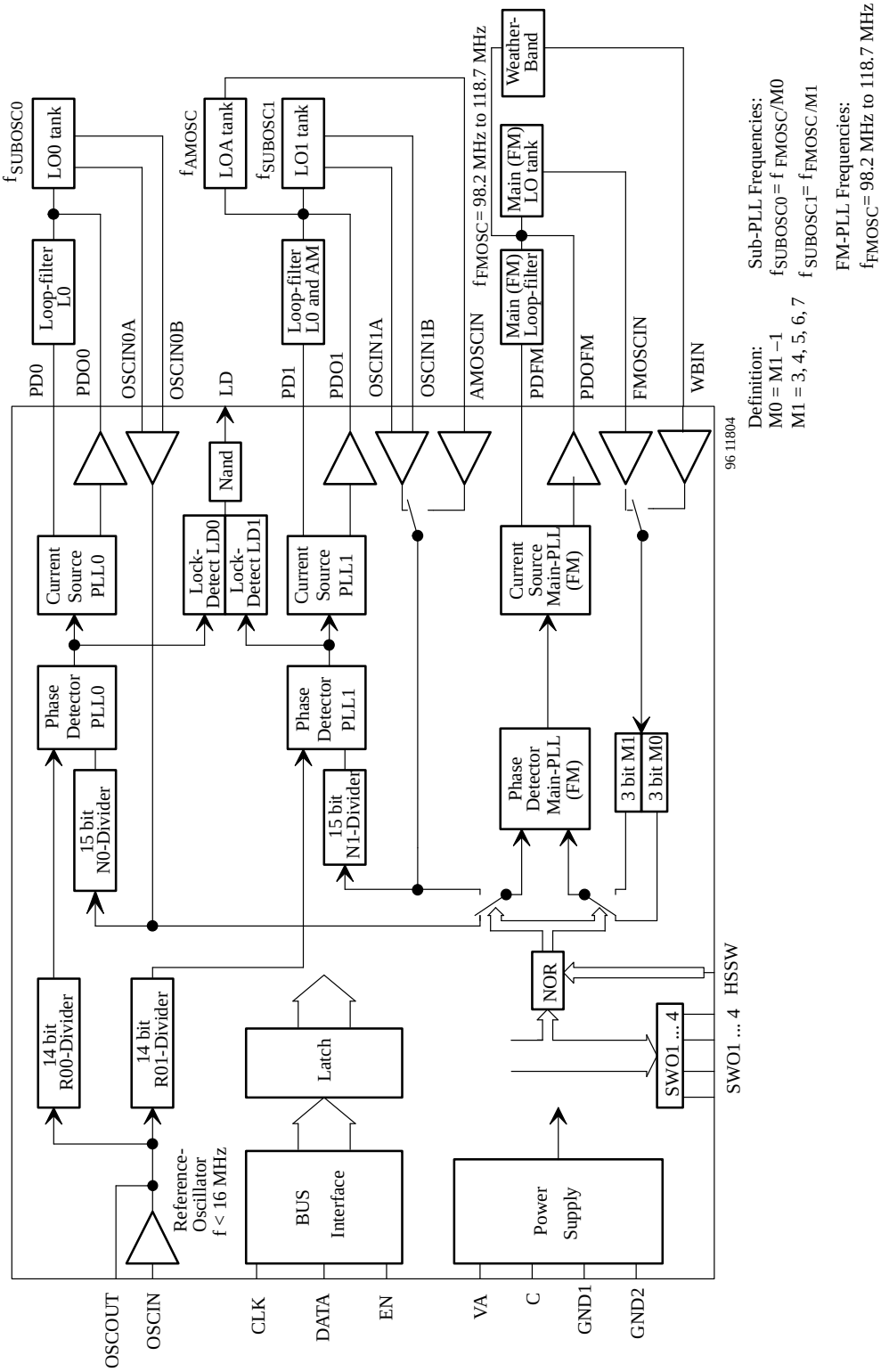


Figure 17.

Application Circuit

Best performance of this apllication circuit can be only achieved on the following conditions:

FM oscillator frequency range: 98.2 to 118.7 MHz
$F_{STEP/MAIN}$ = 50 kHz, IPDM = 100 µA

M0 = 5 → $f_{SUBOSC0}$: 19.64 to 23.74 MHz
$f_{STEP/SUB0}$ = 10 kHz, IPD0 = 2000 µA
M! = 4 → $f_{SUBOSC0}$: 24.55 to 29.675 MHz
$f_{STEP/SUB1}$ = 12.5 kHz, IPD1 = 2000 µA

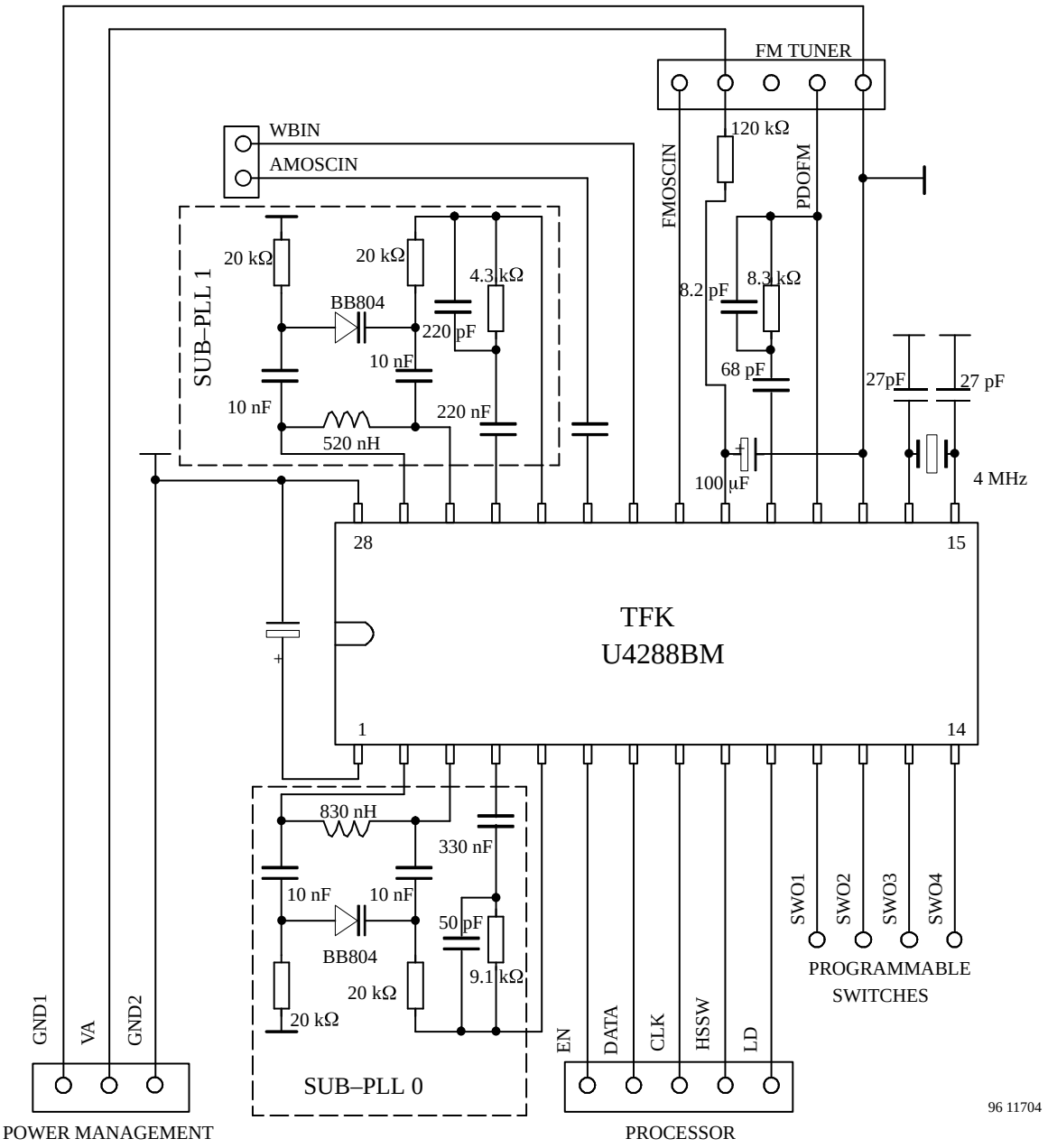
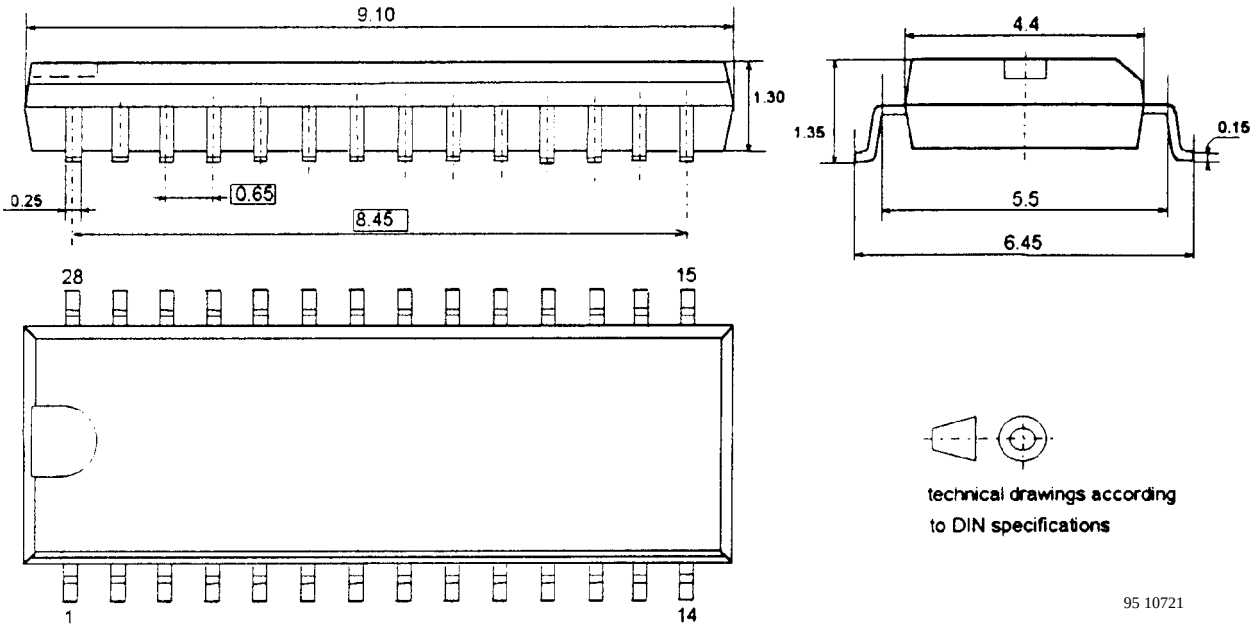


Figure 18.

Ordering and Package Information

Extended Type Number	Package	Remarks
U4288BM-AFS	SSO28 plastic	
U4288BM-AFSG3	SSO28 plastic	Taping according IEC-286-3

Package SSO28
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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