
Low Power FM Transmitter / Synthesizer System 26 to 50 MHz

Description

Radio frequency IC for analog cordless telephone application in 26/50 MHz band (CTO standard). The IC performs full duplex communication. The transmitting and receiving frequency are depending on whether the IC is used in the handset or in the base station.

Frequency converter U3550BM comprise a FM transmitter with switchable output power and first receiver mixer in the same unit. A two wire bus interface can be used for the frequency control as well as for switching the transmitter power amplifier and the receiver. Fine frequency adjust of reference quartz oscillator is programmable.

The receive part is designed for a double conversion

architecture. The incoming radio frequency signal will be filtered and amplified (U3550BM) before reaching the first mixer. At this stage the RF signal will be converted down to the first intermediate frequency (10.7 MHz) by using a local adjustable oscillator (VCO3). The frequency of this oscillator is controlled by PLL.

The transmitter part contains two PLL controlled VCO's. The frequency modulation is accomplished by superposing the incoming audio signal on the first PLL control voltage. Finally frequency is a product of mixing VCO1 with local oscillator (VCO3). The FM modulated carrier is amplified by external power amplifier before entering the output filter and the antenna connector.

Features

- All oscillators and PLLs maximally integrated
- All functions and channel selection controllable by serial bus
- Receive mixer1 with integrated image-rejection
- Up to 25 channels selectable depending on CTO standard
- Integrated oscillator circuit with external crystal 11.15 MHz
- Programmable carrier modulation frequency

Package: SO28

Application

CTO (USA, France, Spain, Netherlands, Portugal, Korea, Taiwan, New Zealand)
Narrow band voice and data transmitting / receiving systems

Block Diagram

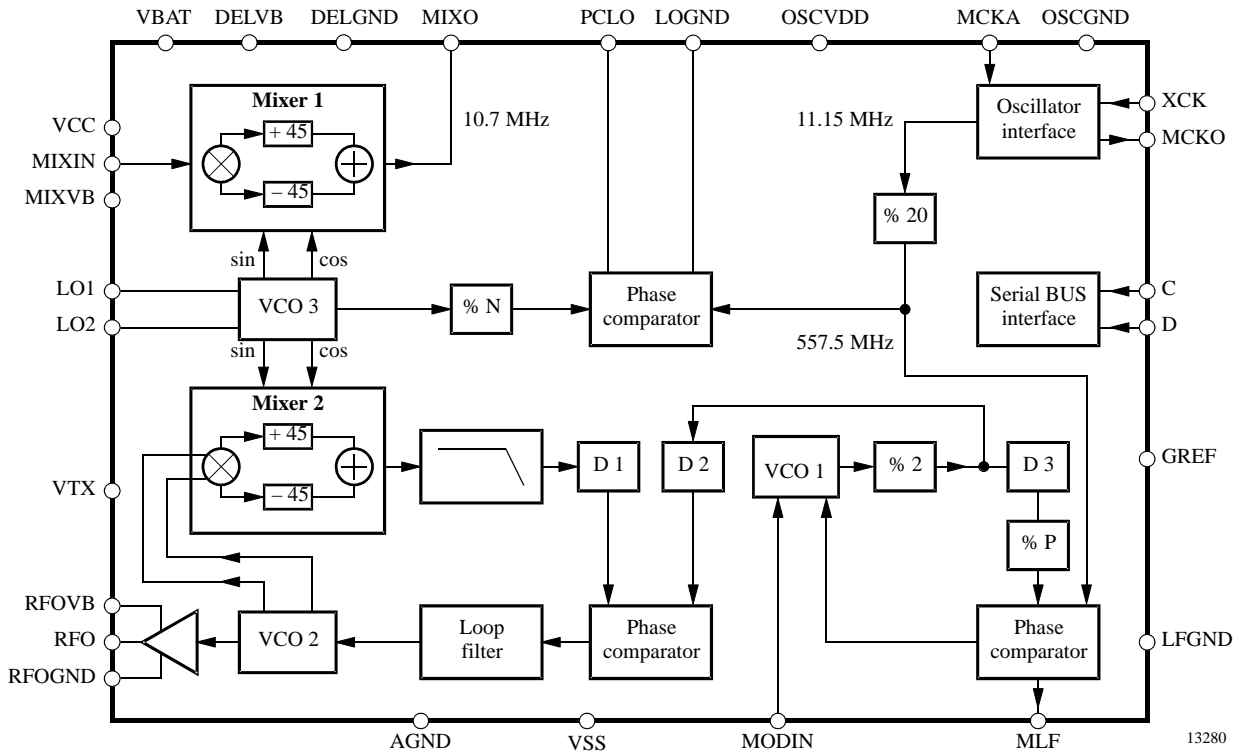


Figure 1. Block diagram

Pin Description



Figure 2. Pinning

Pin	Symbol	Function
1	MCKO	Clock output for peripherals
2	D	Data input of serial bus
3	C	Clock line of serial bus
4	OSCGND	Oscillator ground
5	XCK	Oscillator input (11.15 MHz)
6	OSCVDD	Oscillator supply input
7	DELVB	Phase correction VCO3 supply input
8	DELGND	Phase correction VCO3 ground
9	GREF	Voltage reference for internal current sources
10	MIXIN	Mixer input
11	MIXVB	Mixer supply input
12	MIXO	Mixer output
13	LO1	Tank elements for LO are connected to these pins
14	LO2	
15	PCLO	Phase comparator PLL3 output
16	LOGND	VCO3 ground
17	RFOGND	RF transmit output ground
18	RFO	RF transmit output
19	RFOVB	Power supply input of RF transmit output buffer
20	VTX	Power supply output of RF external power amplifier
21	AGND	Analog ground
22	VBAT	Power supply of analog part
23	MLF	Modulator loop filter
24	LFGND	Modulator loop filter ground
25	MODIN	Modulator input signal
26	MCKA	Peripherals clock output adjustment
27	VSS	Digital ground
28	VCC	Power supply of digital part

Adjustments for the VCOs

To be able to use a wide frequency range for the VCOs (i.e., VCO2 26.3 to 49.9 MHz) the internal VCOs have a rough adjust and a fine adjust to increase the frequency range given by the phase comparator.

The 4 rough adjusts for each VCO (3 used in VCO1) are correlated with the country setting. For every country there are two sets of VCO rough adjust settings, one for the base and one for the handset. See tables at channels frequencies and dividers.

To compensate the variation in production there is a fine adjust with 32 steps for each VCO. These fine adjusts could be set manually (for test purposes) or set by the automatically mode. Theoretically the sign of the changing (increase/ decrease when the voltage of the phase comparator is to high) is selectable, but we need value 1 () in all cases.

Setting normal conditions VCO1:

EAF A1 = 1, automatic fine adjust VCO1 enabled
SAFA1 = 1, sign of auto fine adjustment VCO1=1.

Setting for VCO2 identical.

For VCO3 there is no internal adjustment.

Speed-Up of the Modulator Loopfilter

To have a fast locking time for the modulator loop there is a precharge and a speed-up mode for the external loopfilter.

During receive mode (VCO3 enabled, VCO1 disabled) the modulator loopfilter is precharged to 1.25 V.

During the first 30 ms after enabling VCO1 the modulator phase comparator is in speed-up mode. In this mode the current of the phase comparator which charges the loop filter is much larger than in normal mode. The duration of the speed-up mode depends on the number of oscillator clock cycles.

Table 1. Clock output values

Level on MCKA	0 to 7% VCC	13% to 27% VCC	33% to 47% VCC	53% to 67% VCC	73% to 87% VCC	93% to VCC
Level on MCKA for VCC = 3.6 V	0 to 0.25	0.47 to 0.97	1.19 to 1.69	1.91 to 2.41	2.63 to 3.13	3.35 to 3.6
Corresponding divider	X	6	4	3	2	1
Corresponding clock on MCK0 (MHz)	No output	1.858	2.7875	3.716	5.575	11.15

Duration Adjustment of the Antibacklash Signals

The phase comparators of the modulator- and the mixer-loop has a 2 bit adjustment for the duration of the up- and down pulses when the loop is locked (antibacklash).

Setting all the bits (AMOD[2:1], AMIX[2:1]) to 0 give the best results.

In the phase correction block of VCO3 is a threshold adjustment of two bits TLO[2:1]. Setting these bits in all cases to 0 give the best results.

All the values and limits of the data sheet referred to this settings, unless otherwise specified.

Adjustment of the Modulator Gain

To fulfill the different demands of the different countries three conversion gains of the modulator are selectable by the bits GMOD[1:0].

Country settings see tables at channels frequencies and dividers. Ranges see electrical characteristics at RF transmitter.

Clock Output Divider Adjustment

The MCKO pin is a clock output which is derived from the crystal oscillator. It can be used to drive a microprocessor or other remote component and thereby reduce the number of crystal required.

The crystal oscillator frequency can be divided by an integer value: 1, 2, 3, 4, 6 or switched off.

The divider value is adjusted by an analog level on the MCKA pin.

Table 1 shows the clock output value on MCKO for different divider values and the corresponding level required on MCKA.

Crystal oscillator = 11.15 MHz.

Logical Part Dividers

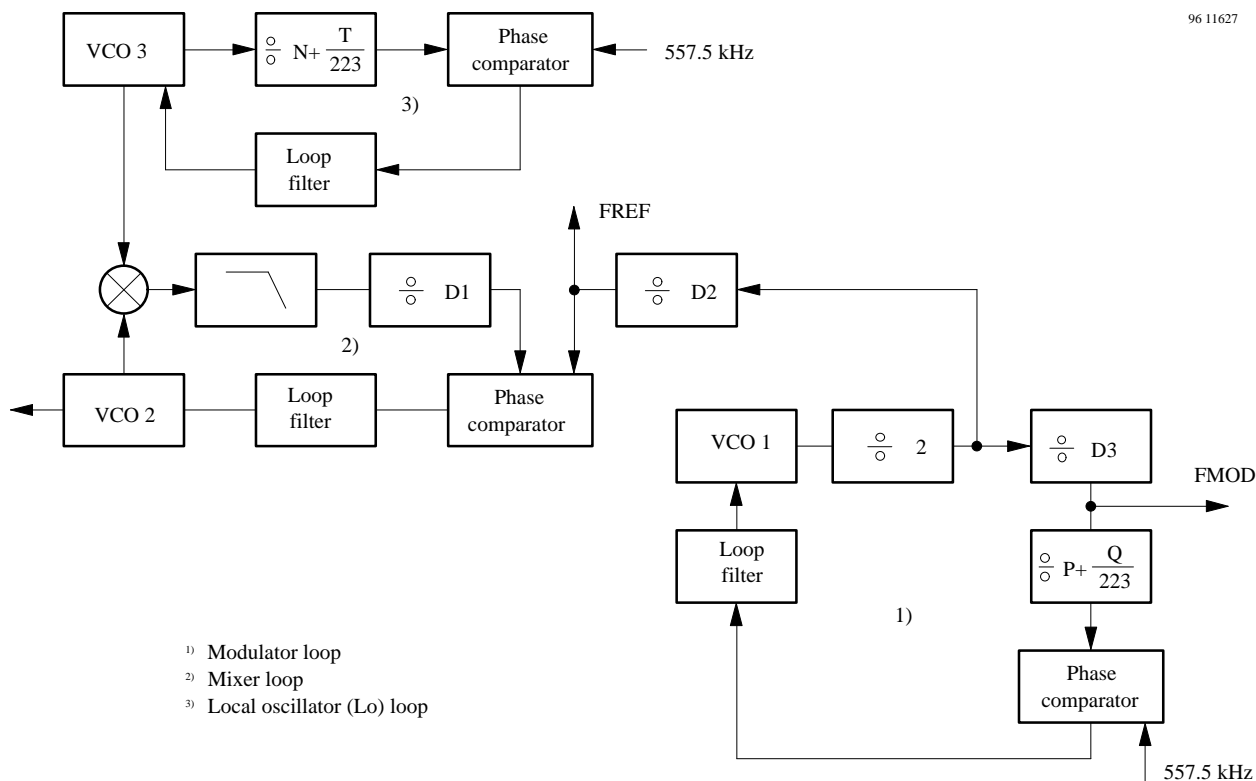


Figure 3.

Integer Dividers

	D1	D2	D3	F _{REF} (MHz)	F _{MOD} (MHz)
France	4	8	2	1.075	4.3
Spain	2	8	4	0.9	1.8
Netherlands	2	8	4	0.9	1.8
Portugal	2	8	4	0.625	1.25
USA (channels 1 to 10)	8	8	1	0.955	7.64
USA (new channels)	6	6	1	0.943	5.66
Taiwan	8	8	1	0.9625	7.70
New Zealand	4	8	2	0.5875	4.70
Korea	8	8	1	0.955	7.64

Note: For France, Spain, Netherlands, Portugal, Taiwan and New Zealand F_{REF} and F_{MOD} don't change when the channel changes, instead of the USA and Korea: F_{REF} and F_{MOD} are varying according to the channel number. For all countries F_{REF} and F_{MOD} are the same for base set and handset.

Fractional Dividers

Fractional dividers have been chosen in order to increase reference frequency of the modulator and local oscillator PLLs.

1. Modulator PLL

$$557.5 \text{ kHz} = F_{\text{MOD}} / \left(P + \frac{Q}{223} \right)$$

P: integer part of the fractional divider
Q: fractional part of the fractional divider

$$Q = 223 \times \left(\frac{F_{\text{MOD}}}{557.5 \text{ kHz}} - P \right)$$

$$223 = \frac{557.5 \text{ kHz}}{2.5 \text{ kHz}}$$

The frequency step 2.5 kHz is a fraction of the reference frequency 557.5 kHz

In fact, the fractional divider, divide Q times by (P + 1) and (223 - Q) times by P during 223 cycles.

$$\rightarrow \frac{Q \times (P + 1) + (223 - Q)P}{223} = P + \frac{Q}{223}$$

For each cycle (F = 557.5 kHz) of comparison, the accumulator content is incremented by the Q value and the divider divides by the P value. When the accumulator value reach or exceed 223, the divider divides by the (P + 1) value. Then, the accumulator hold the excess value (accumulator value - 223). After 223 cycles, the right division has been executed.

2. Local Oscillator PLL

$$557.5 \text{ kHz} = FV_{\text{CO3}} / \left(N + \frac{T}{223} \right)$$

N: integer part of the fractional divider
T: fractional part of the fractional divider

$$T = 223 \times \left(\frac{FV_{\text{CO3}}}{557.5 \text{ kHz}} - N \right)$$

Same principle as in number 1.

Serial Bus Interface

The circuit is remoted by an external micro controller through the serial bus.

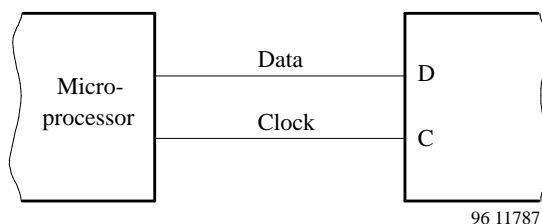
The data is an 12-bit word:

A0 - A3: address of the destination register (0 to 15)

D0 - D7: contents of register

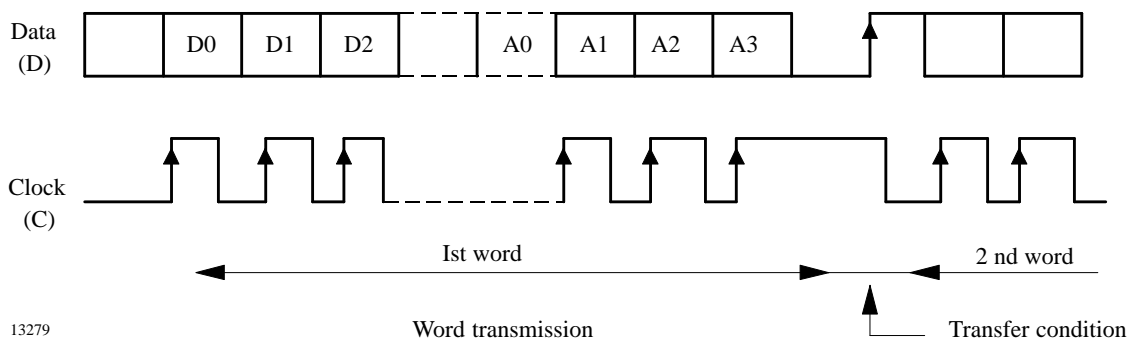
The data line must be stable when the clock is high and data must be serially shifted.

After 12 clock periods, the transfer to the destination register is (internally) generated by a low to high transition of the data line when the clock is high.



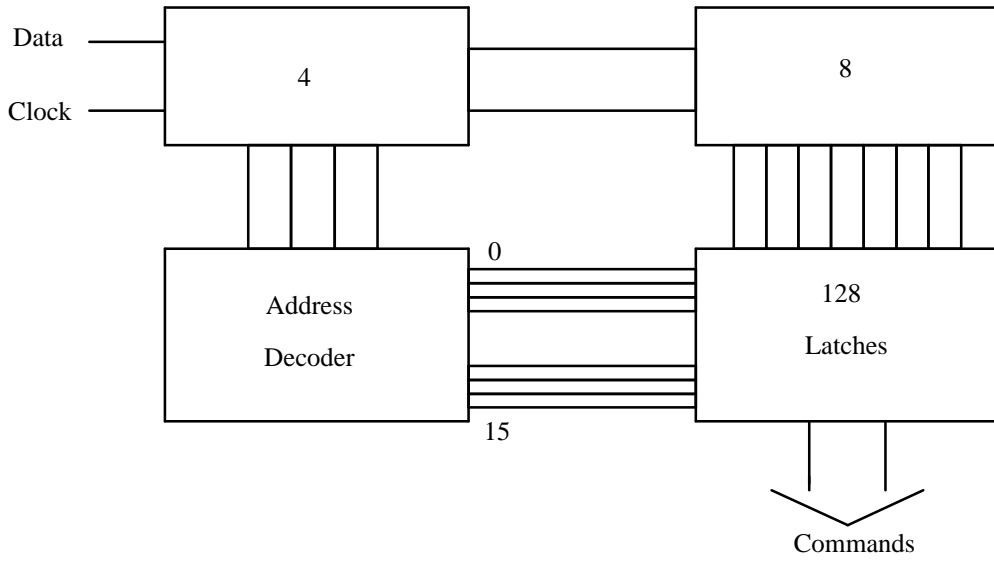
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Figure 4.



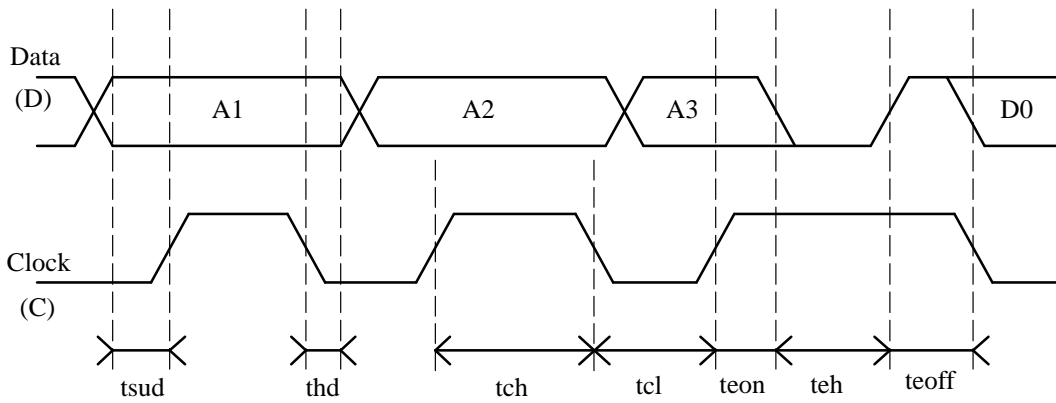
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Figure 5. Serial bus transmission



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Figure 6.



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Figure 7.

Content of Internal Registers

The registers have the following structure

D7	D6	D5	D4	D3	D2	D1	D0
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R0 – R4: reserved for U3500BM

R5: Gain VCO2

free	free	KV23	KV22	KV21	M12	reserved U3500	
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KV2[3:1]: Gain VCO2

M12: Frequency of phase comparator MIXER loop

R6: Country setting bits

ETXO	M1CP	UDM1	IMIXI	GMOD1	GMOD0	free	free
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ETXO: Enable HF-transmit output

M1CP: Changes 1dB compression point of MIXER1

UDM1: Up-down mixing of MIXER1

IMIXI: Inverse PCMIX inputs

GMOD[1:0]: Modulation gain of VCO1

R7: Divider VCO3 fractional part

DV3F7	DV3F6	DV3F5	DV3F4	DV3F3	DV3F2	DV3F1	DV3F0
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DV3F [7:0]: Divider setting VCO3 fractional part

R8: Divider VCO1 fractional part

DV1F7	DV1F6	DV1F5	DV1F4	DV1F3	DV1F2	DV1F1	DV1F0
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DV1F [7:0]: Divider setting VCO1 fractional part

R9: Divider VCO3 integer part

DPC	DV3I6	DV3I5	DV3I4	DV3I3	DV3I2	DV3I1	DV3I0
-----	-------	-------	-------	-------	-------	-------	-------

DPC: Disables the phase correction function VCO3

DV3I [6:0]: Divider setting VCO3 integer part

R10: VCO1 setting

AMOD2	AMOD1	RA11	RA10	DV1I3	DV1I2	DV1I1	DV1I0
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AMOD[2:1]: Lengthening antibacklash signal modulator loop

RA1[1:0]: Rough adjustment VCO1

DV1I[3:0]: Divider setting VCO1 integer part

R11: Setting VCO2 and VCO3

TLO2	TLO1	FRMT	free	AMIX2	AMIX1	RA21
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TLO[2:1]: Threshold adjust of phase correction of local oscillator

FRMT: Output frequency range of MIXT

AMIX[2:1]: Lengthening antibacklash signal mixer loop

RA2[1:0]: Rough adjustment VCO2

R12: Divider for country setting, fine adjust oscillator

FAOS2	FAOS1	FAOS0	D31	D30	D20	D11	D10
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FAOS[2:0]: Oscillator fine adjust

D3[1:0]: Setting divider D3

D20: Setting divider D2

D1[1:0]: Setting divider D1

R13: VCO1 enable and fine adjust

EVCO1	SAFA1	EAFSA1	FA14	FA13	FA12	FA11	FA10
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EVCO1: Enable VCO1

SAFA1: Sign for automatic fine adjust VCO1

EAFSA1: Enable automatic fine adjust VCO1

FA1[4:0]: Fine adjust VCO1 for manual adjustment

R14: VCO2 enable and fine adjust

EVCO2	SAFA2	EAFSA2	FA24	FA23	FA22	FA21	FA20
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EVCO2: Enable VCO2 and MIXT

SAFA2: Sign for automatic fine adjust VCO2

EAFSA2: Enable automatic fine adjust VCO2

FA2 [4:0]: Fine adjust VCO2 for manual adjustment

R15: VCO3 enable and fine adjust

EVCO3	free	free	free	free	free	free	free
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EVCO3: Enable VCO3 and MIXER1

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	VSUP (*)		5.5	V
Junction temperature	T _j		+125	°C
Ambient temperature	T _{amb}	-25	+75	°C
Storage temperature	T _{stg}	-50	+125	°C
Power dissipation T _{amb} = 60°C	P _{tot}		520	mW
Thermal resistance Junction ambient	R _{thJA}		120	K/W

Electrical Characteristics

T_{amb} = +25°C; (*) VSUP: = VBAT = MIXVB = RFOVB = DELVB = VCC = OSCVDD; VSUP = 3.6 V; FMIXIN = 26.40 MHz, FDEV = ± 2.5 kHz; VMIXIN = 2.24 mVRMS; FRFO = 41.4 MHz; (Fh8) FMODIN = 1.0 kHz; VMODIN = 0.5 VRMS, Offset 1.5 V; VMCKA = VCC, all blocks disabled (ETXO = EVCO1 = EVCO2 = EVCO3 = 0); unless otherwise specified. Test circuit, see figure 8.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Operating voltage range			3.1	3.6	5.2	V
Operating current in inactive mode	VBAT = MIXVB = RFOVB = DELVB = 2.9 V OSCVDD = VCC = 0V				5	µA
Operating current in standby mode	VBAT = MIXVB = RFOVB = DELVB = VCC = OSCVDD = 3.6			1	1.4	mA
Operating current in RX mode	EVCO3 = 1			5		mA
Operating current in active mode without TX output	EVCO1 = EVCO2 = 1			12		mA
Operating current in active mode	ETXO = 1 no load at RFO			13	16	mA
RF transmitter						
MODIN input impedance				100	130	kΩ
RFO output impedance	Load = 200			300	390	Ω
RFO output voltage level	ETXO = 0; no load				0.3	V
Lowest operating frequency	France base channel 1 (Fb1) (2)			26.3125		MHz
Highest operating frequency	USA base channel 9 (US1b9) (2)			49.9900		MHz
TX conversion gain RFO - MODIN	Eb1: FRFO = 31.025 MHz US1b9: FRFO = 49.99 Hz Fh6: FRFO = 41.4375 MHz for VSUP = 3.1 V, to 5.2 V			5.7 3.42 2.85		kHZ/V kHZ/V kHZ/V
Demodulated distortion THD	Eb1: ΔF = 5.0 kHz Fh9: ΔF = 1.5 kHz for VSUP = 3.1 V, to 5.2 V				2	%
Residual modulation (4) on demodulated signal	Test cond. as THD measurement with psophometric filter					dB

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Spurious at RFO output (delta versus carrier)	a/ Fb6: FRFO = 26.375 MHz b/ US1h9: FRFO = 49.99 MHz $\Delta F = \pm 2.5$ kHz $\Delta F = \pm 12.5$ kHz $\Delta F = \pm 557.5$ kHz $\Delta F = \pm 1/2$ FMOD $\Delta F = \pm$ FMOD for VSUP = 3.1 V to 5.2 V		60			dBc
VTX output capability	ILOAD = 3 mA ΔV with and without load				0.5	V
VTX output leakage current	ETXO = 0; current to GND				1	μ A
PLLs VSUP = 3.1 and VSUP = 5.2 V						
Charge pump output voltage	EVCO 1 = 1 output high		2.38	2.5	2.63	V
Precharge voltage at the loopfilter	EVCO 3 = 1, EVCO 1 = 0		1.15	1.25	1.35	V
Charge pump output current in speed-up mode	EVCO 1 = 1 VMLF = 1.25 V output high		-400	-300	-200	μ A
Charge pump output current	VMLF = 1.25 V output low		4.3	6.2	8	μ A
	VMLF = 1.25 V output high		-8	-6.2	-4.3	μ A
Charge pump leakage current	VMLF = 1.25 V output tristate		-50		+50	nA
VCO1 gain	VMLF = 0 V then 2.5V			20.35		kHz/V
Receiver input mixer (MIX1)						
Input frequency range	EVCO3 = 1		20		50	MHz
Output frequency				10.7		MHz
Input resistance				3.0		k Ω
Input capacitor				3.5		pF
Output impedance	M1CP = 0			330		Ω
	M1CP = 1			130		Ω
Voltage gain on MIXO	M1CP = 0 M1CP = 1 for: Fb8: FLO = 30.7 MHz FRF11 = 20 MHz UDM1 = 1		6.7 8.5	9.5 12.1	12.3 15.7	dB dB
	Fb8: FLO = 30.7 MHz FRF21 = 41.4 MHz UDM1 = 0 US1h10: FLO = 57.67 MHz FRF31 = 46.97 MHz UDM1 = 1 for VSUP = 3.1 to 5.2 V					
Noise figure	BW = 1 MHz; 50 Ω input impedance			14	18	dB
Input compression point	M1CP = 0		-19	-17.7		dBm
	M1CP = 1 50 Ω input impedance		-16	-14.3		dBm

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Third order input intercept point	MICP = 0		-7	-5		dBm
	MICP = 1		-4	-2		dBm
Image frequency rejection	50 Ω input impedance FRF1 = 41.4 MHz FRF2 = 41.4125 MHz Input level 1 = -30 dBm Input level 2 = -30 dBm					
	Fb8: FLO = 30.7 MHz UDM1 = 0 FRF11 = 41.4 MHz FRF12 = 20 MHz (image)		30			dB
	Fb8: FLO = 30.7 MHz UDM1 = 0 FRF21 = 20 MHz FRF22 = 41.4 MHz (image)					
US1h10: FLO = 57.67 MHz UDM1 = 1 FRF31 = 46.97 MHz FRF32 = 68.37 MHz (image)						
LO to RF MIXO input isolation	Fb8: measuring FOL = 30.7 MHz				0.2	mV _{RMS}
LO to IF MIXO output isolation	Fb8: measuring FOL = 30.7 MHz				1.2	mV _{RMS}
Logical part						
Inputs: C, D, Low voltage input High voltage input Inputs: C, D, MCKA Input leakage current (0 < VI < VCC)		Vil Vih Ii	0.8*V CC -1		0.2*V CC 1	 μA
Input leakage current pin XCK (0 < VI < VCC)			-5		5	μA
Output impedance at MCKO			0.5		1.0	kΩ
Serial bus (figure 8) Data set-up time Data hold time Clock low time Clock high time Hold time before transfer condition Data low pulse on transfer condition Data high pulse on transfer condition		tsud thd tcl tch teon teh teoff	0.1 0 2 2 0.1 0.2 0.2			μs μs μs μs μs μs μs

(1) ISUP = IVBAT + IVCC + IMIXVB + IRFOVB + ODELVB + IOSCVDD

- (2) 1 -measure 11.5 MHz at MCKO pin
2 -measure FRFO at RFO pin
3 -see country channels

(4) Ratio between demodulated audio level with and without 1 kHz modulation

Fine Adjustment of the Oscillator Frequency

To set the frequency of the oscillator exact to 11.15 MHz, the frequency is adjustable in 8 steps, by adding 3 different internal capacities the frequency could be reduced.

Parameters	Test Conditions / Pins	Min.	Typ.	Max.	Unit
Oscillator frequency without reduction	FAOS (0:2) = 0		11.15		MHz
Changing of oscillator frequency with FOSC reduction	FAO2 FAO1 FAO0				Hz
	0 0 1		100		
	0 1 0		200		
	1 0 0		400		
	1 1 1		700		

Test Circuit

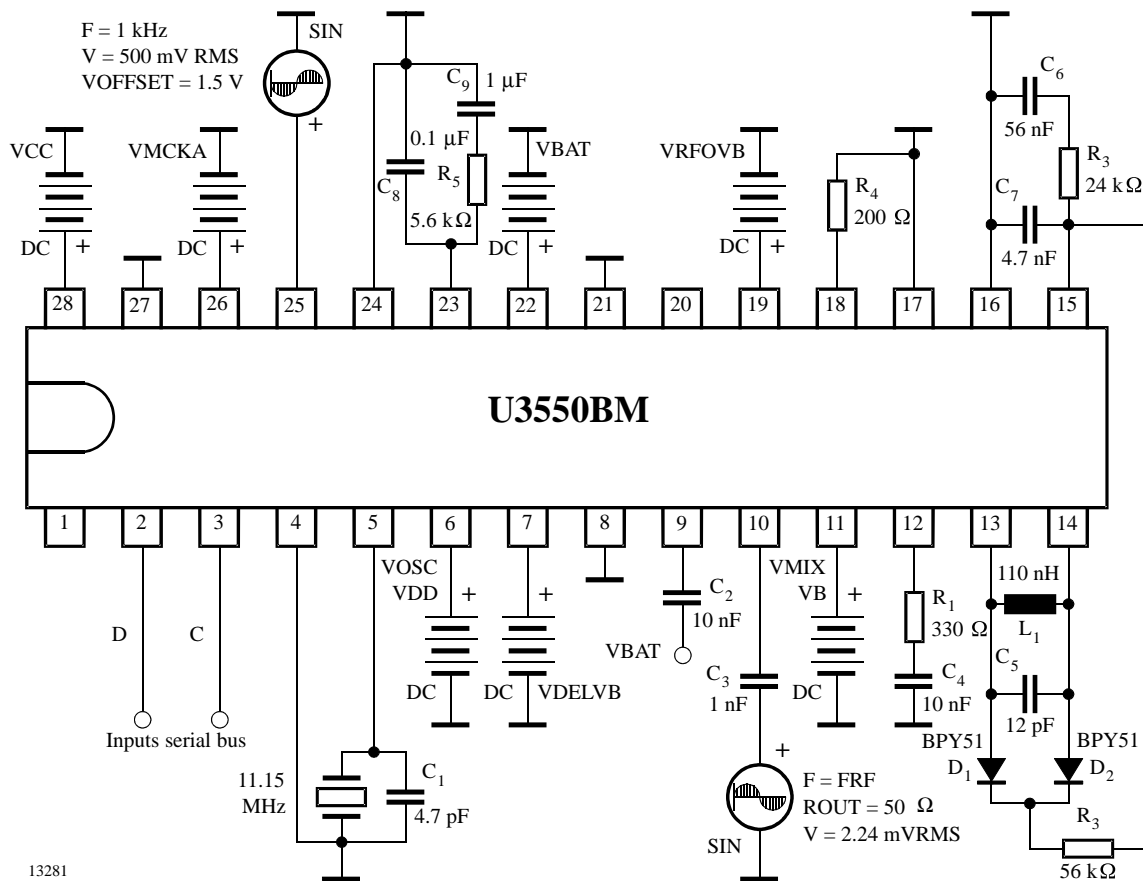


Figure 8. Test circuit

Channels Frequencies, Dividers and Country Settings

To meet all requirements of the different countries – France (F), Spain (E), Netherlands (NL), USA and Portugal (P), Korea, Taiwan, New Zealand – and modes – base (b), handset (h) – several bits have to be set which don't change for the different channels. These settings are called country settings.

To this country setting bits belong:

- Rough adjustments for 2 VCOs
- Setting of the 3 integer divider in the mixer and modulator loop
- Conversion gain adjustment of mixer loop
- Modulator gain
- Up-down mixing MIXER1 and transmit mixer
- Output range of MIXT

Name Registers	Function	Notes	
RA1[0:1]	Rough adjust VCO1	00: is highest frequency	3
RA2[0:1]	Rough adjust VCO2	00: is highest frequency	4
D1[0:1]	Integer divider D1	Division by 2, 4, 6, 8	4
D20	Integer divider D2	Division by 6, 8	2
D3[0:1]	Integer divider D3	Division by 1, 2, 4	3
KV[1:3]	Conversion gain mixer		6
GMOD[0:1]	Modulator gain	00: gain minimal	3
IMIXI	Up-down mixing Transmit-mixer	0: if fVCO2 lower than fVCO3	2
UDM1	Up-down mixing Mixer1	1: supra band active (handset)	2
FRMT	Output range MIXT	0: for VCO2-VCO3 < 6 MHz	2

Note: Setting the fractional dividers

For N, T, Q send the binary equivalent of the numbers given below.

For P (integer part of mixer loop) send the D2 complement (16 - P)

i.e, Fb1(P = 7, Q = 159 => integer: send 16 - P = 9, fractional: send 159)

France CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	00	11	11	1	01	100	01	0	0	0
Setting	max	min	4	8	2		mid	supra	infra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	41.3125	30.6125	54	203
2	41.3250	30.6250	54	208
3	41.3375	30.6375	54	213
4	41.3500	30.6500	54	218
5	41.3625	30.6625	55	0
6	41.3750	30.6750	55	5
7	41.3875	30.6875	55	10
8	41.4000	30.7000	55	15
9	41.4125	30.7125	55	20
10	41.4250	30.7250	55	25
11	41.4375	30.7375	55	30
12	41.4500	30.7500	55	35
13	41.4625	30.7625	55	40
14	41.4750	30.7750	55	45
15	41.4875	30.7875	55	50

France CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	00	01	11	1	01	101	01	1	0	0
Setting	max	high	4	8	2		mid	infra	infra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	26.3125	37.0125	66	87
2	26.3250	37.0250	66	92
3	26.3375	37.0375	66	97
4	26.3500	37.0500	66	102
5	26.3625	37.0625	66	107
6	26.3750	37.0750	66	112
7	26.3875	37.0875	66	117
8	26.4000	37.1000	66	122
9	26.4125	37.1125	66	127
10	26.4250	37.1250	66	132
11	26.4375	37.1375	66	137
12	26.4500	37.1500	66	142
13	26.4625	37.1625	66	147
14	26.4750	37.1750	66	152
15	26.4875	37.1875	66	157

France CT0 Modulation Loop Frequency and Divider

$F_{MOD} = 4.3 \text{ MHz}$, $P = 7$, $Q = 159$

Spain CT0 Base

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	10	00	1	11	100	10	1	0	0
Setting	min	low	2	8	4		high	infra	infra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	39.925	29.225	52	94
2	39.950	29.250	52	104
3	39.975	29.275	52	114
4	40.000	29.300	52	124
5	40.025	29.325	52	134
6	40.050	29.350	52	144
7	40.075	29.375	52	154
8	40.100	29.400	52	164
9	40.150	29.450	52	184
10	40.175	29.475	52	194
11	40.200	29.500	52	204
12	40.225	29.525	52	214

Spain CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[0:1]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	01	00	1	11	100	10	0	1	0
Setting	min	high	2	8	4		high	supra	supra	low

Channel frequencies and 1st LO dividers

Channel	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	31.025	41.725	74	188
2	31.050	41.750	74	198
3	31.075	41.775	74	208
4	31.100	41.800	74	218
5	31.125	41.825	75	5
6	31.150	41.850	75	15
7	31.175	41.875	75	25
8	31.200	41.900	75	35
9	31.250	41.950	75	55
10	31.275	41.975	75	65
11	31.300	42.000	75	75
12	31.325	42.025	75	85

Spain CT0 Modulation Loop Frequency and Divider

$F_{MOD} = 1.8 \text{ MHz}$, $P = 3$, $Q = 51$

Netherlands CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	10	00	1	11	100	10	1	0	0
Setting	min	low	2	8	4		high	infra	infra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	39.9375	29.2375	52	99
2	39.9625	29.2625	52	109
3	39.9875	29.2875	52	119
4	40.0125	29.3125	52	129
5	40.0375	29.3375	52	139
6	40.0625	29.3625	52	149
7	40.0875	29.3875	52	159
8	40.1125	29.4125	52	169
9	40.1375	29.4375	52	179
10	40.1625	29.4625	52	189
11	40.1875	29.4875	52	199
12	40.2125	29.5125	52	209

Netherlands CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	01	00	1	11	001	10	0	1	0
Setting	min	high	2	8	4		high	supra	supra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	31.0375	41.7375	74	193
2	31.0625	41.7625	74	203
3	31.0875	41.7875	74	213
4	31.1125	41.8125	75	0
5	31.1375	41.8375	75	10
6	31.1625	41.8625	75	20
7	31.1875	41.8875	75	30
8	31.2125	41.9125	75	40
9	31.2375	41.9375	75	50
10	31.2625	41.9625	75	60
11	31.2875	41.9875	75	70
12	31.3125	42.0125	75	80

Netherlands CT0 Modulation Loop Frequency and Divider

$$F_{MOD} = 1.8 \text{ MHz}, P = 3, Q = 51$$

USA CT0 Base Set

Country setting channel 1 –10 (USA1):

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	100	00	1	0	1
Setting	mid	max	8	8	1		low	infra	infra	high

Country setting new channels (channel 11 –25, UAS2):

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	01	10	0	00	110	01	1	0	0
Setting	mid	high	6	6	1		mid	infra	infra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	49.670	38.970	69	201
2	49.845	39.145	70	48
3	49.860	39.160	70	54
4	49.770	39.070	70	18
5	49.875	39.175	70	60
6	49.830	39.130	70	42
7	49.890	39.190	70	66
8	49.930	39.230	70	82
9	49.990	39.290	70	106
10	49.970	39.270	70	98

New Channels

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
11	48.760	38.06	68	60
12	48.840	38.14	68	92
13	48.860	38.16	68	100
14	48.920	38.22	68	124
15	49.020	38.32	68	164
16	49.080	38.38	68	188
17	49.100	38.40	68	196
18	49.160	38.46	68	220
19	49.200	38.50	69	13
20	49.240	38.54	69	29
21	49.280	38.58	69	45
22	49.360	38.66	69	77
23	49.400	38.70	69	93
24	49.460	38.76	69	117
25	49.500	38.80	69	133

USA CT0 Handset

Country setting channel 1 –10 (USA1):

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	100	00	0	1	1
Setting	mid	max	8	8	1		low	supra	supra	high

Country setting new channels (channel 11 –25, USA2):

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	10	0	00	110	01	0	1	0
Setting	mis	max	6	6	1		mid	supra	supra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	46.610	57.31	102	178
2	46.630	57.33	102	186
3	46.670	57.37	102	202
4	46.710	57.41	102	218
5	46.730	57.43	103	3
6	46.770	57.47	103	19
7	46.830	57.53	103	43
8	46.870	57.57	103	59
9	46.930	57.63	103	83
10	46.970	57.67	103	99

New Channels

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
11	43.720	54.42	97	137
12	43.740	54.44	97	145
13	43.820	54.52	97	177
14	43.840	54.54	97	185
15	43.920	54.62	97	217
16	43.960	54.66	98	10
17	44.120	54.82	98	74
18	44.160	54.86	98	90
19	44.180	54.88	98	98
20	44.200	54.90	98	106
21	44.320	55.02	98	154
22	44.360	55.06	98	170
23	44.400	55.10	98	186
24	44.460	55.16	98	210
25	44.480	55.18	98	218

USA CT Modulation Loop Frequencies and Dividers

N Channel	P	Q	F _{MOD} (MHz)
1	13	157	7.640
2	13	95	7.485
3	13	105	7.510
4	13	157	7.640
5	13	123	7.555
6	13	157	7.640
7	13	157	7.640
8	13	157	7.640
9	13	157	7.640
10	13	181	7.700

New Channels

N Channel	P	Q	F _{MOD} (MHz)
11	10	34	5.66
12	10	10	5.60
13	10	34	5.66
14	10	18	5.62
15	10	10	5.60
16	10	2	5.58
17	10	58	5.72
18	10	50	5.70
19	10	42	5.68
20	10	34	5.66
21	10	66	5.74
22	10	50	5.70
23	10	50	5.70
24	10	50	5.70
25	10	42	5.68

Portugal CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	01	10	00	1	11	010	10	1	0	0
Setting	mid	low	2	8	4		high	infra	infra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	37.000	26.300	47	39
2	37.025	26.325	47	49
3	37.050	26.350	47	59
4	37.075	26.375	47	69
5	37.100	26.400	47	79
6	37.125	26.425	47	89
7	37.150	26.450	47	99
8	37.175	26.475	47	109
9	37.200	26.500	47	119
10	37.225	26.525	47	129
11	37.250	26.550	47	139
12	37.275	26.575	47	149

Portugal CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	01	00	1	11	001	10	0	0	0
Setting	min	high	2	8	4		high	supra	infra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	27.550	38.250	68	136
2	27.575	38.275	68	146
3	27.600	38.300	68	156
4	27.625	38.325	68	166
5	27.650	38.350	68	176
6	27.675	38.375	68	186
7	27.700	38.400	68	196
8	27.725	38.425	68	206
9	27.750	38.450	68	216
10	27.775	38.475	69	3
11	27.800	38.500	69	13
12	27.825	38.525	69	23

Portugal CT0 Modulation Loop Frequency and Divider

$$F_{MOD} = 1.25 \text{ MHz}, P = 2, Q = 54$$

Taiwan CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	110	01	1	1	1
Setting	min	max	8	8	1		low	infra	supra	higher

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	48.2500	37.5500	67	79
2	48.2750	37.5750	67	89
3	48.3000	37.6000	67	99
4	48.3250	37.6250	67	109
5	48.3500	37.6500	67	119
6	48.3750	37.6750	67	129
7	48.4000	37.7000	67	139
8	48.4250	37.7250	67	149
9	48.4500	37.7500	67	159
10	48.4750	37.7750	67	169

Taiwan CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	110	00	0	1	1
Setting	min	max	8	8	1		low	supra	supra	high

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	45.2500	55.9500	100	80
2	45.2750	55.9750	100	90
3	45.3000	56.0000	100	100
4	45.3250	56.0250	100	100
5	45.3500	56.0500	100	120
6	45.3750	56.0750	100	130
7	45.4000	56.1000	100	140
8	45.4250	56.1250	100	150
9	45.4500	56.1500	100	160
10	45.4750	56.1750	100	170

Taiwan CT0 Modulation Loop Frequency and Divider

$FMOD = 7.70 \text{ MHz}$, $P = 13$, $Q = 181$

New Zealand CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	00	01	11	1	01	110	01	1	0	0
Setting	max	high	4	8	2		mid	infra	infra	low

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
11	40.2500	29.5500	53	1
12	40.2750	29.5750	53	11
13	40.3000	29.6000	53	21
14	40.3250	29.6250	53	31
15	40.3500	29.6500	53	41
16	40.3750	29.6750	53	51
17	40.4000	29.7000	53	61
18	40.4250	29.7250	53	71
19	40.4500	29.7500	53	81
20	40.4750	29.7750	53	91

New Zealand CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	00	01	11	1	01	101	01	0	1	0
Setting	max	high	4	8	2		mid	supra	supra	low

Channel frequencies and 1st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
11	34.2500	44.9500	80	140
12	34.2750	44.9750	80	150
13	34.3000	45.0000	80	160
14	34.3250	45.0250	80	170
15	34.3500	45.0500	80	180
16	34.3750	45.0750	80	190
17	34.4000	45.1000	80	200
18	34.4250	45.1250	80	210
19	34.4500	45.1500	80	220
20	34.4750	45.1750	81	7

New Zealand CT0 modulation loop frequency and divider

$F_{MOD} = 4.70 \text{ MHz}$, $P = 8$, $Q = 96$

Korea CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	100	00	1	0	1
Setting	min	max	8	8	1		low	infra	infra	high

Channel frequencies and 1 st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	49.6700	38.9700	69	201
2	49.8450	39.1450	70	48
3	49.8600	39.1600	70	54
4	49.7700	39.0700	70	18
5	49.8750	39.1750	70	60
6	49.8300	39.1300	70	42
7	49.8900	39.1900	70	66
8	49.9300	39.2300	70	82
9	49.9900	39.2900	70	106
10	49.9700	39.2700	70	98
11	49.6950	38.9950	69	211
12	49.7100	39.0100	69	217
13	49.7250	39.0250	70	0
14	49.7400	39.0400	70	6
15	49.7550	39.0550	70	12

Korea CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	100	00	0	1	1
Setting	min	max	8	8	1		low	supra	supra	high

Channel frequencies and 1 st LO dividers

Channel Number	RX Channel Frequency (MHz)	1st LO-Frequency (MHz)	N	T
1	46.6100	57.3100	102	178
2	46.6300	57.3300	102	186
3	46.6700	57.3700	102	202
4	46.7100	57.4100	102	218
5	46.7300	57.4300	103	3
6	46.7700	57.4700	103	19
7	46.8300	57.5300	103	43
8	46.8700	57.5700	103	59
9	46.9300	57.6300	103	83
10	46.9700	57.6700	103	99
11	46.5100	57.2100	102	138
12	46.5300	57.2300	102	146
13	46.5500	57.2500	102	154
14	46.5700	57.2700	102	162
15	46.5900	57.2900	102	170

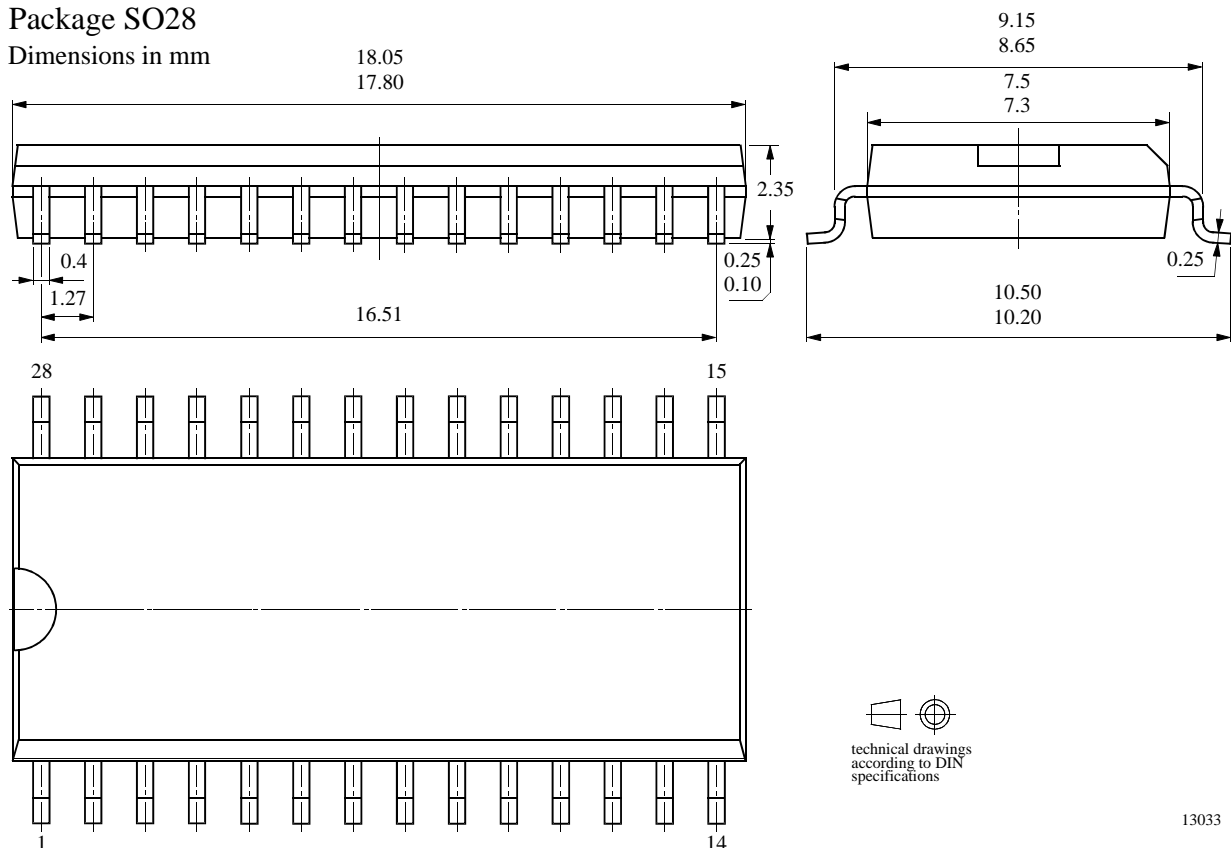
Korea CT Modulation Loop Frequencies and Dividers

N Channel	P	Q	F _{MOD} (MHz)
1	13	157	7.640
2	13	95	7.485
3	13	105	7.510
4	13	157	7.640
5	13	123	7.555
6	13	157	7.640
7	13	157	7.640
8	13	157	7.640
9	13	157	7.640
10	13	181	7.700
11	13	107	7.515
12	13	109	7.520
13	13	111	7.525
14	13	113	7.530
15	13	115	7.535

Package Information

Package SO28

Dimensions in mm



13033

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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