Microcontroller with TrackPoint™ microcode from IBM   TPM754

The Philips Semiconductors TPM754 is a small package, low cost, ROM-coded 80C51 with IBM®'s TrackPoint™ pointing algorithms and control code. TrackPoint is the result of years of human factors research and innovation at IBM. The result is a "velocity sensitive" pointing solution more efficient and easier to use than "position sensitive" devices such as the mouse, the trackball, or the touchpad.

IBM has licensed Philips Semiconductors to sell microcontrollers with TrackPoint code. By purchasing a TPM from Philips, the purchaser becomes a sub-licensee of Philips. The selling price of Philips' TPM includes the royalties for IBM's intellectual property, which Philips in turn pays to IBM. Customers for TPMs do not need to sign any licensing agreement with either IBM or Philips. This code is the intellectual property of IBM, which is covered by numerous patents, and must be treated accordingly.

The TPM754 contains IBM® TrackPoint™ code, a single module PCA, a 256×8 RAM, 21 I/O lines, two 16-bit counter/timers, a two-priority level interrupt structure, a full duplex serial channel, an on-chip oscillator, and an 8-bit D/A converter.

For identical device without TrackPoint code, see the 8XC754 datasheet.
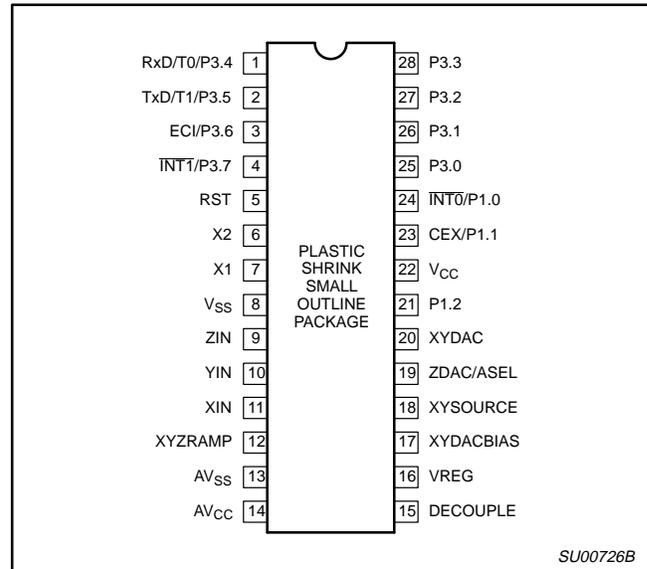
FEATURES

- 80C51-based architecture
- Small package sizes – 28-pin SSOP
- Power control modes:
  - Idle mode
  - Power-down mode
- 256×8 RAM
- Two 16-bit auto reloadable counter/timers
- Single module PCA counter/timer
- Full duplex serial channel
- Boolean processor
- CMOS and TTL compatible

PIN CONFIGURATION

RxD/T0/P3.4	1	28	P3.3
TxD/T1/P3.5	2	27	P3.2
ECI/P3.6	3	26	P3.1
$\overline{INT1}$/P3.7	4	25	P3.0
RST	5	24	$\overline{INT0}$/P1.0
X2	6	23	CEX/P1.1
X1	7	22	V_{CC}
V_{SS}	8	21	P1.2
ZIN	9	20	XYDAC
YIN	10	19	ZDAC/ASEL
XIN	11	18	XYSOURCE
XYZRAMP	12	17	XYDACBIAS
AV_{SS}	13	16	VREG
AV_{CC}	14	15	DECOUPLE

PLASTIC SHRINK SMALL OUTLINE PACKAGE

SU00726B

ORDERING INFROMATION

ORDERING CODE	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
PTPM754 DB	0 to +70, 28-pin Shrink Small Outline Package	3.5 to 12MHz	SOT341-1

For compatible pointing device, contact:

COMPANY	CONTACT	TELEPHONE
Bokam Engineering	Ms. Jane Kamenster	(714)513-2200
CTS Corporation	Mr. Dave Poole	(219)589-7169

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SCHEMATIC OF TRACKPOINT SYSTEM
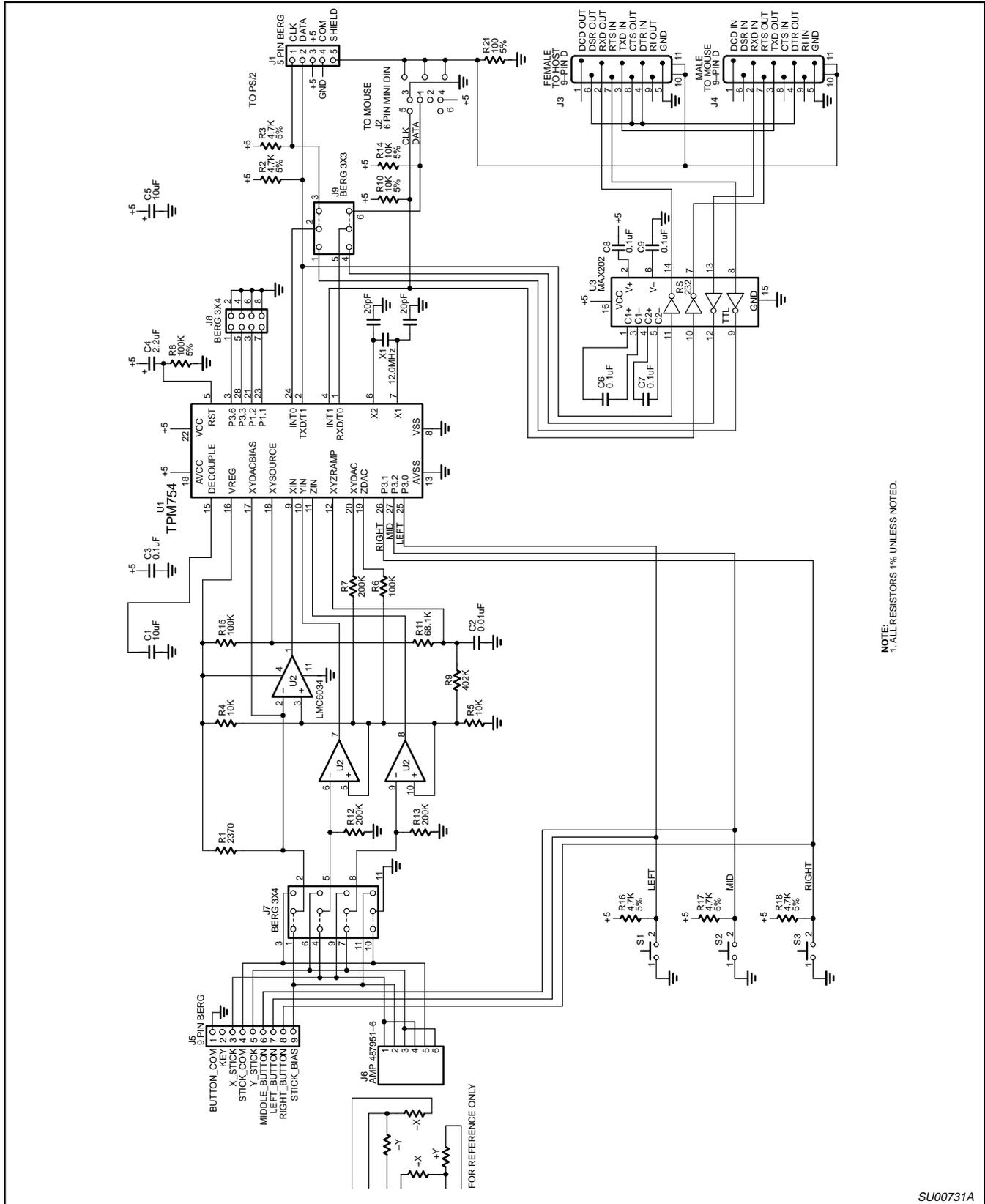
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PIN DESCRIPTION

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
V_{SS}	8	I	**Circuit Ground Potential.**
V_{CC}	22	I	**Supply voltage during normal, idle, and power-down operation.**
P1.0–P1.2	21, 23, 24	I/O	**Port 1:** Port 1 is a 3-bit bidirectional I/O port with internal pull-ups on P1.0 and P1.1. Port 1 pins that have 1s written to them can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups (P1.0, P1.1). (See DC Electrical Characteristics: I_{IL}). Port 1 also serves the special function features listed below (Note: P1.0 does **not** have the strong pullup that is on for 2 oscillator periods.):
	24	I	$\overline{INT0}$ **(P1.0):** External interrupt 0.
	23	O	**CEX (P1.1):** PCA clock output.
P3.0–P3.7	1–4, 25–28	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). (Note: P3.5 does **not** have the strong pullup that is on for 2 oscillator periods.)
			Port 3 also serves the special function as listed below:
	3	I	**ECI (P3.6):** External PCA clock input.
	1	I	**RxD/T0 (P3.4):** Serial port receiver data input. Timer 0 external clock input.
	4	I	$\overline{INT1}$**:** External interrupt 1.
	2	I	**TxD/T1 (P3.5):** Serial port transmitter data. Timer 1 external clock input.
RST	5	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running resets the device. **(NOTE: The TPM754 does not have an internal reset resistor.)**
X1	7	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
X2	6	O	**Crystal 2:** Output from the inverting oscillator amplifier.
AV_{CC} [1]	14	I	**Analog supply voltage and reference input.**
AV_{SS} [1]	13	I	**Analog supply and reference ground.**
ZIN	9	I	**ZIN:** Input to analog multiplexer.
YIN	10	I	**YIN:** Input to analog multiplexer.
XIN	11	I	**XIN:** Input to analog multiplexer.
XYZRAMP	12	O	**XYZRAMP:** Provides a low impedance pulldown to V_{SS} under S/W control.
DECOUPLE	15	O	**DECOUPLE:** Output from regulated supply for connection of decoupling capacitors.
VREG	16	O	**VREG:** Provides regulated analog supply output.
XYDACBIAS	17	O	**XYDACBIAS:** Provides source voltage for bias of external circuitry.
XYSOURCE	18	O	**XYSOURCE:** Provides source voltage from regulated analog supply.
ZDAC	19	O	**ZDAC:** Switchable output from the internal DAC.
XYDAC	20	O	**XYDAC:** Non-switchable output from the internal DAC.

NOTE:
1. AV_{SS} (reference ground) must be connected to 0V (ground). AV_{CC} (reference input) cannot differ from V_{CC} by more than ±0.2V, and must be in the range 4.5V to 5.5V.

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OSCILLATOR CHARACTERISTICS

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

IDLE MODE

The TPM754 includes the 80C51 power-down and idle mode features. In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals except the D/A stays active. The functions that continue to run while in the idle mode are the timers and the interrupts. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset. Upon powering-up the circuit, or exiting from idle mode, sufficient time must be allowed for stabilization of the internal analog reference voltages before a D/A conversion is started.

I/O Ports

The I/O pins provided by the TPM754 consist of port 1 and port 3.

Port 1

Port 1 is a 3-bit bidirectional I/O port and includes alternate functions on some pins of this port. Pins P1.0 and P1.1 are provided with internal pullups while the remaining pin (P1.2) has an open drain output structure. The alternate functions for port 1 are:

$\overline{INT0}$ – External interrupt 0.
CEX – PCA clock output.

Port 3

Port 3 is an 8-bit bidirectional I/O port structure.

The alternate functions for port 3 are:

RxD – Serial port receiver data input.
T1 – Timer 1 external clock input.
$\overline{INT1}$ – External interrupt 1.
TxD – Serial port transmitter data.
T0 – Timer 0 external clock input.
ECI – PCA external clock input.

Analog Section

The analog section of the TPM754, shown in Figure 1, consists of four major elements: a bandgap referenced voltage regulator, an 8-bit DAC, an input multiplexer and comparator, and a low impedance pulldown device.

The bandgap voltage regulator uses the AV_{CC} pin as its supply and produces a regulated output on the VREG pin. The regulator also supplies the analog supply voltage for the DAC. The regulator may be switched on/off by means of the AC1 bit in the analog control register (ACON0). The regulator output may also be supplied to the XYDACBIAS and XYSOURCE pins by means of bits AC3 and AC4, respectively. The DECOUPLE pin is provided for decoupling the regulator output.

The DAC is an 8-bit device and its output appears on the XYDAC pin. In addition, the DAC output may also be routed to the ZDAC pin by means of bit AC6 in the ACON0 register. The DAC output is not buffered, so external load impedances should be taken into consideration when using either of these outputs.

A 3-input multiplexer is provided, whose output is connected to the positive reference of a comparator. The multiplexer output is controlled by bits MUX2:0 of ACON1. A bandgap reference supplies the negative reference of the comparator. The output of the comparator may be used the trigger the capture input of module 4 of the PCA.

A low impedance pulldown is supplied at the XYZRAMP pin and is controlled by bit AC5 of ACON0.

The functions of the analog section are controlled by the IBM® TrackPoint™ code embedded within the Philips TPM754.
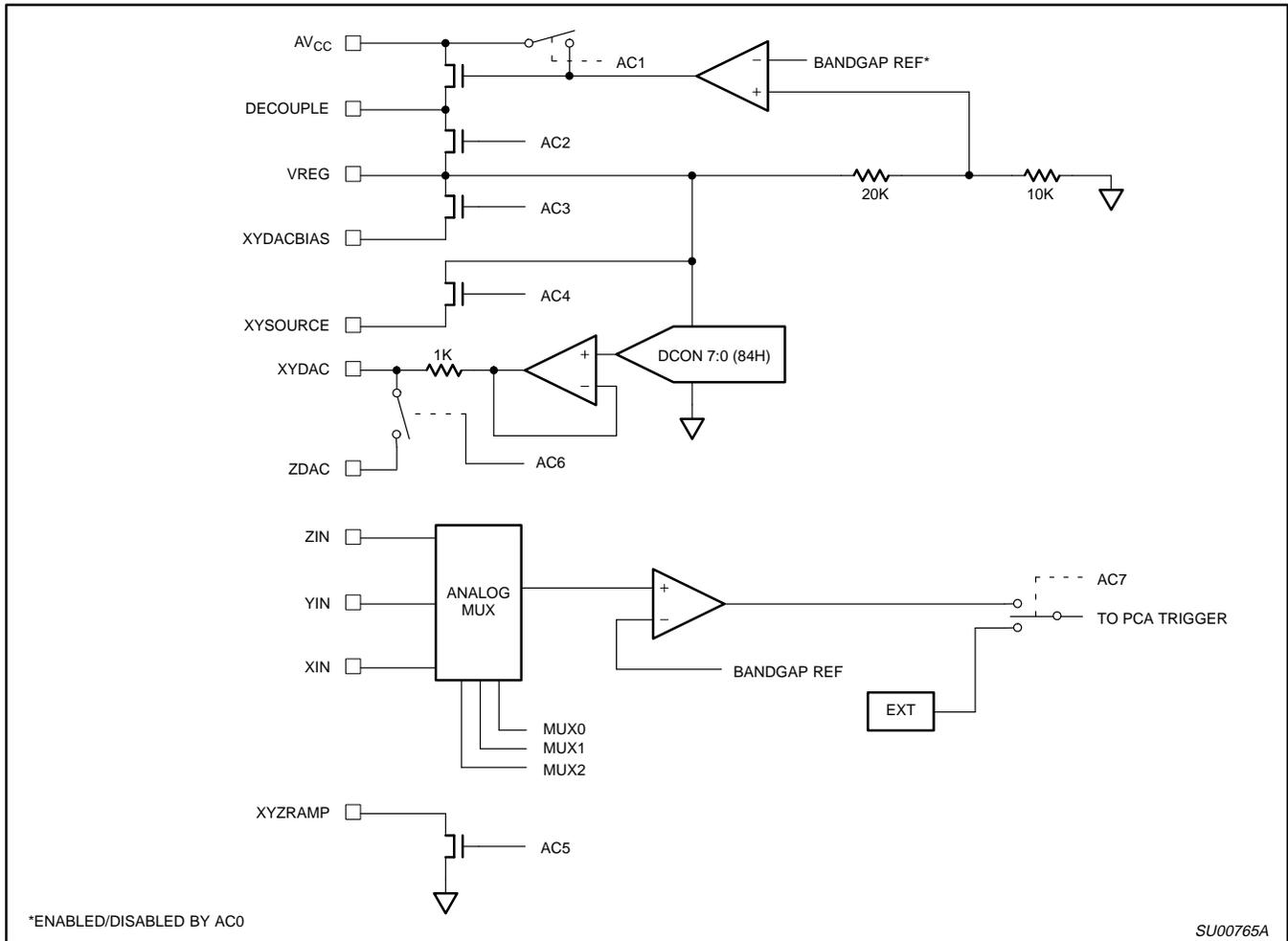
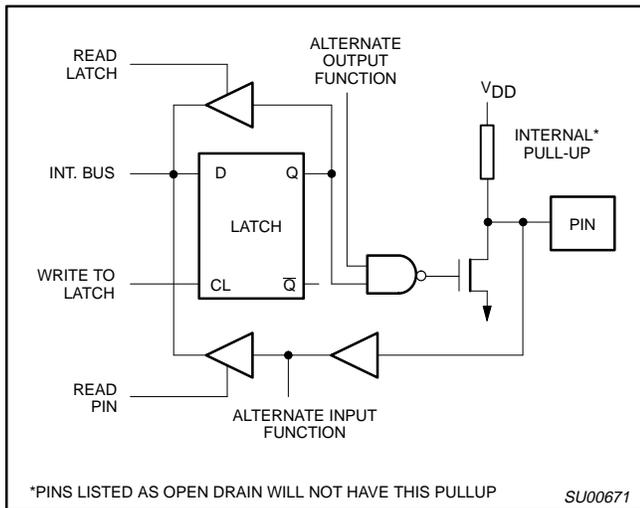**Figure 1. Analog Section**

Figure 2.   Typical Port Bit Latches and I/O Buffers

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ABSOLUTE MAXIMUM RATINGS[1, 3, 4]

PARAMETER	RATING	UNIT
Storage temperature range	−65 to +150	°C
Voltage from V_{CC} to V_{SS}	−0.5 to +6.5	V
Voltage from any pin to V_{SS}	−0.5 to V_{CC} + 0.5	V
Power dissipation	1.0	W

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0°C$ to $+70°C$, $AV_{CC} = 5V \pm 5$, $AV_{SS} = 0V$[4]
$V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[4]			UNIT
			MIN	TYP[1]	MAX	
I_{CC}	Supply current (see Figure 5)					
Inputs						
V_{IL}	Input low voltage, port 1, 3		−0.5		$0.2V_{CC}$−0.1	V
V_{IH}	Input high voltage, port 1, 3		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, X1, RST		$0.7V_{CC}$		V_{CC}+0.5	V
Outputs						
V_{OL}	Output low voltage, port 3, 1.2	I_{OL} = 1.6mA[2]			0.45	V
V_{OL1}	Output low voltage, port 1.0, 1.1	I_{OL} = 3.2mA[2]			0.45	V
V_{OH}	Output high voltage, ports 3, 1.0, 1.1	I_{OH} = −60µA,	2.4			V
I_{LI}	Input leakage current, port 1, 3, RST	$0.45 < V_{IN} < V_{CC}$			±10	µA
C_{IO}	Pin capacitance	Test freq = 1MHz, T_{amb} = 25°C			10	pF

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. Under steady state (non-transient) conditions, IOL must be externally limited as follows:
   - Maximum I_{OL} per port pin: 10mA
   - Maximum I_{OL} per 8-bit port: 26mA
   - Maximum total I_{OL} for all outputs: 67mA

   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
5. Power-down I_{CC} is measured with all output pins disconnected; X2, X1 n.c.; RST = V_{SS}.
6. I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} − 0.5V$; X2 n.c.; RST = V_{CC}. I_{CC} will be slightly higher if a crystal oscillator is used.
7. Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} − 0.5V$; X2 n.c.; RST = V_{SS}.

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ANALOG SECTION ELECTRICAL CHARACTERISTICS

$T_{amb} = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[4]			UNIT
			MIN	TYP[1]	MAX	
Analog Inputs						
AV_{CC}	Analog supply voltage		4.5	–	5.5	V
	Sensor resistor		330	–	3K	Ω
IAV_{CC}		AC0 = 0 IC only	–	1.2	1.8	mA
		AC0 = 1	–	–	10	μA
Regulator						
VREG			3.6	3.8	4.0	V
IVREG			13	–	80	mA
CDECOUPLE		Stability requirement	–	10	–	μF
RDSONQ1			–	7	12	Ω
ILEAKAGEQ1			–10		+10	μA
ILEAKAGEQ2			–10		+10	μA
PSRR		100Hz	–	–40	–	dB
MUX and Comparator						
	Comparator trip point		1.14	1.26	1.38	V
	MUX impedance		–	1	4	kΩ
ILEAKAGEMUX			–10		+10	μA
Digital-to-Analog Conversion						
	ZDAC, XYDAC monotonicity		8	–	–	bits
	ZDAC switch impedance		–	75	200	Ω
	DAC output resistance		–	2.7	5	kΩ
	ZDAC switch leakage		–10		+10	μA
Switches						
	XYZRAMP impedance		–	33	100	Ω
	XYZRAMP leakage		–10		+10	μA
	XYDACBIAS impedance		–	13	25	Ω
	XYDACBIAS leakage		–10		+10	μA
	XYSOURCE impedance		–	200	400	Ω
	XYSOURCE leakage		–10		+70	μA

AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm10\%$, $V_{SS} = 0V$[4]

SYMBOL	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
		MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	Oscillator frequency:			3.5	12	MHz
External Clock (Figure 3)						
t_{CHCX}	High time	20		20		ns
t_{CLCX}	Low time	20		20		ns
t_{CLCH}	Rise time		20		20	ns
t_{CHCL}	Fall time		20		20	ns

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always
't' (= time). The other characters, depending on their positions,
indicate the name of a signal or the logical status of that signal.
The designations are:

C – Clock
D – Input data
H – Logic level high
L – Logic level low
Q – Output data
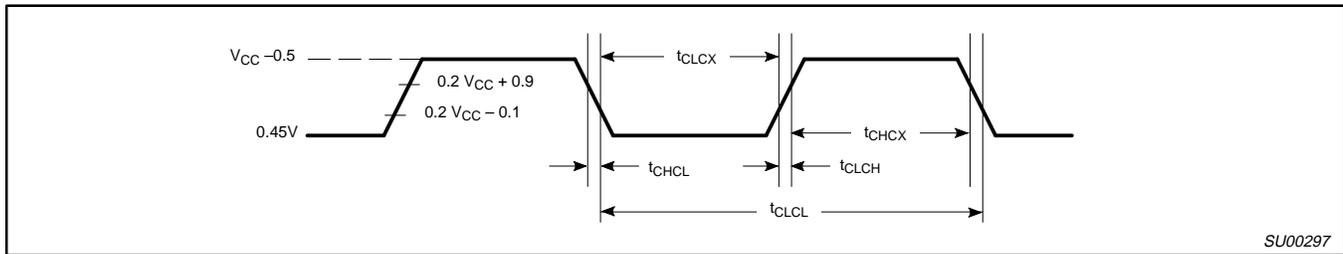T – Time
V – Valid
X – No longer a valid logic level
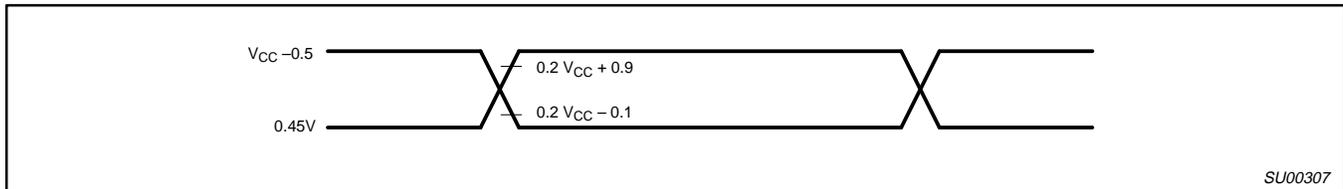Z – Float

SU00297

Figure 3. External Clock Drive

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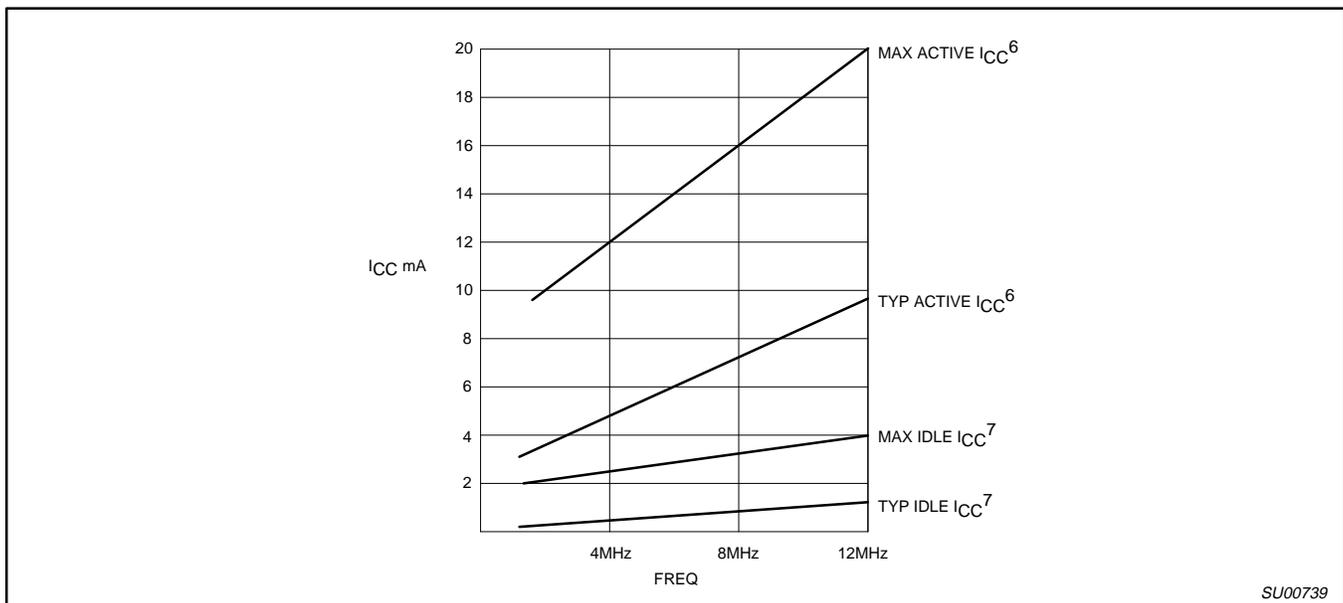
Figure 4. AC Testing Input/Output

SU00739

Figure 5. I_{CC} vs. FREQ
Maximum I_{CC} values taken at V_{CC} = 5.5V and worst case temperature.
Typical I_{CC} values taken at V_{CC} = 5.0V and 25°C.
Notes 6 and 7 refer to AC Electrical Characteristics.