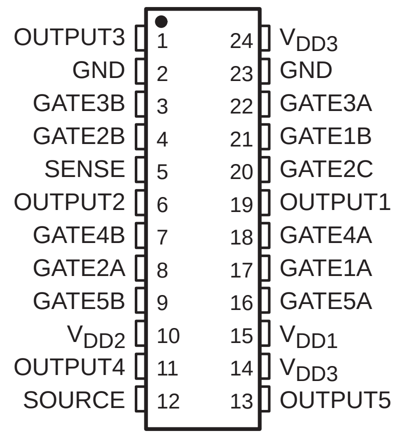
- **Low $r_{DS(on)}$:**
  0.1 Ω Typ (Full H-Bridge)
  0.4 Ω Typ (Triple Half H-Bridge)
- **Pulsed Current:**
  12 A Per Channel (Full H-Bridge)
  6 A Per Channel (Triple Half H-Bridge)
- **Matched Sense Transistor for Class A-B Linear Operation**
- **Fast Commutation Speed**

DW PACKAGE
(TOP VIEW)

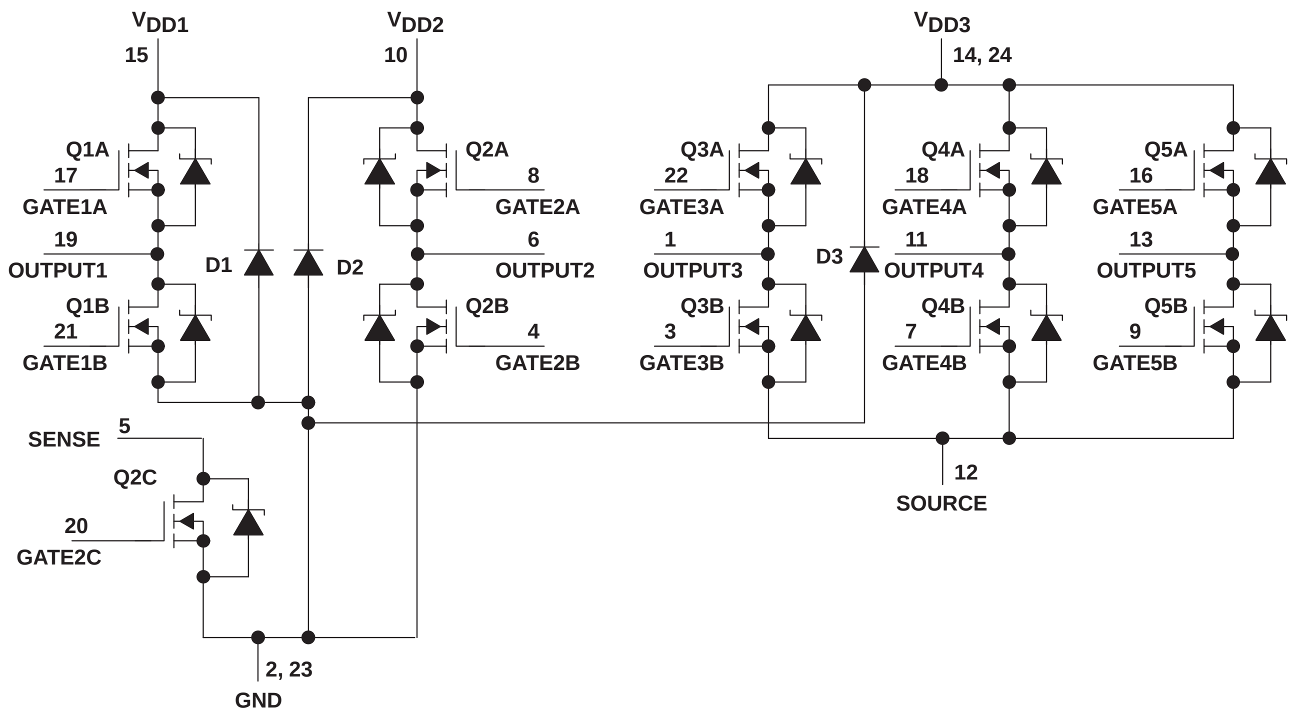


description

The TPIC1501A is a monolithic power array that consists of ten electrically isolated N-channel enhancement-mode power DMOS transistors, four of which are configured as a full H-bridge and six as a triple half H-bridge. The lower stage of the full H-bridge features an integrated sense FET to allow biasing of the bridge in class A-B operation.

The TPIC1501A is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



NOTES: A. Pins 2 and 23 must be externally connected.
B. Pins 14 and 24 must be externally connected.
C. No output may be taken greater than 0.5 V below GND.

absolute maximum ratings, T_C = 25°C (unless otherwise noted)†

Supply-to-GND voltage	20 V
Source-to-GND voltage (Q3A, Q4A, Q5A)	20 V
Output-to-GND voltage	20 V
Sense-to-GND voltage	20 V
Gate-to-source voltage range, V_{GS} (Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	±20 V
Gate-to-source voltage range, V_{GS} (Q2C)	–0.7 V to 6 V
Continuous drain current, each output (Q1A, Q1B, Q2A, Q2B)	3 A
Continuous drain current, each output (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	1.5 A
Continuous drain current (Q2C)	15 mA
Continuous source-to-drain diode current (Q1A, Q1B, Q2A, Q2B)	3 A
Continuous source-to-drain diode current (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	1.5 A
Continuous source-to-drain diode current (Q2C)	15 mA
Pulsed drain current, each output, I_{max} (Q1A, Q1B, Q2A, Q2B) (see Note 1 and Figure 24)	12 A
Pulsed drain current, each output, I_{max} (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) (see Note 1 and Figure 25)	6 A
Pulsed drain current, I_{max} (Q2C) (see Note 1)	60 mA
Continuous total power dissipation, T_C = 70°C (see Note 2 and Figures 24 and 25)	2.86 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Pulse duration = 10 ms, duty cycle = 2%
2. Package is mounted in intimate contact with infinite heat sink.

electrical characteristics, Q1A, Q1B, Q2A, Q2B, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA,	V_{GS} = 0	20			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.4	1.7	2.1	V
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	I_D = 1 mA,	V_{DS} = V_{GS}			40	mV
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 µA (D1, D2)		20			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2 A, See Notes 3 and 4	V_{GS} = 10 V,		0.2	0.24	V
V_F	Forward on-state voltage, GND-to-V_{DD1}, GND-to-V_{DD2}	I_D = 3 A (D1, D2) See Notes 3 and 4			1.8		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2 A, See Notes 3 and 4 and Figure 19	V_{GS} = 0,		0.85	1.05	V
		I_S = 3 A, See Notes 3 and 4 and Figure 19	V_{GS} = 0,		0.9	1.1	
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 16 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 16 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 16 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, V_{DD1}-to-GND, V_{DD2}-to-GND, gate shorted to source	V_{DGND} = 16 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2 A, See Notes 3 and 4 and Figure 9	T_C = 25°C		0.1	0.12	Ω
			T_C = 125°C		0.14	0.18	
		V_{GS} = 10 V, I_D = 3 A, See Notes 3 and 4 and Figures 7 and 9	T_C = 25°C		0.1	0.12	
			T_C = 125°C		0.14	0.18	
g_{fs}	Forward transconductance	V_{DS} = 14 V, See Notes 3 and 4	I_D = 1 A,	1.5	2.5		S
		V_{DS} = 14 V, See Notes 3 and 4 and Figure 13	I_D = 1.5 A,	2	3.1		
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 14 V, f = 1 MHz,	V_{GS} = 0, See Figure 17		240		pF
C_{oss}	Short-circuit output capacitance, common source				170		
C_{rss}	Short-circuit reverse transfer capacitance, common source				130		
α_S	Sense-FET drain current ratio	V_{DS} = 6 V,	$I_{D(Q2C)}$ = 40 µA	75	130	200	

NOTES: 3. Technique should limit T_J – T_C to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, Q1A, Q2A, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 1.5 A, V_{DS} = 14 V, See Figures 1 and 23	V_{GS} = 0, di/dt = 100 A/µs,		70		ns
Q_{RR}	Total diode charge				90		nC
t_{rr}	Reverse-recovery time	I_S = 2 A, V_{DS} = 14 V,	V_{GS} = 0, di/dt = 100 A/µs		75		ns
Q_{RR}	Total diode charge				110		nC

resistive-load switching characteristics, Q1A, Q1B, Q2A, Q2B, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 14 V, R_L = 9.3 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 3		20		ns
$t_{d(off)}$	Turn-off delay time			30		
t_r	Rise time			15		
t_f	Fall time			25		
Q_g	Total gate charge	V_{DS} = 14 V, I_D = 1.5 A, V_{GS} = 10 V, See Figure 4		5.6	7	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.8	1	
Q_{gd}	Gate-to-drain charge			1.4	1.75	
$L_{(drain)}$	Internal drain inductance			5		nH
$L_{(source)}$	Internal source inductance			5		
$r_{(gate)}$	Internal gate resistance			0.25		Ω

electrical characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA,	V_{GS} = 0 V	20			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 6	V_{DS} = V_{GS},	1.4	1.7	2.1	V
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	I_D = 1 mA,	V_{DS} = V_{GS}			40	mV
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 µA (D3)		20			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.5 A, See Notes 3 and 4	V_{GS} = 10 V,		0.6	0.68	V
V_F	Forward on-state voltage, GND-to-V_{DD3}	I_D = 1.5 A (D3) See Notes 3 and 4			1.7		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.5 A, See Notes 3 and 4 and Figure 20	V_{GS} = 0,		1	1.2	V
		I_S = 2 A, See Notes 3 and 4 and Figure 20	V_{GS} = 0,		1.1	1.3	
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 16 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 16 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 16 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, V_{DD3}-to-GND, gate shorted to source	V_{DGND} = 16 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 0.3 A, See Notes 3 and 4 and Figure 10	T_C = 25°C		0.35	0.39	Ω
			T_C = 125°C		0.5	0.56	
		V_{GS} = 10 V, I_D = 1.5 A, See Notes 3 and 4 and Figures 8 and 10	T_C = 25°C		0.4	0.45	
			T_C = 125°C		0.56	0.65	
g_{fs}	Forward transconductance	V_{DS} = 14 V, See Notes 3 and 4	I_D = 500 mA,	0.3	0.8		S
		V_{DS} = 14 V, See Notes 3 and 4 and Figure 14	I_D = 750 mA,	0.4	0.93		
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 14 V, f = 1 MHz,	V_{GS} = 0, See Figure 18		96		pF
C_{oss}	Short-circuit output capacitance, common source				98		
C_{rss}	Short-circuit reverse transfer capacitance, common source				65		

NOTES: 3. Technique should limit T_J – T_C to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, Q3A, Q4A, Q5A, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 750 mA, V_{GS} = 0, V_{DS} = 14 V, di/dt = 100 A/µs, See Figures 2 and 23		60		ns
Q_{RR}	Total diode charge			55		nC
t_{rr}	Reverse-recovery time	I_S = 1.5 A, V_{GS} = 0, V_{DS} = 14 V, di/dt = 100 A/µs		120		ns
Q_{RR}	Total diode charge			150		nC

resistive-load switching characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, T_C = 25°C

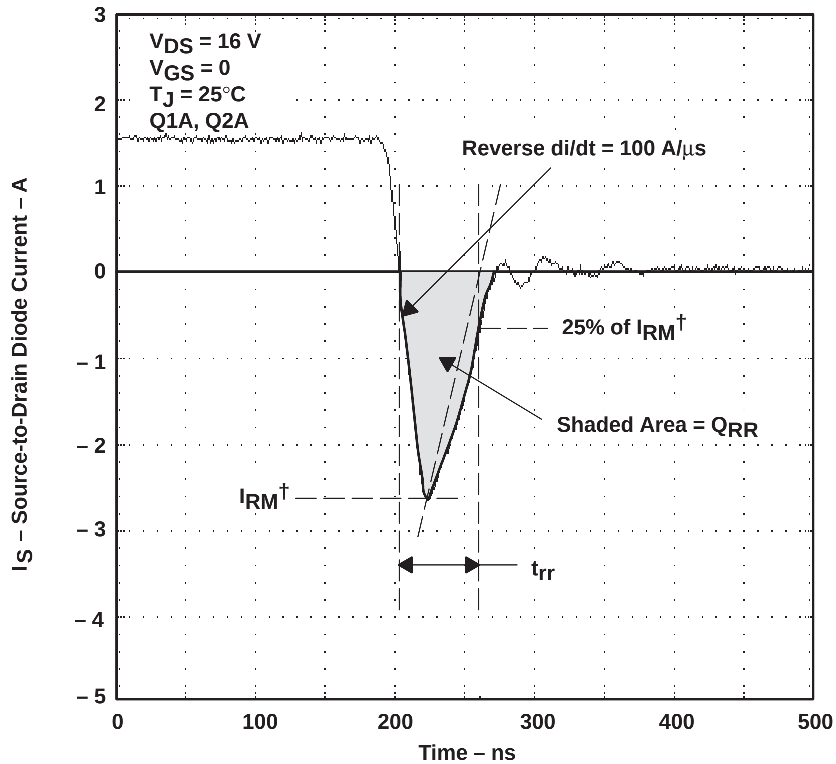
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 14 V, R_L = 18.7 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 3		18		ns
$t_{d(off)}$	Turn-off delay time			25		
t_r	Rise time			13		
t_f	Fall time			20		
Q_g	Total gate charge	V_{DS} = 14 V, I_D = 750 mA, V_{GS} = 10 V, See Figure 4		1.6	2	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.26	0.32	
Q_{gd}	Gate-to-drain charge			0.42	0.52	
$L_{(drain)}$	Internal drain inductance			5		nH
$L_{(source)}$	Internal source inductance			5		
$r_{(gate)}$	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 5 and 8		90		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 6 and 8		38		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 7 and 8		28		

NOTES: 5. Package is mounted on a FR4 printed-circuit board with no heat sink.
6. Package is mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
7. Package is mounted in intimate contact with infinite heat sink.
8. All outputs have equal power.

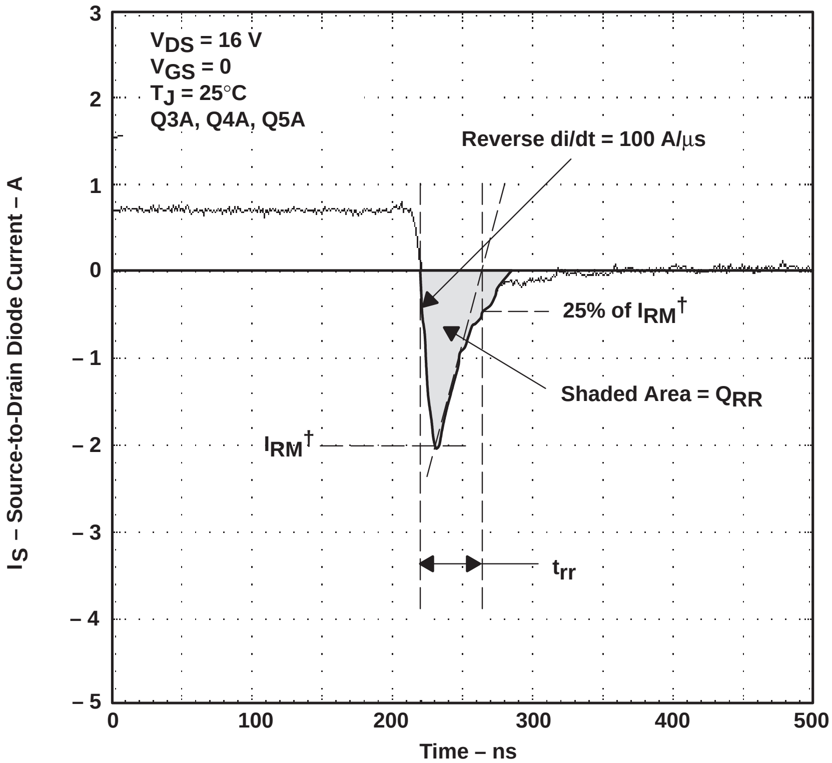
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

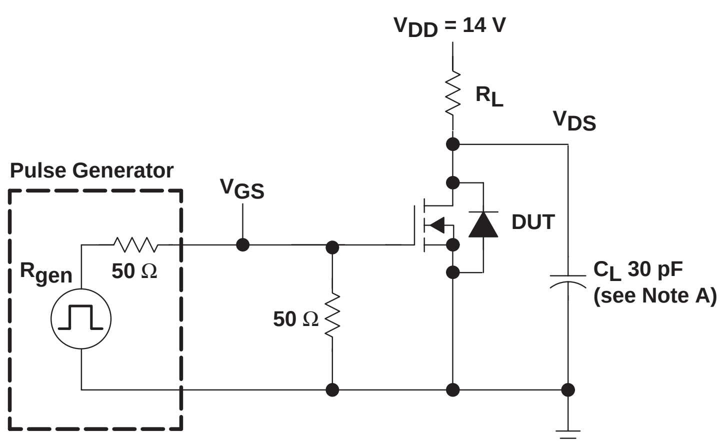
Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes

PARAMETER MEASUREMENT INFORMATION

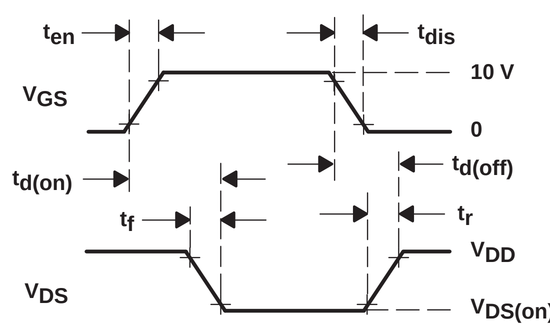


† I_{RM} = maximum recovery current

Figure 2. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes



TEST CIRCUIT

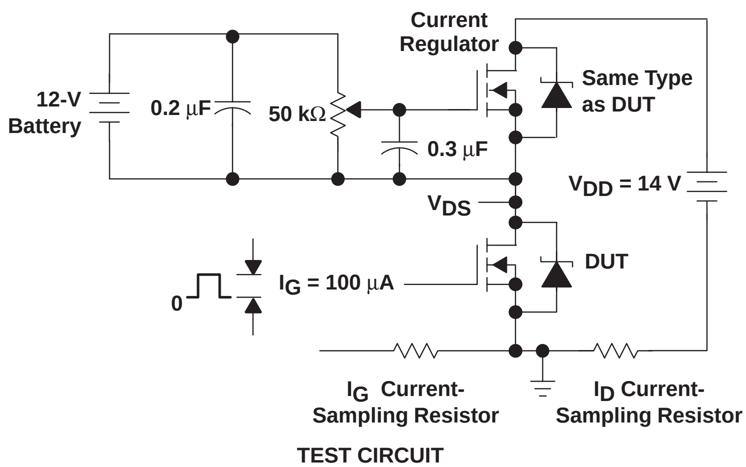


VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



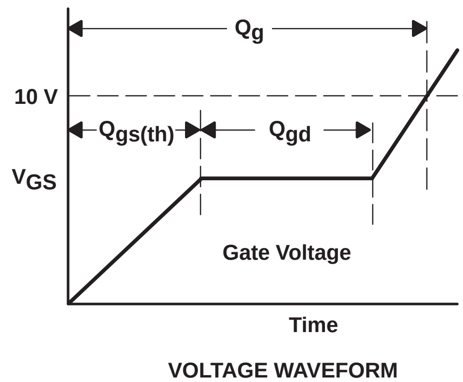


Figure 4. Gate-Charge Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS

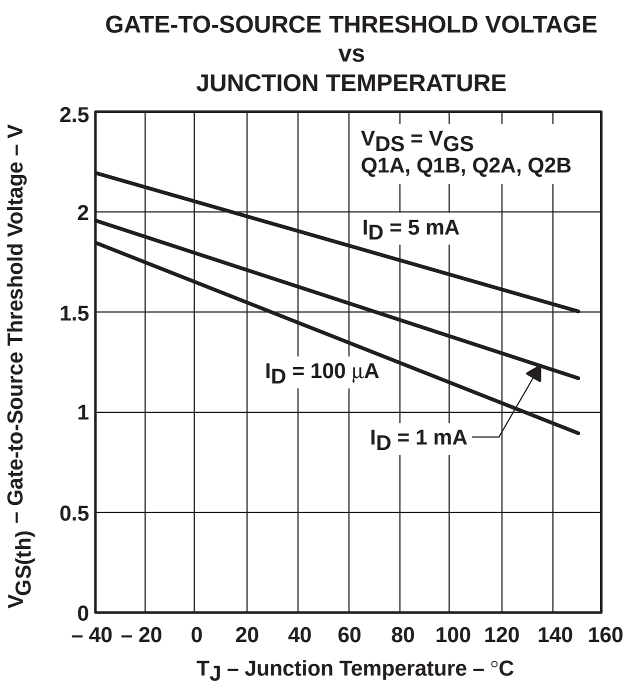


Figure 5

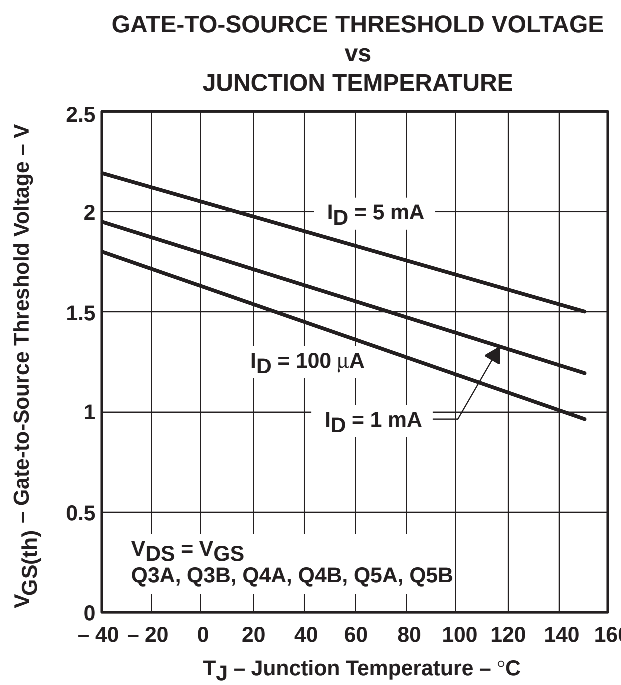


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

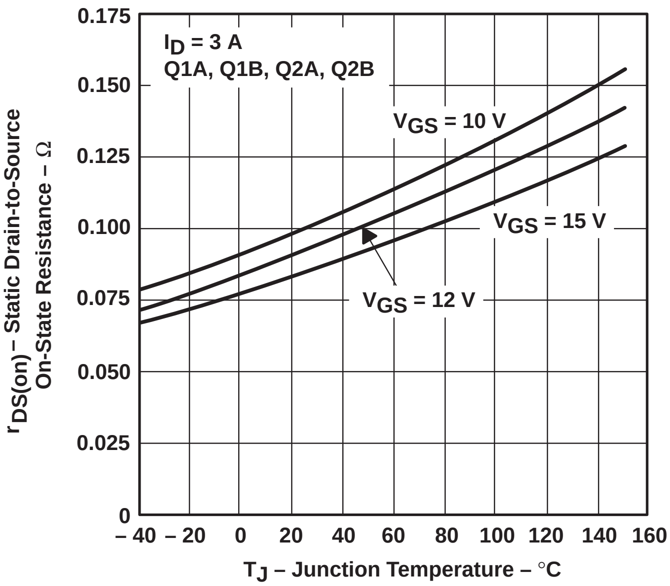


Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

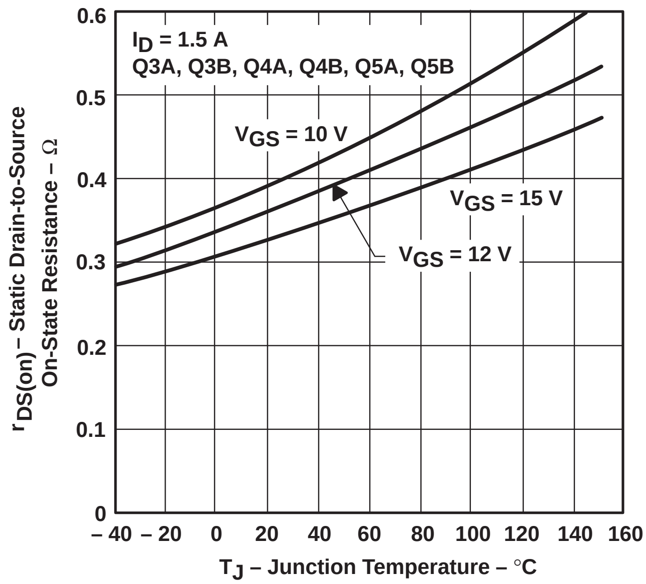


Figure 8

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

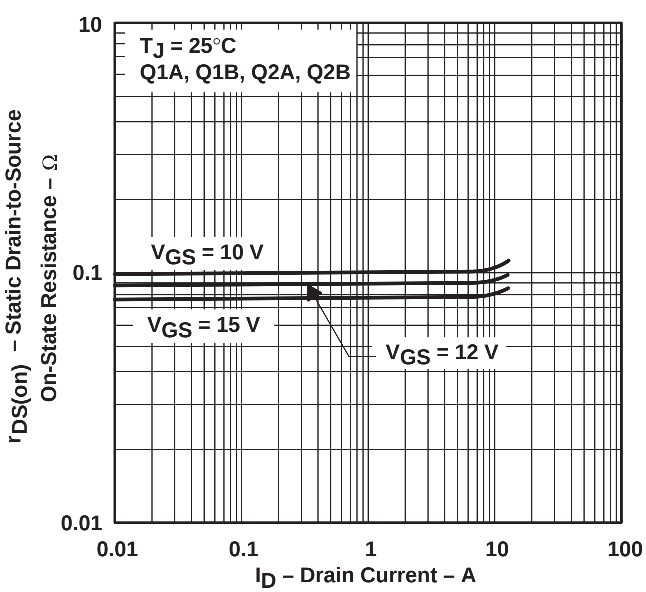


Figure 9

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

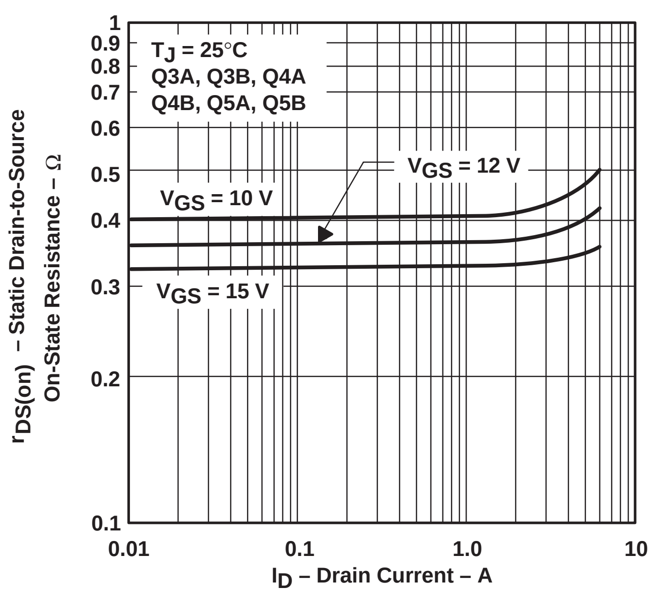


Figure 10

TYPICAL CHARACTERISTICS

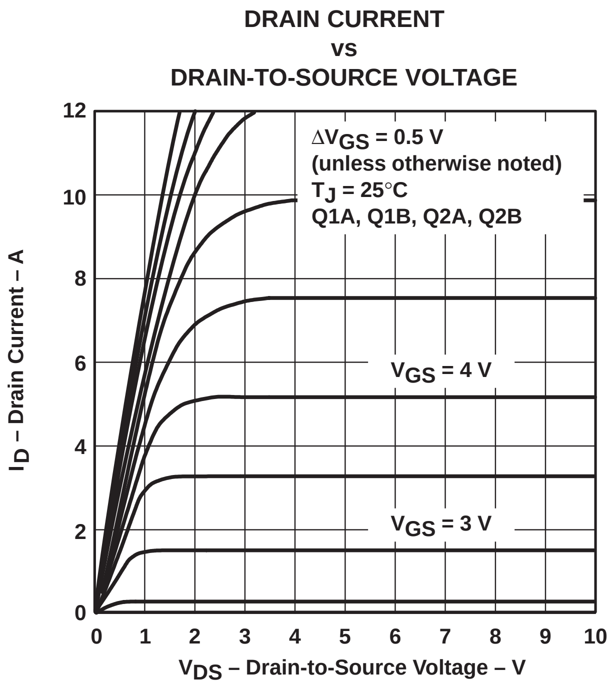


Figure 11

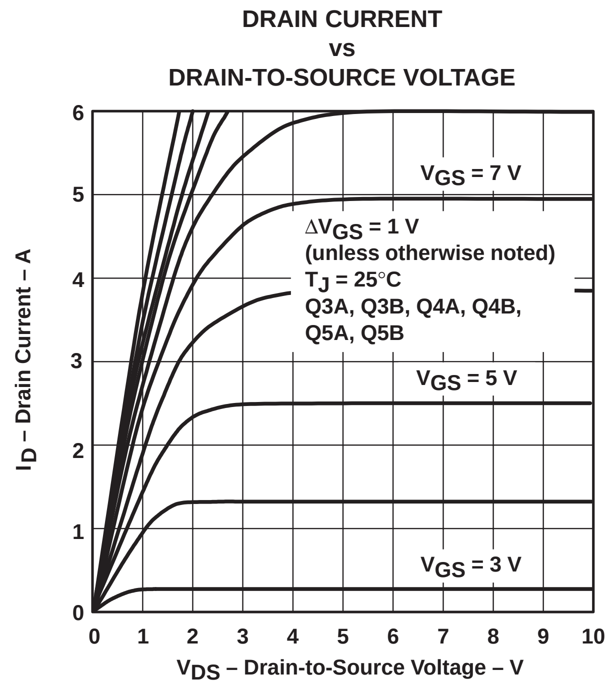


Figure 12

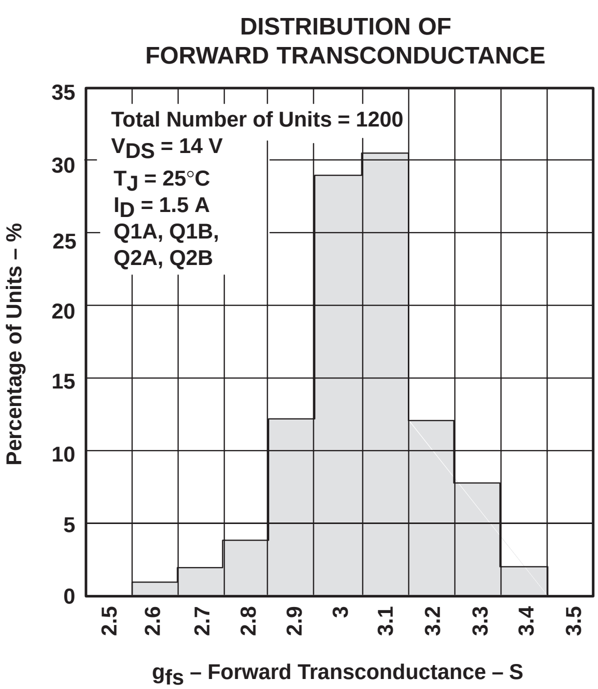


Figure 13

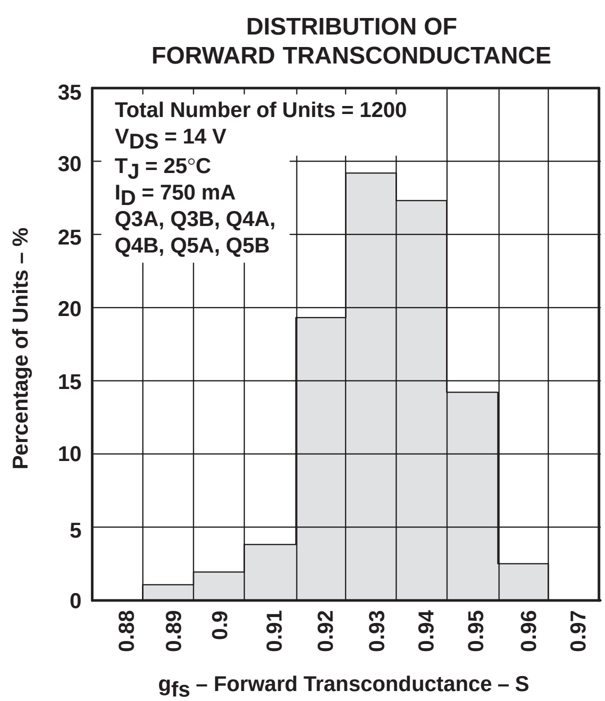


Figure 14

TYPICAL CHARACTERISTICS

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

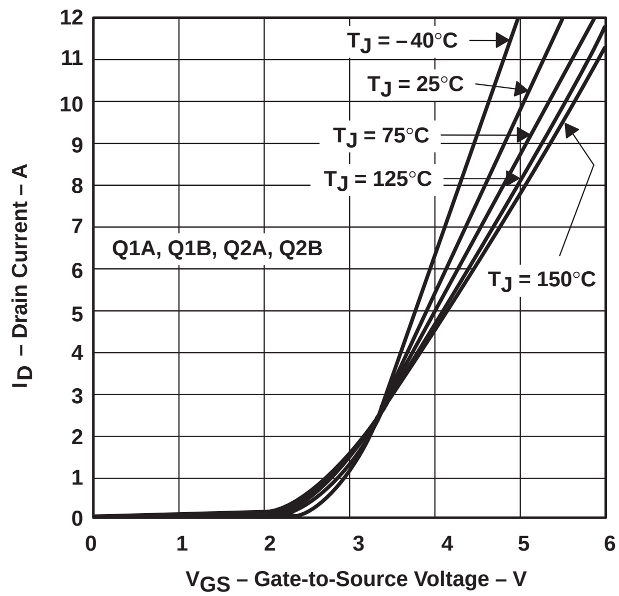


Figure 15

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

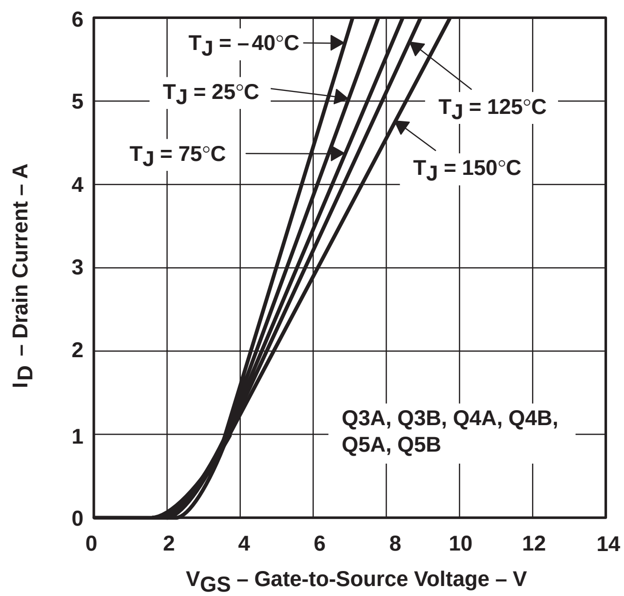


Figure 16

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

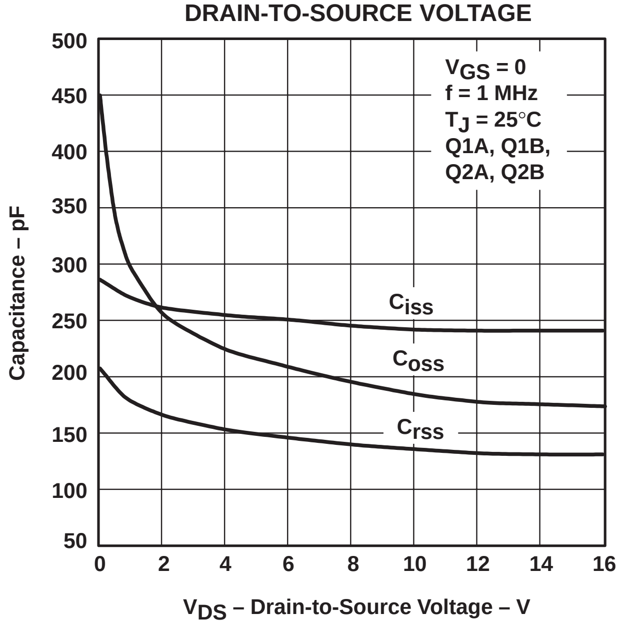


Figure 17

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

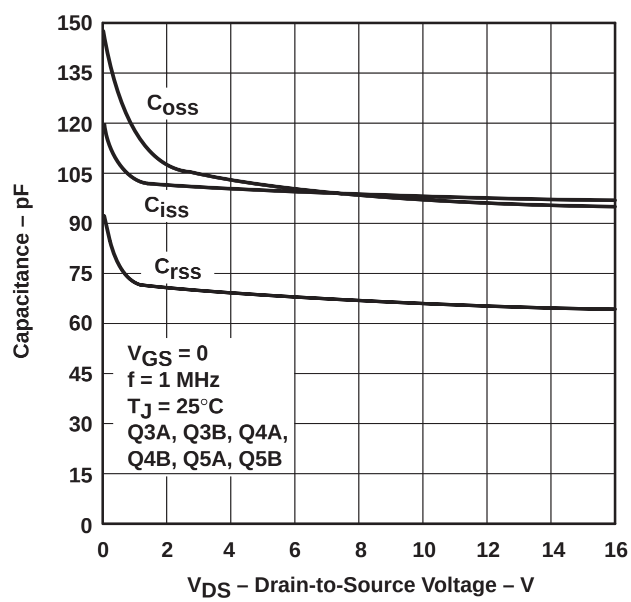


Figure 18

TYPICAL CHARACTERISTICS

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

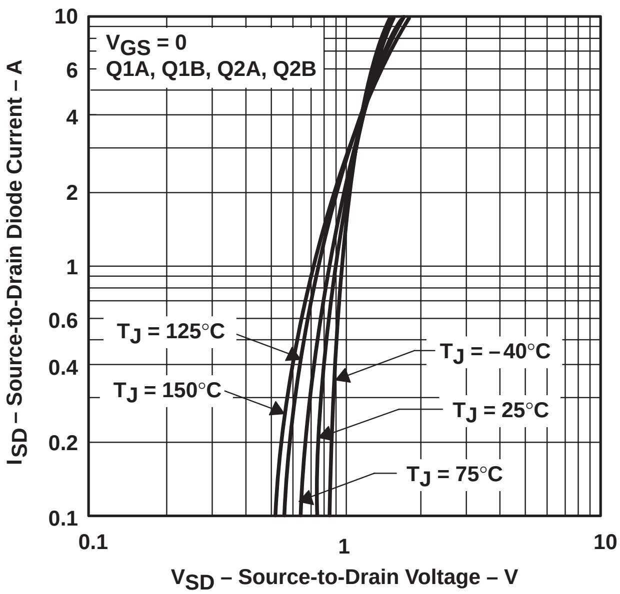


Figure 19

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

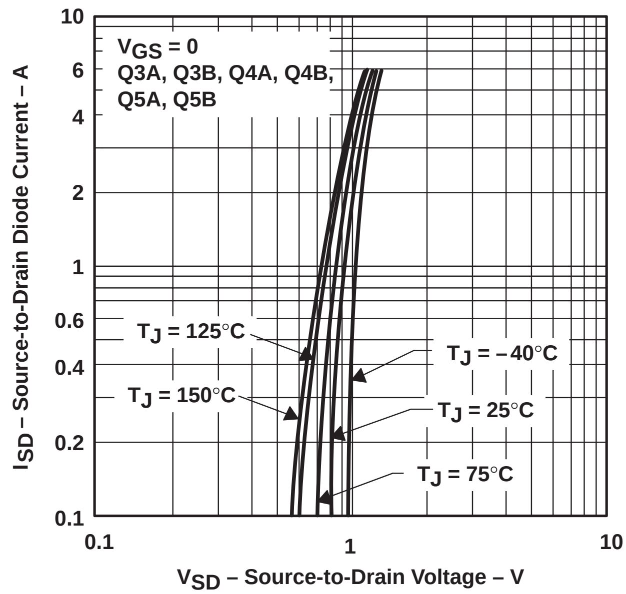


Figure 20

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

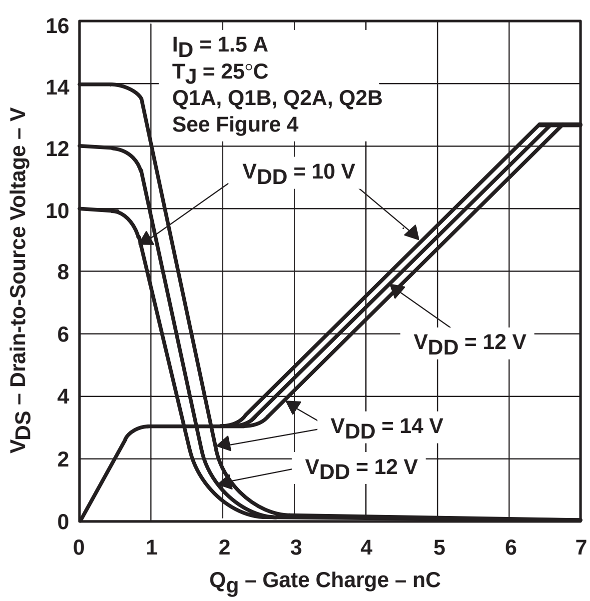


Figure 21

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

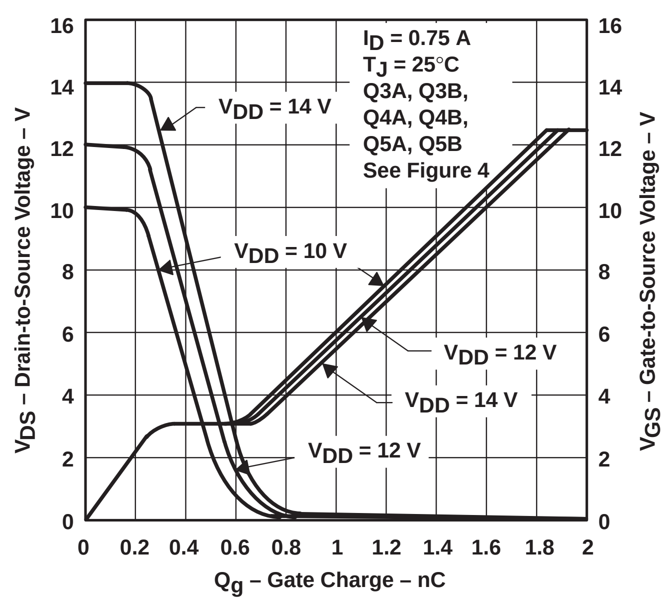


Figure 22

TYPICAL CHARACTERISTICS

**REVERSE RECOVERY TIME
vs
REVERSE di/dt**

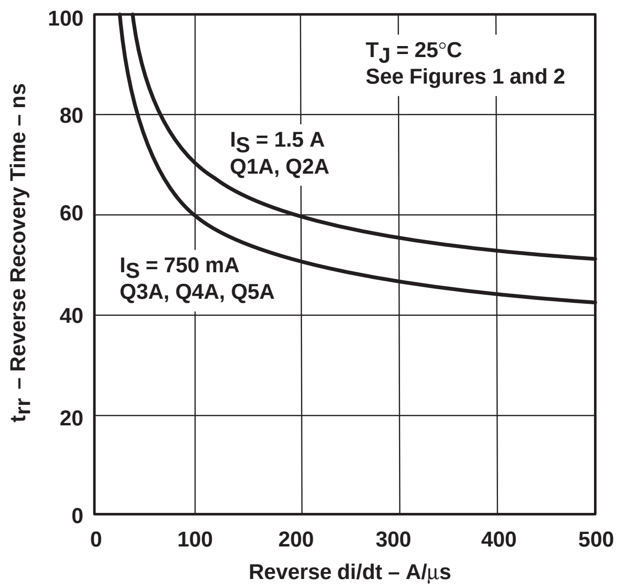


Figure 23

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**

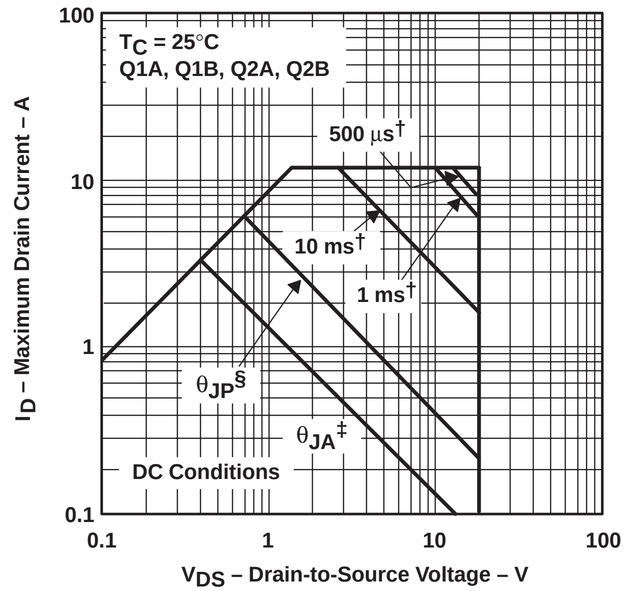


Figure 24

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**

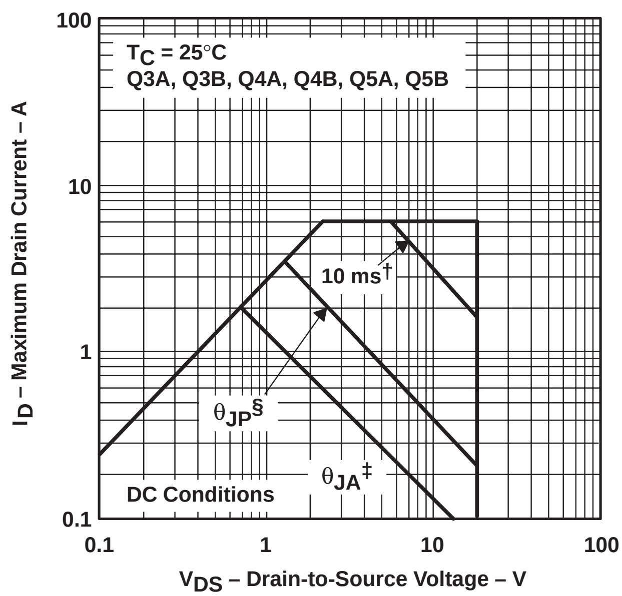
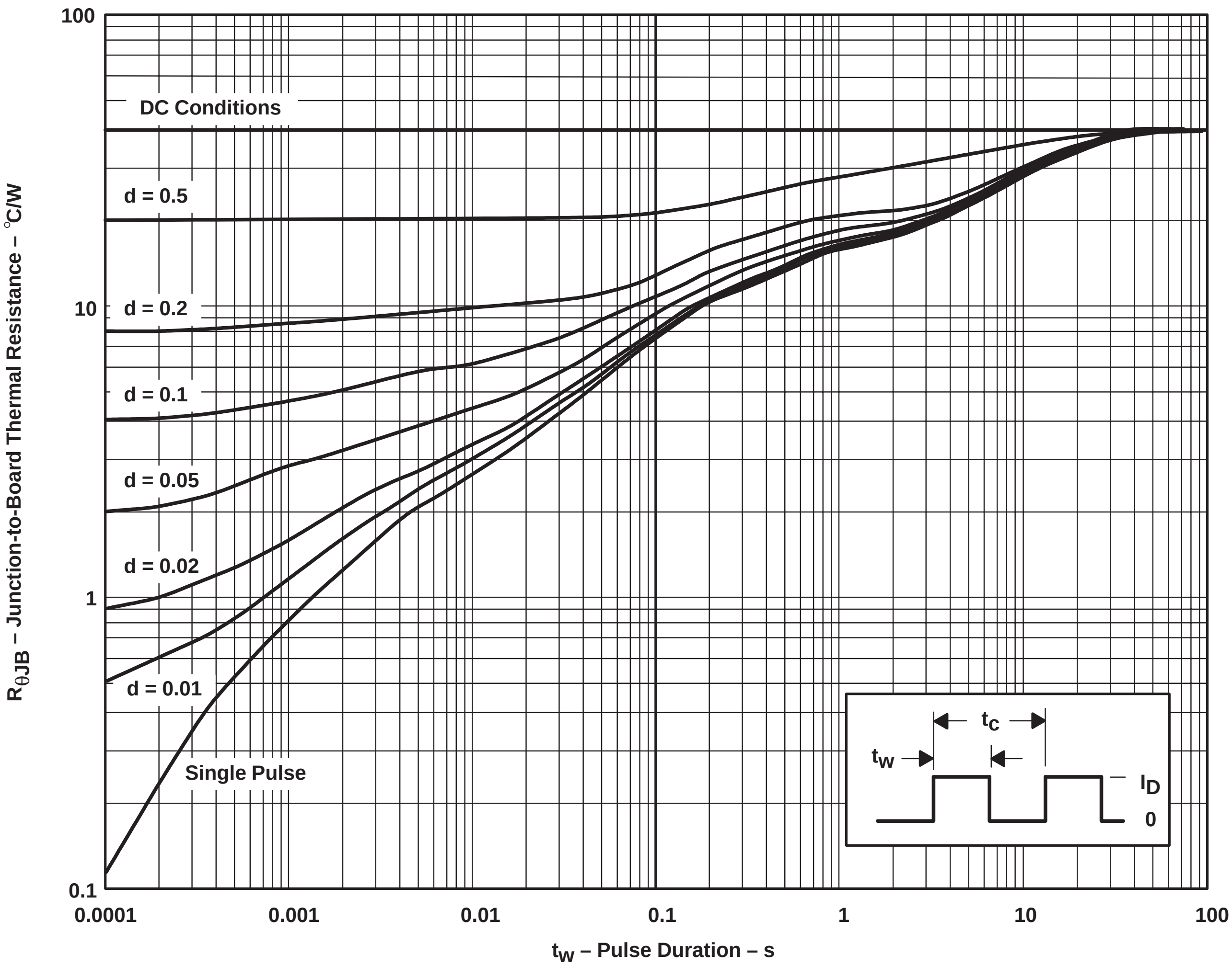


Figure 25

† Less than 10% duty cycle
‡ Device is mounted on a 24 in^2, 4 layer FR4 printed-circuit board.
§ Device is mounted in intimate contact with infinite heat sink.

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device is mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heat sink.

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 26

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TPIC1501ADW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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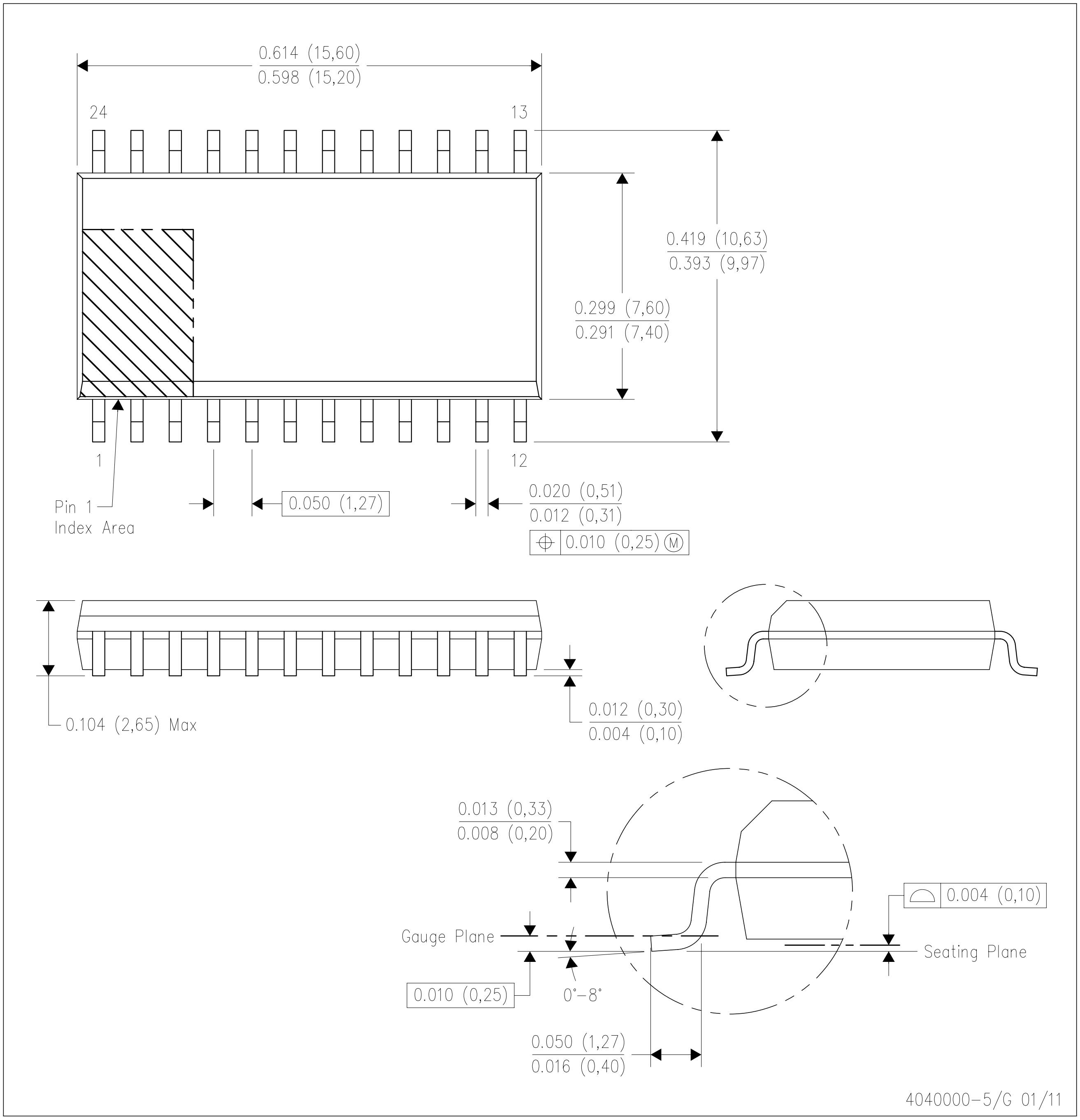
DW (R-PDSO-G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AD.

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