4-CHANNEL ESD PROTECTION ARRAY WITH 1.5-pF IO CAPACITANCE

Check for Samples: TPD4E001-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H3B**
  - **HBM Level 15 kV**
  - **Device CDM ESD Classification Level C4B**
- **4-Channel ESD Clamp Array to Enhance System-Level ESD Protection**
- **Exceeds IEC61000-4-2 (Level 4) ESD Protection Requirements**
  - **±8-kV IEC 61000-4-2 Contact Discharge**
  - **±15-kV IEC 61000-4-2 Air-Gap Discharge**
- **5.5-A Peak Pulse Current (8/20-us Pulse)**
- **Low 1.5-pF Input Capacitance**
- **Low 1-nA (Max) Leakage Current**
- **0.9-V to 5.5-V Supply-Voltage Range**

APPLICATIONS

- **USB 2.0**
- **Ethernet**
- **FireWire™**
- **Precision Analog Interface**
- **SVGA Connections**

DESCRIPTION

The TPD4E001-Q1 is a low-capacitance ±15-kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND. The TPD4E001-Q1 protects against ESD pulses up to ±15-kV human-body model (HBM), ±8-kV contact discharge, and ±15-kV air-gap discharge, as specified in IEC 61000-4-2. This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultralow leakage current (<1 nA maximum) is suitable for precision analog measurements in applications like glucose meters, heart rate monitors, and so forth.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	DBV (SOT-23)	Reel of 3000	TPD4E001QDBVRQ1	AAXQ

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

DBV PACKAGE (TOP VIEW)

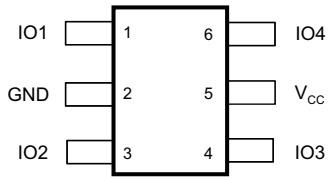

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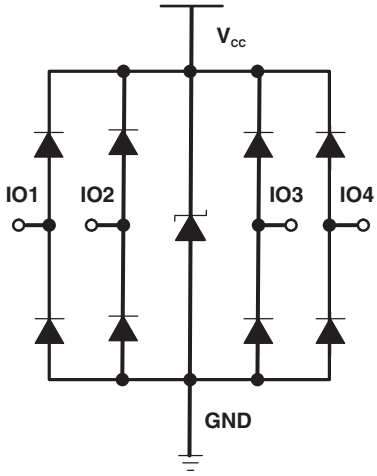
Figure 1. FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

DBV NO.	NAME	FUNCTION
1, 3, 4, 6	IOx	ESD-protected channel
2	GND	Ground
5	V_{CC}	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.
–	N/A	Exposed thermal pad. Connect to GND or leave floating.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}			–0.3	7	V
$V_{I/O}$	IO voltage tolerance		–0.3	V_{CC} + 0.3	V
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C
ESD	Electrostatic discharge	Human-body model, HBM, ESD classification level H3B		15	kV
		Charged-device model, CDM, ESD Classification Level C4B		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPD4E001-Q1 DBV 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	202.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	146.2	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	47.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	37.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	46.7	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Electrical Characteristics

V_{CC} = 5 V ± 10%, T_A = –40°C to 125°C (unless otherwise noted)

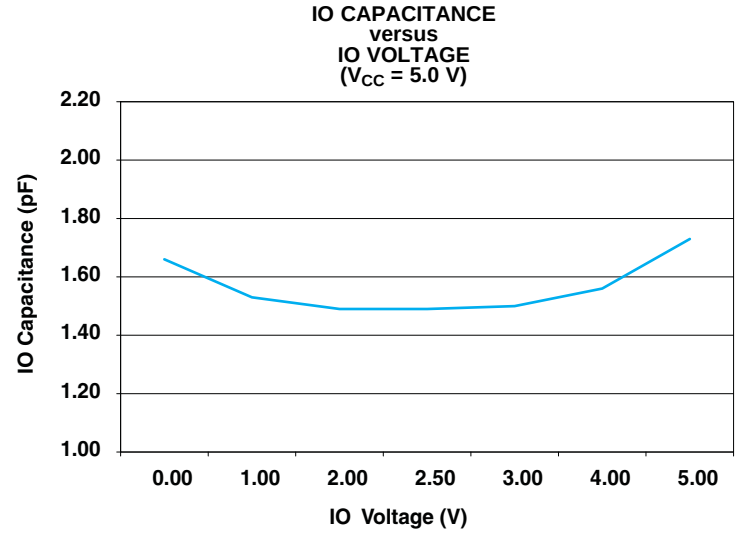
PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	100	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown voltage	I_{BR} = 10 mA		11			V
V_C	Channel clamp voltage	T_A = 25°C, ±15-kV HBM, I_F = 10 A	Positive transients			V_{CC} + 25	V
			Negative transients			–25	
		T_A = 25°C, ±8-kV contact discharge (IEC 61000-4-2), I_F = 24 A	Positive transients			V_{CC} + 60	
			Negative transients			–60	
		T_A = 25°C, ±15-kV air-gap discharge (IEC 61000-4-2), I_F = 45 A	Positive transients			V_{CC} + 100	
			Negative transients			–100	
		ESD strike on IO pin, GND pin grounded, I_{PP} = 5 A, 8/20 µs(2)	Positive transients		17		
V_{RWM}	Reverse standoff voltage	IO pin to GND pin				5.5	V
$I_{i/o}$	Channel leakage current	$V_{i/o}$ = GND to V_{CC}				±1	nA
$C_{i/o}$	Channel input capacitance	V_{CC} = 5 V, bias of V_{CC}/2			1.5		pF

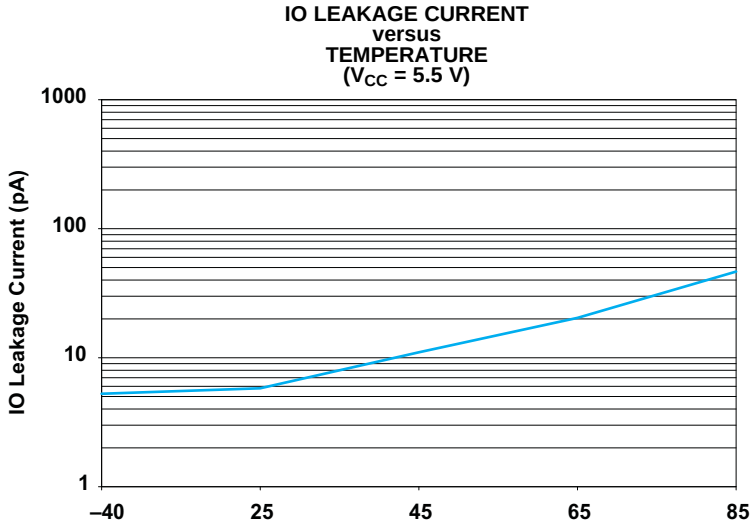
(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to ICE61000-4-5.

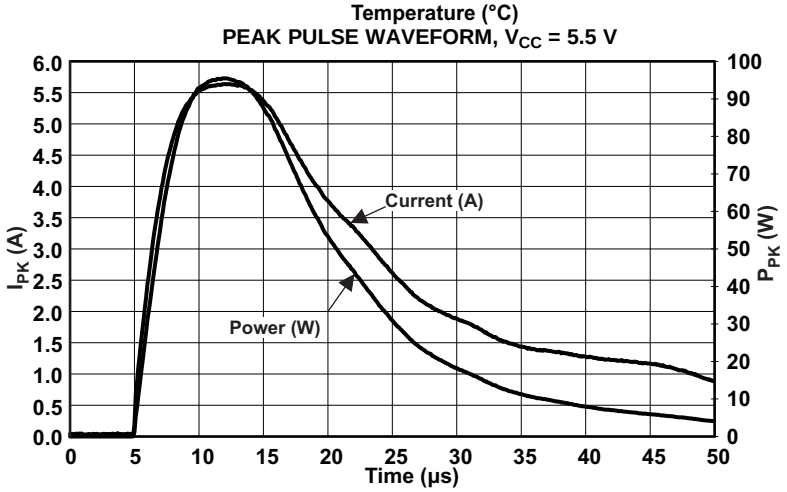
ESD Protection

PARAMETER	TYP	UNIT
HBM	±15	kV
IEC 61000-4-2 Contact Discharge	±8	kV
IEC 61000-4-2 Air-Gap Discharge	±15	kV
Peak Pulse Current, IPK (Tp = 8/20 µs)	5.5	A
Peak Pulse Power, PPK (Tp = 8/20 µs)	100	W

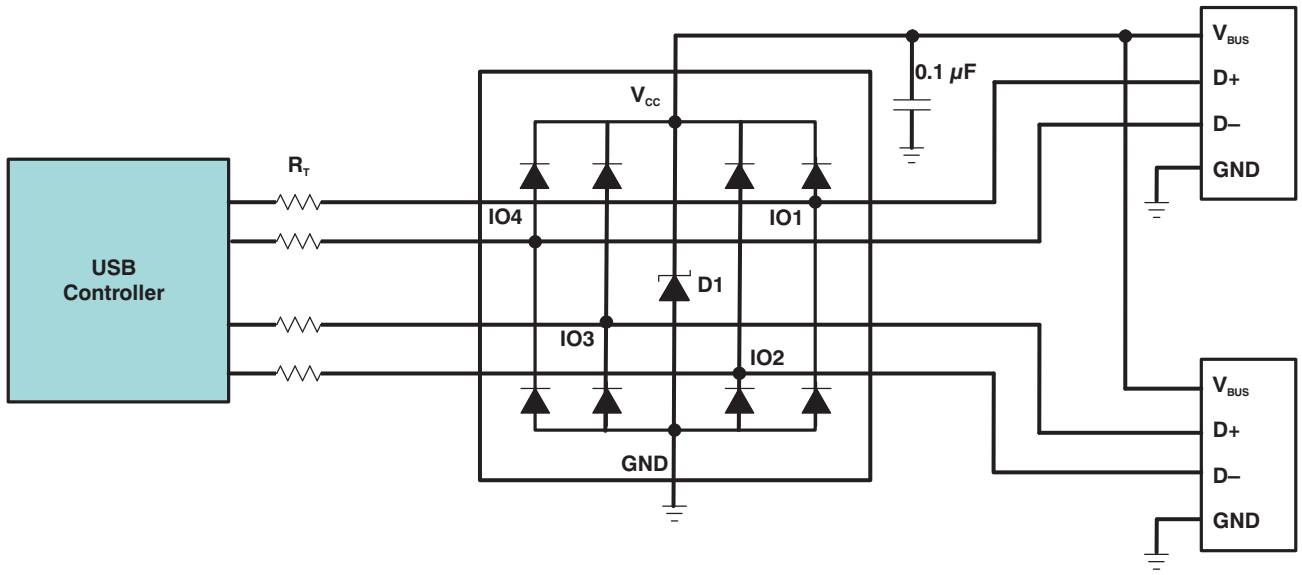
TYPICAL OPERATING CHARACTERISTICS







APPLICATION INFORMATION



Detailed Description

When placed near the connector, the TPD4E001-Q1 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultralow leakage-current specifications. The TPD4E001-Q1 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, observe the following layout and design guidelines:

1. Place the TPD4E001-Q1 solution close to the connector. This allows the TPD4E001-Q1 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-μF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E001-Q1 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating .
5. One can connect the V_{CC} pin in two different ways:
   (a) If the V_{CC} pin connects to the system power supply, the TPD4E001-Q1 works as a transient suppressor for any signal swing above V_{CC} + V_F. TI recommends a 0.1-μF capacitor on the device V_{CC} pin for ESD bypass.
   (b) If the V_{CC} pin does not connect to the system power supply, the TPD4E001-Q1 can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1-μF capacitor at the V_{CC} pin for ESD bypass.

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