CMOS 8-Bit Microcontroller

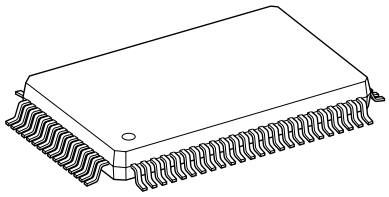
TMP88CU74F

The TMP88CU74 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain 8-bit AD conversion inputs and a VFT (Vacuum Fluorescent Tube) driver on a chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP88CU74F	96 Kbytes + 256 bytes	2 Kbytes	P-QFP80-1420-0.80B	TMP88PU74F

Features

P-QFP80-1420-0.80B



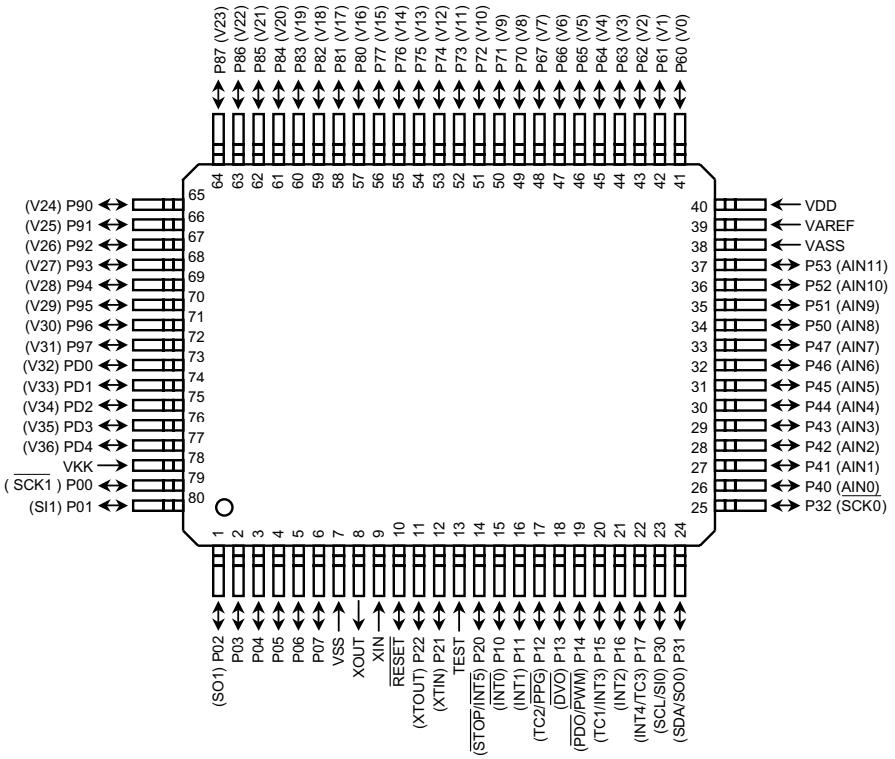
TMP88CU74F
TMP88PU74F

- 8-bit single chip microcomputer TLCS-870/X Series
- Instruction execution time: 0.32 μs (at 12.5 MHz), 122 μs (at 32.768 kHz)
- 842 basic instructions
- General-purpose register: 16 banks
- 15 interrupt sources (External: 6, Internal: 9)
  - All sources have independent latches each
  - Edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- Input/Output ports (71 pins)
- 16-bit timer/counters: 2 channels
  - TC1: Timer, Event counter, PPG (Programable Pulse Generator) output, Pulse width measurement, External trigger timer, Window modes.
  - TC2: Timer, Eventcounter, Window modes.
- 8-bit timer/counters: 2 channels
  - TC3: Timer, Eventcounter, Capture (Pulse width/duty measurment)
  - TC4: Timer, PWM output, PDO (Programmable Divider Output) mode

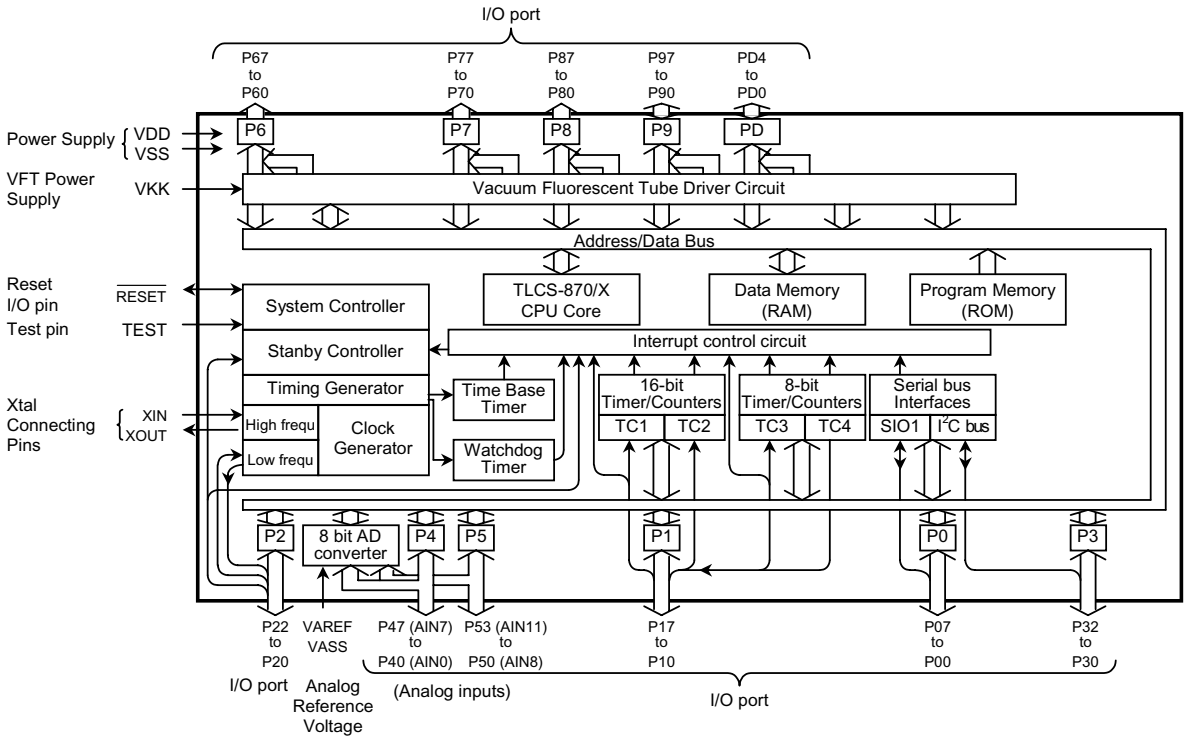
- Time base timer
- Divider output function
- Watchdog timer
  - Interrupt source/reset output (programmable)
- 8-bit serial interface: 1 channel
  - With 8 bytes transmit/receive data buffer
  - Internal/External serial clock, and 4/8-bit mode
- Serial bus interface
  - 8-bit SIO/I²C bus mode
- 8-bit successive approximate type AD converter with sample and hold
  - Analog inputs: 12 channels conversion time: 23 μs at 8 MHz (High-speed conversion mode), 59 μs at 12.5 MHz (Low-speed conversion mode)
- Vacuum fluorescent tube driver (Automatic display)
  - High breakdown voltage ports (Max 40 V × 37 bits)
  - Programmable grid scan output
- Dual clock operation
  - Single/Dual-clock mode (selection)
- Five power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Release by stop pin input.
  - SLOW mode: Low power consumption operation using low-frequency clock.
  - IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupts.
  - SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.
- Wide operating voltage: 2.7 to 5.5 V at 32.8 kHz, 4.5 to 5.5 V at 12.5 MHz/32.8 kHz
- Emulation Pod: BM88CU74F0A

Pin Assignments (Top View)

P-QFP80-1420-0.80B



Block Diagram



Pin Functions (1/2)

Pin Name	Input/Output	Function	
P07 to P03	I/O	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a PPG output or a divider output, the output latch must be set to "1".	
P02 (SO1)	I/O (Output)		SIO1 Serial data Output
P01 (SI1)	I/O (Input)		SIO1 Serial data Input
P00 ($\overline{SCK1}$)	I/O (I/O)		SIO1 Serial clock input/output
P17 (INT4/TC3)	I/O (Input)		External interrupt 4 input or Timer Counter 3 input
P16 (INT2)			External interrupt 2 input
P15 (INT3/TC1)			External interrupt 3 input or Timer Counter 1 input
P14 ($\overline{PDO}$ / $\overline{PWM}$)	I/O (Output)		PWM output or programmable divider output
P13 ($\overline{DVO}$)	I/O (Output)		Divider output
P12 (TC2/ $\overline{PPG}$)	I/O (I/O)		Timer counter input 2 or programmable pulse generator output
P11 (INT1)	I/O (Input)		External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, a resonator connecting pin, an external interrupt input, or a STOP mode release input, the output latch must be set to "1".	Resonator connecting pins (32.8 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$ / $\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P32 ($\overline{SCK0}$)	I/O (Input)	3-bit programmable input/output port (tri-state/programmable open drain). Each bit of the port can be individully configured as an input or an output under software control. When used as a serial interface output, the output latch must be set to "1".	SIO0 clock input/output
P31 (SDA/SO0)	I/O (I/O/Output)		I^2C bus data input/output or SIO0 data output
P30 (SCL/SI0)	I/O (I/O/Input)		I^2C bus clock input/output or SIO0 data input
P47 (AIN7) to P40 (AIN0)	I/O (Input)	8/4-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or output under software control. When used as an analog input set to input mode.	AD converter analog inputs
P53 (AIN13) to P50 (AIN8)	I/O (Input)		
P67 (V7) to P60 (V0)	I/O (Output)	8-bit high breakdown voltage output ports with the latch. When used as an vacuum fluorescent tube driver output, the output latch must be cleared to "0".	VTF output
P77 (V15) to P70 (V8)			
P87 (V23) to P80 (V16)			
P97 (V31) to P90 (V24)			
PD4(V36) to PD0 (V32)		5-bit high breakdown voltage output ports with the latch. When used as an vacuum fluorescent tube driver output, the latch must be cleared to "0".	

Pin Functions (2/2)

Pin Name	Input/Output	Function
XIN, XOUT	Input/Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used an XOUT is opened.
$\overline{\text{RESET}}$	Input/Output	Reset signal input or watchdog timer output/address-reset output/system clock reset output.
TEST	Input	Test pin for out-going teset. Be tied to low.
VDD, VSS	Power Supply	+5 V, 0 V (GND)
VKK		Vacuum fluore scent tube driver voltage pin.
VAREF, VASS		Analog reference voltage input (High, Low)

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer.

This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

TLCS-870/X Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). Figure 1.1.1 shows the memory address maps of the TMP88CU74. It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers.

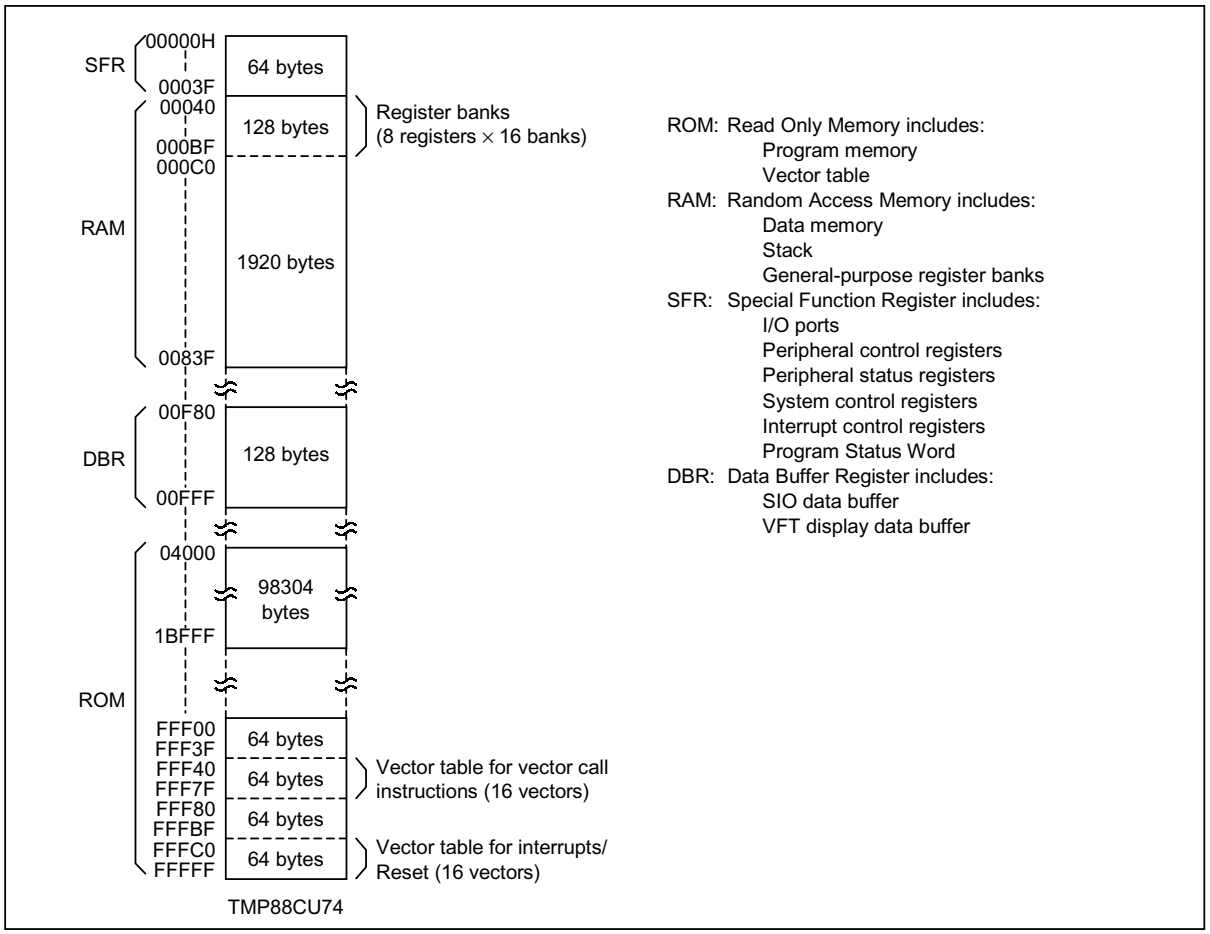


Figure 1.1.1 Memory Address Maps

1.2 Program Memory (ROM)

The TMP88CU74 has a 96 Kbytes (addresses 04000H to 1BFFFH) and 256 bytes (addresses FFF00H to FFFFFH) of program memory (mask programmed ROM). Figure 1.1.1 shown in Memory address maps.

Addresses FFF00H to FFFFFH in the program memory can also be used for special purposes.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		−0.3 to 6.5	V
Input Voltage	V_{IN}		−0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT1}	P2, P3 (at open-drain)	−0.3 to V_{DD} + 0.3	
	V_{OUT2}	P6, P7, P8, P9, PD	V_{DD} − 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P2, P3, P4, P5 Ports	3.2	mA
	I_{OUT2}	P6, P7, P8, P9, PD Ports	−25	
Output Current (Total)	ΣI_{OUT1}	P0, P1, P3, P4, P5 Ports	−40	
	ΣI_{OUT2}	P0, P1, P2, P3, P4, P5 Ports	120	
	ΣI_{OUT3}	P6, P7, P8, P9, PD Ports	−160	
Power Dissipation [Topr = 25°C]	PD (Note 2)		1200	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		−55 to + 125	
Operating Temperature	Topr		−30 to + 70	

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: Power Dissipation (PD); For PD, it is necessary to decrease 14.3 mw/°C.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = −30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 12.5 MHz	NORMAL1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			fs = 32.768 KHz	SLOW modes	2.7		
				SLEEP modes			
				STOP modes	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geq 4.5$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V (Note 2)		8	12.5	MHz
		XTIN, XTOUT	V_{DD} = 2.7 to 5.5 V		30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, Operating temperature range, Specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL 1/2 mode and IDLE 1/2 mode.

How to Calculate Power Consumption.

With the TMP88CU74, a pull-down resistor (R_K = 80 kΩ typ.) can be built into a VFT driver using mask option (port by port). The share of VFT driver loss (VFT driver output loss + pull-down resistor (R_K) loss) in power consumption Pmax is high. When using a fluorescent display tube with a large number of segments, the maximum power consumption P_D must not be exceeded.

Power consumption Pmax = operating power consumption + normal output port loss + VFT driver loss

Where,

1. Operating power consumption: $V_{DD} \times I_{DD}$
2. Normal power consumption: $\Sigma I_{OUT2} \times 0.4$
3. VFT driver loss: VFT driver output loss + pull-down resistor (R_K) loss

Example:

When Ta = 10 to 50°C and a fluorescent display tube with segment output = 3 mA, digit output = 15 mA, Vxx = –25 V is used.

Operating conditions: V_{DD} = 5 V±10%, fc = 12.5 MHz, VFT dimmer time (DIM) = (14/16) × tseg:

Power consumption Pmax = (1) + (2) + (3)

Where, segments pin = X grid pin = Y, Y = 2

1. Operating power consumption: $V_{DD} \times I_{DD}$ = 5.5 V × 20 mA = 110 mW
2. Normal output port loss: $\Sigma I_{OUT2} \times 0.4$ V = 120 mA × 0.4 V = 48 mW
3. VFT driver loss: segment pin = 3 mA × 2 V × number of segmentsX = 6 mW × X × number of gridsY
   digit pin = 15 mA × 2 V × 14/16 (DIM) = 52.5 mW
   R_K loss = $(5.5 + 25\ V)^2/50\ k\Omega$ × (number of segments X + number of digits Y) = 18.605 mW × (X + 2)

Therefore, Pmax = 110 mW + 48 mW + 6 mW × X + 52.5 mW + 18.605 mW × (X + 2)
= 253.71 mW + 24.605 X

Maximum power consumption P_D when Ta = 50°C is determined by the following equation:

$$P_D > Pmax$$
$$842.5\ mW > 253.71 + 24.605\ X$$
$$23.9 > X$$

Thus, a fluorescent display tube with less than 23 segments can be used. If a fluorescent display tube with 23 segments or more is used, either a pull-down resistor must be attached externally , or the number of segments to be lit must be kept to less than 23 by software.

DC Characteristics (V_{SS} = 0 V, Topr = –30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			0.9	—	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V/0 V	—	—	±2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN3}	$\overline{RESET}$		100	220	450	kΩ
Pull-down Resistance	R_K	Source open drain ports	V_{DD} = 5.5 V, V_{KK} = –30 V	50	80	110	
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
	I_{LO2}	Source open drain ports	V_{DD} = 5.5 V, V_{OUT} = –32 V	—	—	–2	
	I_{LO3}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	—	—	2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = –0.7 mA	4.1	—	—	V
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	
Output High current	I_{OH}	P6, P7, P8, P9, PD Port	V_{DD} = 4.5 V, V_{OH} = 2.4 V	—	–20	—	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fc = 12.5 MHz fs = 32.768 kHz	—	18	26	
Supply Current in IDLE 1, 2 modes				—	5.5	8.5	
Supply Current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	—	30	60	μA
Supply Current in SLEEP mode				—	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	—	0.5	10	

Note 1: Typical values show those at Topr = 25°C, VDD = 5 V.

Note 2: Input Current IIN1,IIN3; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

AD Conversion Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = –30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		4.5	—	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}	
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V	—	—	±1	LSB
Zero Point Error			—	—	±1	
Full Scale Error			—	—	±1	
Total Error			—	—	±2	

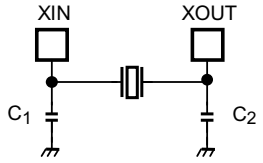
Note: Total errors includes all errors, except quantization error.

AC Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = –30 to 70°C)

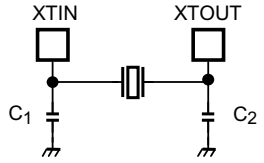
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL1, 2 modes	0.32	—	10	μs
		In IDLE 1, 2 modes				
		In SLOW mode	117.6	—	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 12.5 MHz	33.75	—	—	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	—	—	μs
Low Level Clock Pulse Width	t_{WSL}					

Recommended Oscillating Conditions (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = –30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C_1	C_2
High-frequency Oscillation	Ceramic Resonator	12.5 MHz	Murata	CSA12.5MTZ	30 pF	30 pF
		8 MHz	Murata	CSA8.00MTZ	30 pF	30 pF
	Crystal Oscillator	12.5 MHz	NDK	AT-51	10 pF	10 pF
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;

http://www.murata.co.jp/search/index.html