CMOS 8-Bit Microcontroller

TMP87CH74AF, TMP87CM74AF

The 87CH74A/CM74A are the high speed and high performance 8-bit single chip microcomputers. These MCU contain 8-bit A/D conversion inputs and a VFT (Vacuum Fluorescent Tube) driver on a chip.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CH74AF	16 K × 8-bit	512 × 8-bit	D OFDOO 1430 0 00D	TN4D07DN474F
TMP87CM74AF	32 K × 8-bit	1 K×8-bit	P-QFP80-1420-0.80B	TMP87PM74F

Features

- ◆8-bit single chip microcomputer TLCS-870 Series
- lacktriangle Instruction execution time: 0.5 μ s (at 8 MHz), 122 μ s (at 32.768 kHz)
- 412 basic instructions
 - Multiplication and Division (8 bits x 8 bits, 16 bits ÷ 8 bits)
 - Bit manipulations (Set/Clear/Complement/Load/Store/Test/Exclusive OR)
 - 16-bit data operations
 - 1-byte jump/subroutine-call (Short relative jump/ Vector call)
- ◆15 interrupt sources (External: 6, Internal: 9)
 - All sources have independent latches each, and nested interrupt control is available.
 - 3 edge-selectable external interrupts with noise reject
 - High-speed task switching by register bank changeover
- ◆11 Input/Output ports (71 pins)
 - High current output: 16 pins (typ. 20 mA)
- ▶Two 16-bit Timer/Counters
 - Timer, Event counter, programmable pulse generator output, Pulse width measurement, External trigger timer, Window modes.



- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled
- Quality and Reliability Assurance / Handling Precautions.

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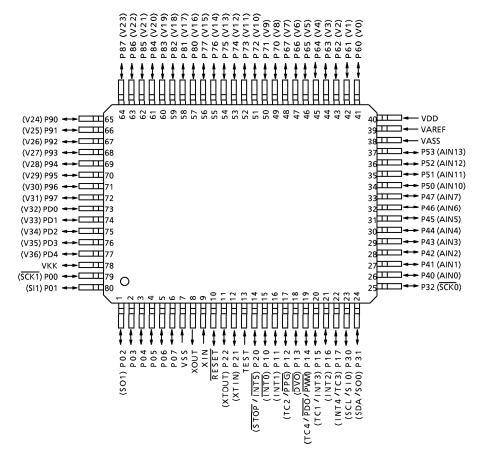
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- ◆Two 8-bit Timer/Counters
 - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider output modes
- ◆Time Base Timer (Interrupt frequency: 1 Hz to 16384 kHz)
- ◆Divider output function (frequency: 1 kHz to 8 kHz)
- **♦**Watchdog Timer
 - Interrupt source/reset output (programmable)
- ◆8-bit Serial Interface
 - With 8 bytes transmit/receive data buffer
 - Internal/external serial clock, and 4/8-bit mode
- ◆ Serial bus Interface
 - I2C-bus, 8-bit SIO modes
- ◆8-bit successive approximate type A/D converter with sample and hold
 - 12 analog inputs
 - Conversion time: 23 μs at 8 MHz
- ◆ Vacuum Fluorescent Tube Driver (automatic display)
 - Programmable grid scan
 - High breakdown voltage ports (max. 40 V × 37 bits)
- ◆ Dual clock operation
 - Single/Dual-clock mode (option)
- ◆ Five Power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
 - SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
 - IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
 - IDLE2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupts.
 - SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.
- ♦ Wide operating voltage: 2.7 to 5.5 V at 32.768 kHz, 4.5 to 5.5 V at 8 MHz / 32.768 kHz
- ◆Emulation Pod: BM87CM75F0A

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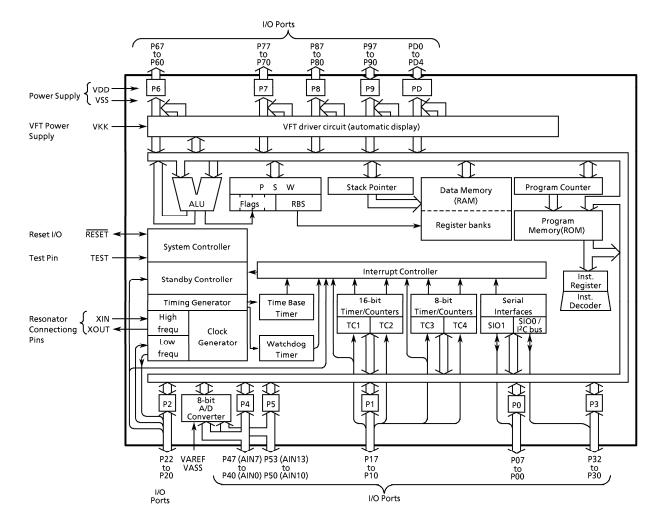
Pin Assignments (Top View)

P-QFP80-1420-0.80B



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Block Diagram



Pin Function

Pin Name	Input / Output	F	unction
P07 to P03	I/O	Two 8-bit programmable	
P02 (SO1)	I/O (Output)	input/output ports (tri-state). Each bit of these ports can be	SIO1 serial data Output
P01 (SI1)	I/O (Input)	individually configured as an input or an output under software control.	SIO1 serial data Input
P00 (SCK1)	I/O (I/O)	When used as a SIO input/output, an	SIO1 serial clock input/output
P17 (INT4/TC3)		External interrupt input, a timer/counter input, the latch must be	External interrupt input 4 or Timer/Counter 3 input
P16 (INT2)	I/O (Input)	set to "0". When used as a PPG output or divider output, the latch	External interrupt input 2
P15 (INT3/TC1)		must be set to "1".	External interrupt input 3 or Timer/Counter 1 input
P14 (TC4/PDO/PWM)	I/O (I/O)		Timer counter 4 input or 8-bit programmable
P13 (DVO)	I/O (Output)		divider output or 8-bit PWM output Divider output
P12 (TC2/ PPG)	I/O (I/O)		Timer counter 2 input or Programmable pulse generator output
P11 (INT1)	1/O (lpp://t)		External interrupt input 1
P10 (ĪNT0)	I/O (Input)		External interrupt input 0
P22 (XTOUT) P21 (XTIN)	I/O (Output)	3-bit input/output port with latch. When used as input port, or external interrupt input, STOP mode release signal input, the latch must be set to	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P20 (INT5/STOP)	ii o (iiipat)	"1".	External interrupt input 5 or STOP mode release signal input
P32 (SCKO)	1/0 (1/0)	3-bit programmable input/output ports (Sink open drain).	SIO0 serial clock input/output
P31 (SDA/SO0)	I/O (I/O/Output)	Each bit of these ports can be individually configured as an input or an output under software control. When used as a I ² C input/output, the	I ² Cbus serial data input/output or SIO0 serial data output
P30 (SCL/SI0)	I/O (I/O/Input)	latch must be set to "1".	l ² Cbus serial clock input/output or SIO0 serial data Input
P47 (AIN7) to P40 (AIN0)	I/O (Input)	8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as a analog input, the P4CR must be set to "0".	A/D converter analog inputs
P53 (AIN13) to P50 (AIN10)	I/O (Input)	4-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as a analog input, the P5CR must be set to "0".	A/D converter analog inputs
P67 (V7) to P60 (V0)		Four 8-bit high brackdown voltage	
P77 (V15) to P70 (V8)		output ports with the latch. When used as a VFT driver output, the	VFT driver outputs
P87 (V23) to P80 (V16)	I/O (Output)	latch must be cleared to "0".	
P97 (V31) to P90 (V24)			
PD4 (V36) toPD0 (V32)	I/O (Output)	5-bit high breakdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".	

Pin Name	Input / Output	Function
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.
RESET	1/0	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset outputted.
TEST	Input	Test pin for out-going test. Be tied to low.
VDD, VSS		+5 V, 0 V (GND)
νκκ	Power Supply	VFT driver power supply
VAREF, VASS		Analog reference voltage inputs (High, Low)

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Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64 Kbytes of memory. Figure 1-1 shows the memory address maps of the 87CH74A/M74A. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

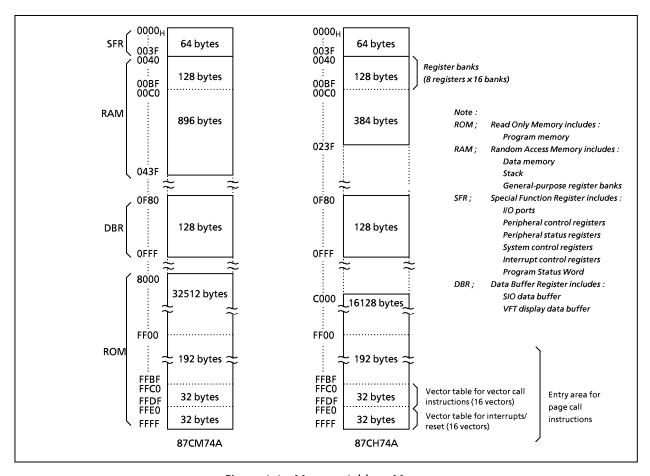


Figure 1-1. Memory Address Maps

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Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		- 0.3 to 6.5	V
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	V
Output Valtage	V _{OUT1}	P2, P3, P4, P5, XOUT, RESET	– 0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT3}	Source open drain ports	V _{DD} – 40 to V _{DD} + 0.3]
	I _{OUT1}	P15 to P17, P3, P4, P5	3.2	
Outrat Comment (Band min)	I _{OUT2}	P0, P10 to P14, P2	30]
Output Current (Per 1 pin)	I _{OUT3}	P8, P9, PD	- 12	mA
	I _{OUT4}	P6, P7	- 25	
	Σ l _{OUT1}	P15 to P17, P3, P4, P5	60	
Output Current (Total)	Σ I _{OUT2}	P0, P10 to P14, P2	160	mA
	Σ I _{OUT3}	P6, P7, P8, P9, PD	- 200]
Power Dissipation [Topr = 25°C]	PD	Note 2	1200	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: Power Dissipation (PD); For PD, it is necessary to decrease 14.3 mw/°C.

Recommended Operating Conditions

 $(V_{SS} = 0 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	c	Conditions		Max	Unit
			fa ONUL	NORMAL 1, 2 modes	4.5		
			fc = 8 MHz	IDLE1, 2 modes	4.5		
Supply Voltage	V_{DD}		fs =	SLOW mode	2.7	5.5	V
			32.768 kHz	SLEEP mode	2.7		
				STOP mode	2.0		
Output Voltage	V _{OUT3}	Source open drain ports			V _{DD} – 38	V_{DD}	٧
	V _{IH1}	Except hysteresis input	V _{DD} ≥4.5 V V _{DD} <4.5 V		$V_{DD} \times 0.70$		V
Input High Voltage	V _{IH2}	Hysteresis input			$V_{DD} \times 0.75$	V _{DD}	
pattingtoage	V _{IH3}				$V_{DD} \times 0.90$		
	V_{IL1}	Except hysteresis input	V >4.5V			$V_{DD} \times 0.30$	
Input Low Voltage	V_{IL2}	Hysteresis input	V _{DD} ≧ 4.5 V		0	$V_{DD} \times 0.25$	V
	V _{IL3}		\	V _{DD} <4.5V		$V_{DD} \times 0.10$	
Clock Frequency		VIN VOLIT	V _{DD} = 4.5 V to 5.5 V		0.4	8.0	
	cy fc XIN, XOUT		V _{DD} = 2.7 V to 5.5 V		0.4	4.2	MHz
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL 1/2 mode and IDLE 1/2 mode.

How to calculate power consumption.

With the TMP87CH74A/M74A, a pull-down resistor (Rk = 80 k Ω typ.) can be built into a VFT driver using mask option. The share of VFT driver loss (VFT driver output loss + pull-down resistor (Rk) loss) in power consumption Pmax is high. When using a fluorescent display tube with a large number of segments, the maximum power consumption Pd must not be exceeded.

power consumption Pmax = operating power consumption + normal output port loss + VFT driver loss

Where,

 $\begin{array}{lll} \text{operating power consumption: VDD x IDD} \\ \text{LED output loss} & : & I_{OL3} \, x \, V_{OL} \end{array}$

VFT driver loss : VFT driver output loss + pull-down resistor (Rk) loss

Example:

When Ta = 10 to 50° C (When using a fluorescent display tube with a grid scan type which can use two or more grid outputs.) and a fluorescent display tube with segment output = 3 mA, digit output = 15 mA, Vxx = -25 V is used.

Operating conditions: VDD = $5 \text{ V} \pm 10 \%$, fc = 8 MHz, VFT dimmer time (DIM) = (14/16) x tseg, Digit outputs = two pin

Power consumption Pmax = (1) + (2) + (3)

Where,

(1) Operating power consumption: $V_{DD} \times I_{DD} = 5.5 \text{ V} \times 14 \text{ mA} = 77 \text{ mW}$

(2) LED output : $10 \text{ mA} \times 1.0 \text{ V} \times 4 = 40 \text{ mW}$ (when using four LED)

(3) VFT driver loss : segment pin = $3 \text{ mA} \times 2 \text{ V} \times \text{number of segments } X = 6 \text{ mW} \times X$

digit pin = $15 \text{ mA} \times 2 \text{ V} \times 14/16$ (DIM) x number of digits Y = 52.5

mW

Rk loss = $(5.5 + 25 \text{ V})^2 / 50 \text{ k}\Omega \text{ x}$ (number of segments X + number

of digits Y) = 18.605 mW x (X + 2)

Therefore, Pmax = 77 mW + 40 mW + 6 mW \times X + 52.5 mW + 18.605 mWx (X + 2) = 206.71 mW + 24.605X...

Maximum power consumption Pd when $Ta = 50^{\circ}C$ is determined by the following equation:

PD = 1200 mW - (14.3 x 25) = 842.5 mW

The number of segments X which can be lit is:

PD > Pmax

 $842.5 \,\text{mW} > 206.71 + 24.605 \,\text{X}$

25.8 > X

Thus, a fluorescent display tube with less than 25 segments can be used. If a fluorescent display tube with 25 segments or more is used, either a pull-down resistor must be attached externally, or the number of segments to be lit must be kept to less than 25 by software.

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D.C. Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input		_	0.9	-	V
	I _{IN1}	TEST					
Input Current	I _{IN2}	Open drain ports, Tri-state ports	V _{DD} = 5.5 V	_	_	± 2	μA
	I _{IN3}	RESET, STOP	V _{IN} = 5.5 V/0 V				
	I _{IN4}	PD ports (Note3)		_	_	80	
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ
Pull-down Resistance	R _K	Source open drain ports	$V_{DD} = 5.5 \text{ V}, V_{KK} = -30 \text{ V}$	50	80	110	kΩ
	I _{LO1}	Sink open drain ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	_	_	2	
Output Leakage Current	I _{LO2}	Source open drain ports and tri-state ports	V _{DD} = 5.5 V, V _{OUT} = -32 V	-	_	- 2	μA
	I _{LO3}	Tri-state ports	$V_{DD} = 5.5 \text{ V}, V_{OUT} = 5.5 \text{ V}/0 \text{ V}$	_	_	± 2	1
Outrout High Maltana	V _{OH2}	Tri-state ports	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1 – –		_	l v
Output High Voltage	V _{OH3}	P8, P9, PD	$V_{DD} = 4.5 \text{ V}, I_{OH} = -8 \text{ mA}$	2.4	-	_	'
Output Low Voltage	V _{OL}	Except XOUT, P0, P10 to P14, P2	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	_	-	0.4	V
Output Low Current	I _{OL3}	P0, P10 to P14, P2	V _{DD} = 4.5 V, V _{OL} = 1.0 V	-	20	-	mΑ
Output High Current	Іон	P6, P7	$V_{DD} = 4.5 \text{ V}, V_{OH} = 2.4 \text{ V}$	_	- 20	_	mA
Supply Current in NORMAL 1, 2 modes			V _{DD} = 5.5 V fc = 8 MHz	-	10	14	
Supply Current in IDLE 1, 2 modes			fs = 32.768 kHz V _{IN} = 5.3 V/0.2 V	_	6	9	mA
Supply Current in SLOW mode	I _{DD}		V _{DD} = 3.0 V	-	30	60	
Supply Current in SLEEP mode			fs = 32.768 kHz V _{IN} = 2.8 V / 0.2 V	-	15	30	μΑ
Supply Current in STOP mode			V _{DD} = 5.5 V V _{IN} = 5.3 V / 0.2 V	-	0.5	10	μΑ

Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 5 V$.

Note 2: Input Current I_{IN1}, I_{IN3}; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Input Current I_{IN4} ; The current when the pull-down register (Rk) is not connected by the mask option.

A/D Conversion Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 6.0 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit	
Analon Beforence Voltage	V_{AREF}	V >25V	V _{DD} 1.5	_	V_{DD}		
Analog Reference Voltage	V _{ASS}	$V_{AREF} - V_{ASS} \ge 2.5 \text{ V}$		V _{SS}		→ ∨	
Analog Input Voltage	V _{AIN}		V _{ASS}	_	V _{AREF}	V	
Analog Supply Current	I _{REF}	V _{AREF} = 5.5 V, V _{ASS} = 0.0 V		0.5	1.0	mA	
Nonlinearity Error			_	_	± 1		
Zero Point Error		$V_{DD} = 5.0 \text{ V}, V_{SS} = 0.0 \text{ V}$	_	_	± 1		
Full Scale Error		V _{AREF} = 5.000 V V _{ASS} = 0.000 V	_	_	± 1	LSB	
Total Error			_	_	± 2		

Note: Total errors includes all errors, except quantization error.

A.C. Characteristics

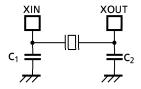
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
		In NORMAL1, 2 modes	0.5		10	
Machine Cycle Time		In IDLE 1, 2 modes	0.5	_		
	t _{cy}	In SLOW mode	117.6			μ S
		In SLEEP mode	117.6	_		
High Level Clock Pulse Width	t _{WCH}	For external clock operation	F0			
Low Level Clock Pulse Width	t _{WCL}	(XIN input), fc = 8 MHz	50	_	_	ns
High Level Clock Pulse Width	t _{WSH}	For external clock operation	14.7			
Low Level Clock Pulse Width	t _{WSL}	(XTIN input), fs = 32.768 kHz	14.7	-	-	μS

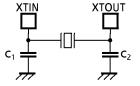
Recommended Oscillating Conditions

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

		Oscillation	Oscillation Recommended Oscillator		Recommended C	
Parameter	Oscillator	Frequency	Recommer	nded Oscillator	C ₁	C ₂
		8 MHz	KYOCERA	KBR8.0M		
	Ceramic Resonator		KYOCERA	KBR4.0MS	30pF	30pF
High-frequency		4 MHz	MURATA	CSA 4.00MG		
Oscillation		8 MHz	тоуосом	210B 8.0000		
	Crystal Oscillator	4 MHz	тоуосом	204B 4.0000	20pF	20pF
Low-frequency Oscillation	Crystal Oscillator	32.768 KHz	NDK	MX-38T	15pF	15pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note: An electrical shield by metal shield plate on the surface of IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.