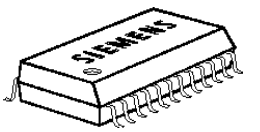
SIEMENS

Intelligent Double 4-A Low-Side Switch — TLE 5224

Preliminary Data — **SPT-IC**

Features

- Double low-side switch (2 x 4 A)
- Low ON-resistance (typical 0.25 Ω)
- Power limitation
- Overtemperature shutdown
- Overload shutdown
- Status monitoring
- Integrated clamp Z-diode
- Shorted load protecting
- Temperature range: – 40 to 85 ˚C

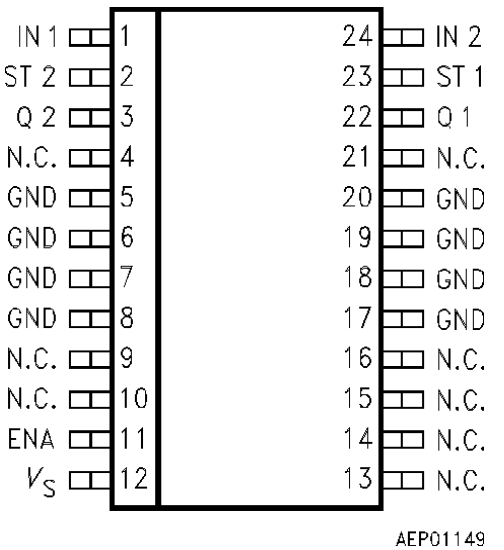


P-DSO-24-3

	Type	Ordering Code	Package
▼	TLE 5224 G	Q67000-A9116	P-DSO-24-3 (SMD)

▼ New type

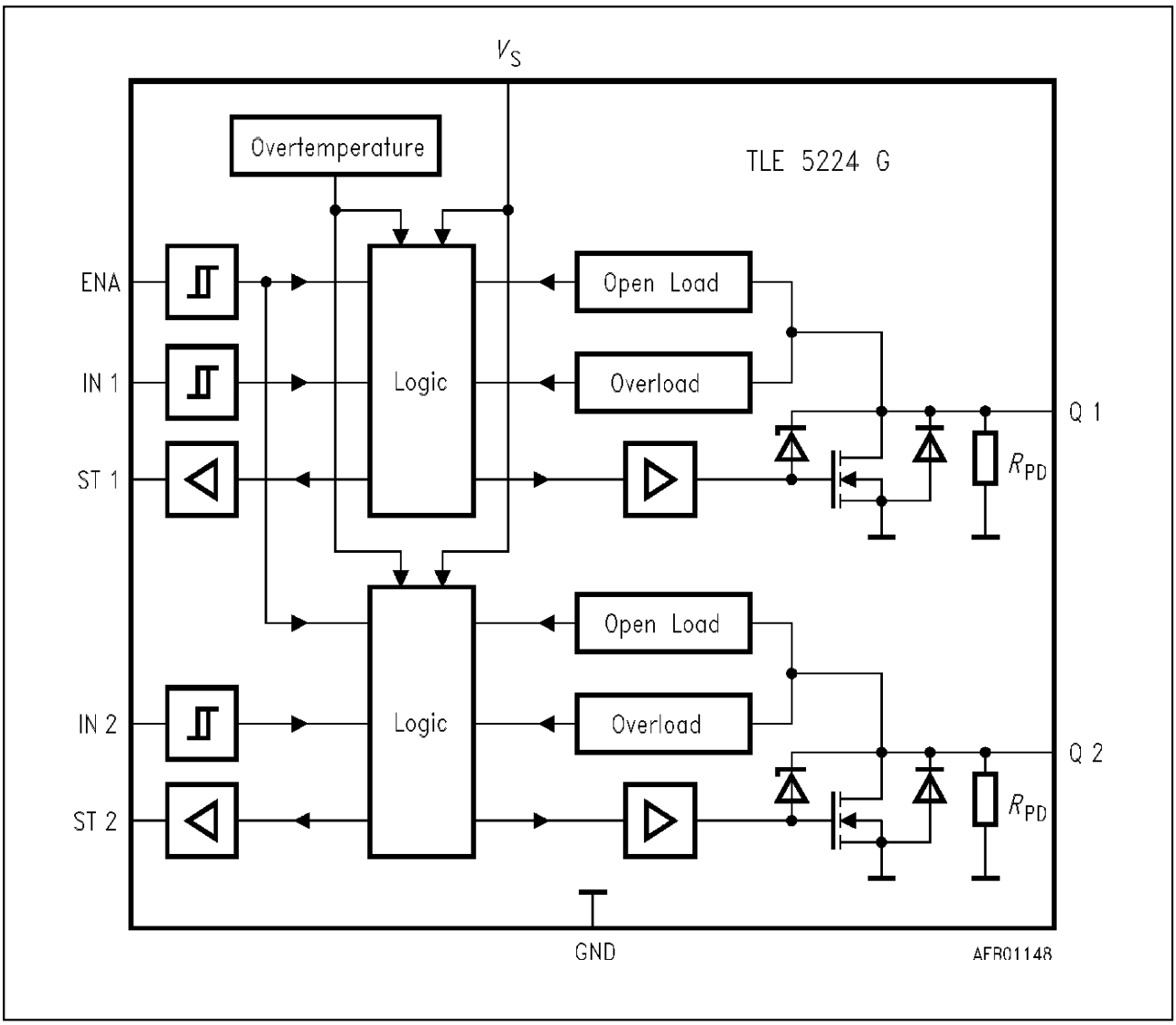
The TLE 5224 G is an integrated double low-side power switch with power limitation, load interrupt and shorted load detection, temperature monitoring, error signaling via two status outputs and integrated Z-diodes for output clamping. The TLE 5224 G is designed for automotive applications.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	IN1	Control input channel 1
2	ST2	Status output channel 2
3	Q2	Power output channel 2
4	N.C.	Not connected, cooling
5, 6, 7, 8	GND	Ground, cooling
9, 10	N.C.	Not connected, cooling
11	ENA	Enable input for both channels
12	V_S	Supply voltage
13, 14, 15, 16	N.C.	Not connected, cooling
17, 18, 19, 20	GND	Ground, cooling
21	N.C.	Not connected, cooling
22	Q1	Power output channel 1
23	ST1	Status output channel 1
24	IN2	Control input channel 2



Block Diagram

Application Description

This IC is specially designed to drive inductive loads (relays, electromagnetic valves). Integrated clamp-diodes limit the discharging EMF during switch off when inductive loads are turned off.

For the detection of errors there are two status outputs, which monitor the following errors by logic levels:

- thermal overload,
- open and shorted load to ground in active and inactive mode,
- overloading of output (also shorted load to supply) in active mode.

Circuit Description

Input Circuits

The control and enable inputs, all active high, consist of Schmitt triggers with hysteresis. All inputs are connected with pull-down current sources. Not connected inputs are interpreted as "low".

Switching Stages

The power outputs consist of a DMOS power transistor with open drain. The output stages are shorted-load-protected throughout the operating range. Integrated clamp diodes limit voltage spikes produced when inductive loads are discharged.

Protective Circuit

The outputs are protected against current overload and thermal overload. There is no protection against reverse polarity of the supply voltage.

Error Detection

The status outputs signal the status of the switching stages at normal operation (LOW = OFF; HIGH = ON). In case of any error the status outputs are set according to the table below.

If current overload occurs, the error condition is stored in an internal register and the output is shutdown. To reset this register the control input of the affected channel has to be switched off and then on again.

The state of the error detection circuit is directly dependent on the input status.

In case of thermal overload both channels will be shutdown. If any other error condition occurs, only the affected channel will be switched off (not influencing the power or status output of the second, non-affected channel).

Open load is detected in on-and off-modus: In on-modus the load current is monitored, in the off-modus the output voltage is compared with the supply voltage to detect an open load condition. Therefore internal pull-down resistors are connected from output to ground.

The state of the error detection circuit is directly dependent on the input status.

Diagnostic Table

Operating Condition	Inputs			Power Outputs		Status Outputs	
	ENA	**IN1**	**IN2**	**Q1**	**Q2**	**ST1**	**ST2**
Normal Function	L H H H H	X L H L H	X L L H H	OFF OFF ON OFF ON	OFF OFF OFF ON ON	L L H L H	L L L H H
Overtemperature	X X X X	L H L H	L L H H	OFF OFF OFF OFF	OFF OFF OFF OFF	H L H L	H H L L
Open Load Channel 1	X L H	L H H	X X X	OFF OFF ON	1)	H H L	1)
Open Load Channel 2	X L H	X X X	L H H	1)	OFF OFF ON	1)	H H L
Overload Channel 1	L H H	X L H	X X X	OFF OFF OFF	1)	L L L	1)
Overload Channel 2	L H H	X X X	X L H	1)	OFF OFF OFF	1)	L L L

1) Power and status outputs according to normal function

Absolute Maximum Ratings

T_A = – 40 to 85 ˚C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 0.3	60	V	–
Output voltage	$V_{Q1, 2}$	–	45	V	–
Output voltage	$V_{Q1, 2}$	–	65	V	$t \leq 1$ ms
Output voltage	V_{ST}	– 0.3	45	V	–
Input voltage	$V_{IN1, IN2, ENA}$	– 1.5	6	V	$I_I < 10$ mA
Currents					
Output current	$I_{Q1, 2}$	5	–	A	limited internally;
Current at reverse poling	$I_{Q1, 2}$; I_{GND}	– 4	–	A	–
Output current, status pin	I_{ST}	– 5	5	mA	–
Discharging energy of inductive load per channel	E	–	50	mJ	$T_j \leq 25$ ˚C
Junction temperature	T_j	– 40	150	˚C	–
Junction temperature	T_j	–	175	˚C	during clamping
Storage temperature	T_{stg}	– 50	150	˚C	–
Operating Range					
Supply voltage	V_S	4.8	45	V	–
Supply voltage rise	dV_S/d_t	– 1	1	V/µs	–
Output voltage	$V_{Q1, 2}$ $V_{Q1, 2}$	– 0.3 –	45 65	V V	– during clamping
Reverse current into inputs	$I_{IN1, IN2, ENA}$	– 10	–	mA	–
Output voltage	V_{ST}	– 0.3	45	V	–
Output current	I_{ST}	0	2	mA	–
Ambient temperature	T_A	– 40	85	˚C	$T_j \leq 150$ ˚C
Chip temperature	T_j	–	175	˚C	during clamping
Thermal resistance junction to case junction to ambient	 $R_{th\ JC}$ $R_{th\ JA}$	 – –	 12 75	 K/W K/W	 1) –

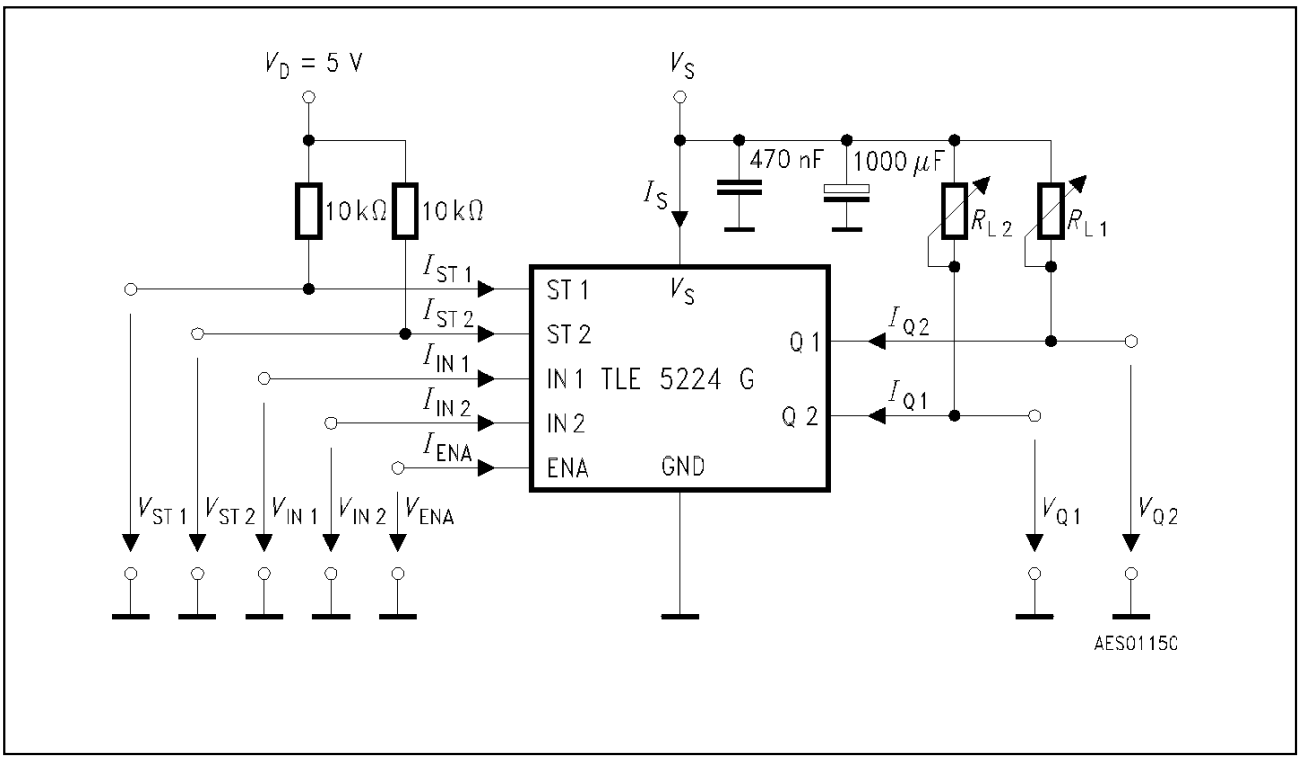
1) Pins 4 to 10 and 13 to 21 have to be connected to the ground-plane used as thermal heatsink to achieve the optimum thermal resistance.

Characteristics

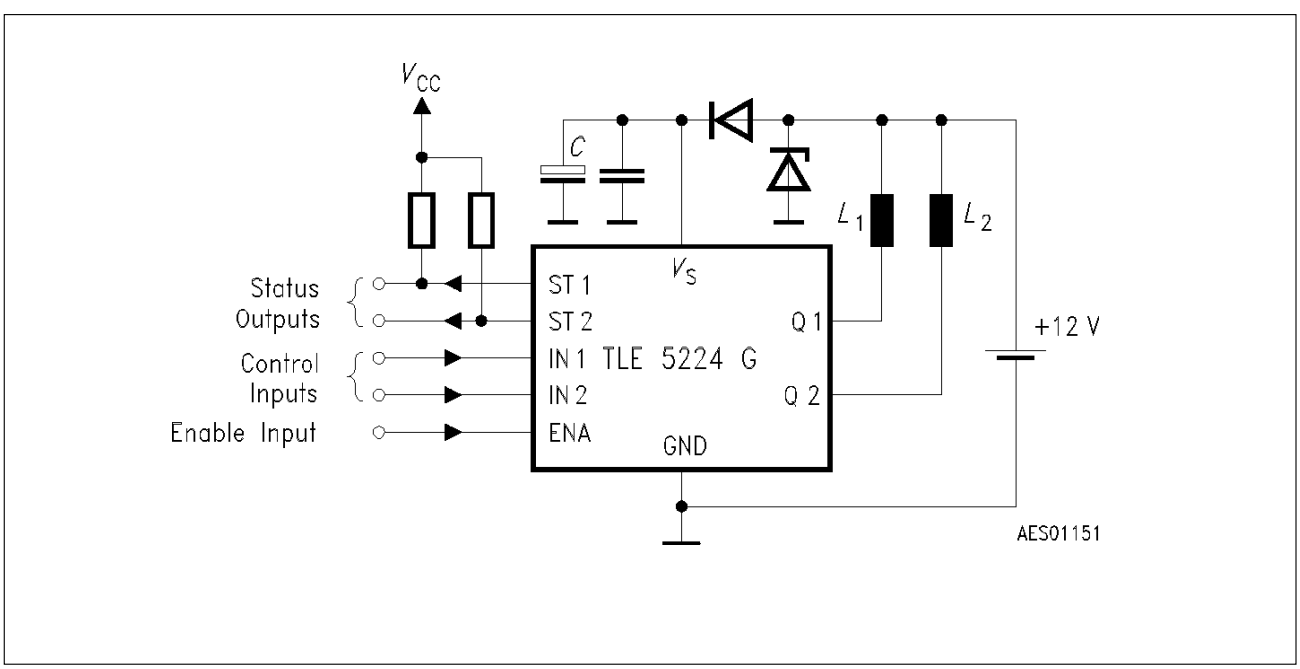
V_S = 6.5 to 45 V; typ. V_S = 12 V; T_j = – 40 to 150 °C, V_D = 5.1 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current	I_S	–	0.6	1	mA	Outputs OFF; $V_S \leq 18$ V
Supply current	I_S	–	1.8	3	mA	Outputs ON; $V_S \leq 18$ V
	I_S			4	mA	Outputs ON; V_S = 45 V
Open load current	I_{Qu}	–	–	250	mA	Output ON
Open load voltage threshold	V_{Qu}	6.2	–	7.0	V	Output OFF; V_S = 12 V
	V_{Qu}	0.515	–	0.585	* V_S	Output OFF; $V_S \leq 18$ V
Overload current	I_{QO}	5.25	–	–	A	Output ON; T_j = 25 °C
	I_{QO}	4	–	–	A	Output ON; T_j = 150 °C
Overtemperature shutdown threshold	T_{th}	155	–	185	°C	only a design value
Hysteresis	ΔT_{th}	–	10	–	K	only a design value
Power Output						
Static drain source ON-resistance	R_{DSON}	–	0.25	–	Ω	T_j = 25 °C
	R_{DSON}	–	–	0.5	Ω	T_j = 150 °C; I_Q = 4 A; $V_S \geq 9.5$ V
Pull-down resistance	R_{PD}	14	20	26	kΩ	T_j = 25 °C
Clamping Voltage	V_{QZ}	45	–	65	V	–
Input (IN1; IN2; ENA)						
H-Input voltage	V_{IH}	2.0	–	6.0	V	–
L-Input voltage	V_{IL}	– 0.3	–	1.0	V	–
Hysteresis	ΔV_I	0.2	–	0.6	V	–
H-input current	$I_{IN1\ ;\ IN2}$	50	100	140	µA	V_{IN1} = 5 V
H-input current	I_{ENAH}	15	30	40	µA	V_{ENA} = 5 V
Status Output						
L-output voltage	V_{ST}	–	–	0.5	V	I_{ST} = 2 mA
H-leakage current	I_{STH}	–	–	2	µA	
Output ON delay time	t_1	10	25	40	µs	I_Q = 0.2 A [2]
Output ON fall time	t_2	–	20	–	µs	I_Q = 0.2 A [2]
Output OFF rise time	t_3	–	25	–	µs	I_Q = 2 A [2]
Output OFF status Delay time	t_4	20	40	60	µs	I_Q = 2 A [2]
Output ON status Delay time	t_5	–	–	50	µs	[1]
Overload switch-OFF Delay time	t_{dSO}	50	–	150	µs	only a design value

1) Time between status valid and switching on or error detection.
2) See timing diagram; resistive load condition; $V_S \geq 9$ V

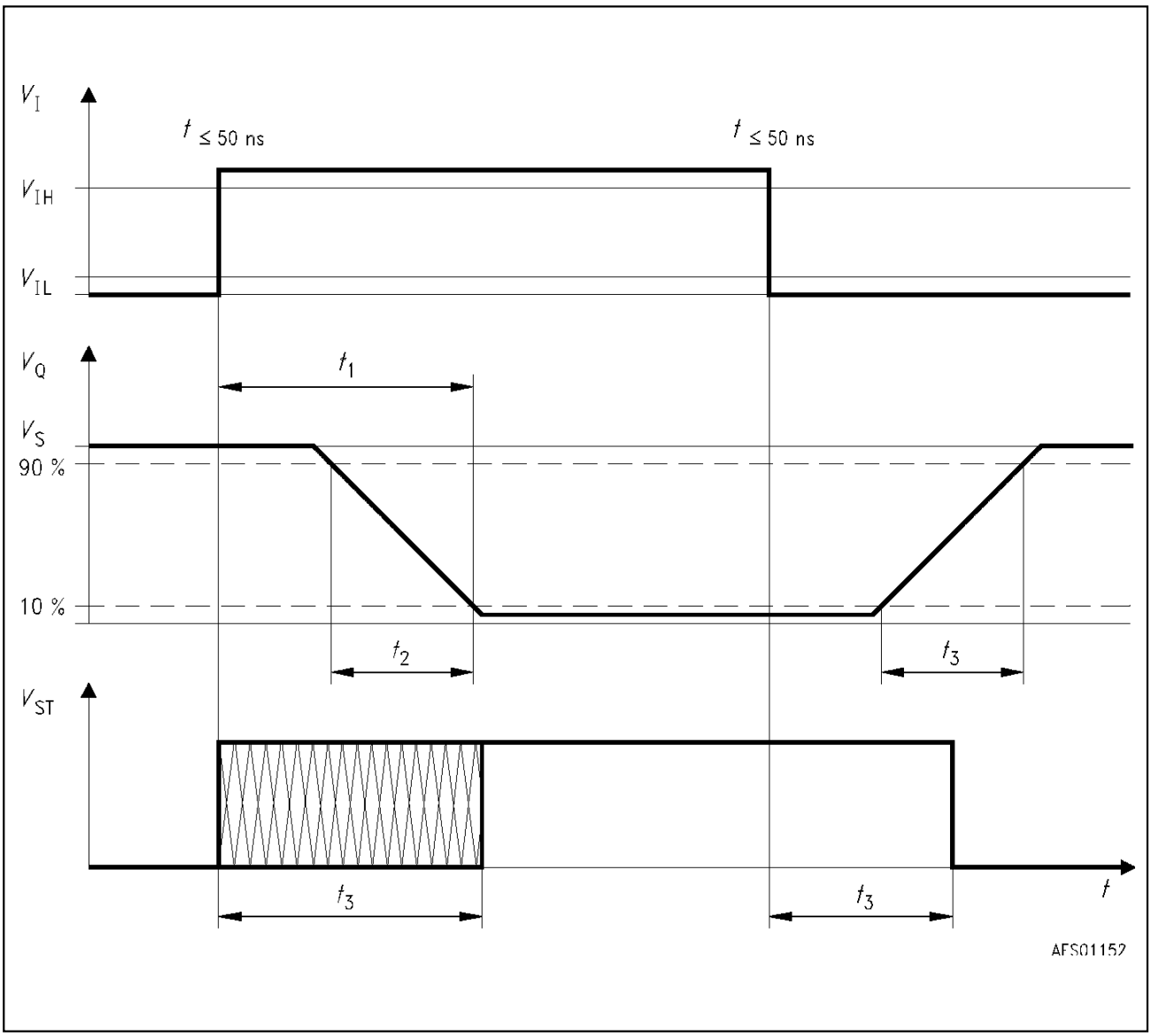


Test Circuit



Application Circuit

The blocking capacitor C is recommended to avoid critical negative voltage spikes on V_S in case of battery interruption during off-communicating.



Timing Diagram

Overload Current versus Temperature