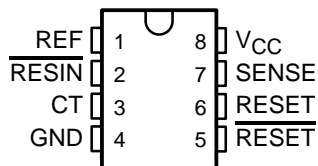


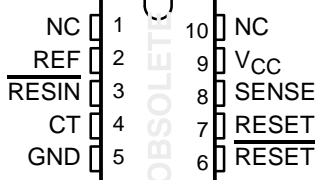
The TL7705BM is obsolete
and no longer is supplied.

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- $\overline{\text{RESET}}$ Output Defined From $V_{CC} \geq 1 \text{ V}$
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- True and Complement Reset Outputs
- Externally Adjustable Pulse Duration

TL77xxBC ... D OR P PACKAGE
TL7705BM ... JG PACKAGE
TL7705BQ ... D PACKAGE
(TOP VIEW)

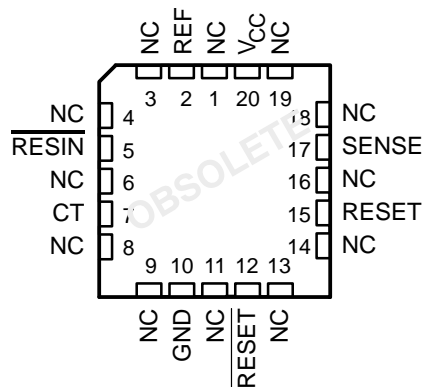


TL7705BM ... U PACKAGE
(TOP VIEW)



NC – No internal connection

TL7705BM ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The TL7702B, TL7705B, and TL7733B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay-timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T . $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL7702BC, TL7705BC, and TL7733BC are characterized for operation from 0°C to 70°C. The TL7702BI, TL7705BI, and TL7733BI are characterized for operation from –40°C to 85°C. The TL7705BQ is characterized for operation from –40°C to 125°C. The TL7705BM is characterized for operation from –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TL7702B, TL7705B, TL7733B SUPPLY-VOLTAGE SUPERVISORS

The TL7705BM is obsolete
and no longer is supplied.

SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

description/ordering information (continued)

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	TL7702BCP	TL7702BCP
	SOIC (D)	Tube of 75	TL7702BCD	7702BC
		Reel of 2500	TL7702BCDR	
	PDIP (P)	Tube of 50	TL7705BCP	TL7705BCP
	SOIC (D)	Tube of 75	TL7705BCD	7705BC
		Reel of 2500	TL7705BCDR	
	PDIP (P)	Tube of 50	TL7733BCP	TL7733BCP
	SOIC (D)	Tube of 75	TL7733BCD	7733BC
		Reel of 2500	TL7733BCDR	
–40°C to 85°C	PDIP (P)	Tube of 50	TL7702BIP	TL7702BIP
	SOIC (D)	Tube of 75	TL7702BID	7702BI
		Reel of 2500	TL7702BIDR	
	PDIP (P)	Tube of 50	TL7705BIP	TL7705BIP
	SOIC (D)	Tube of 75	TL7705BID	7705BI
		Reel of 2500	TL7705BIDR	
	PDIP (P)	Tube of 50	TL7733BIP	TL7705BIP
	SOIC (D)	Tube of 75	TL7733BID	7733BI
		Reel of 2500	TL7733BIDR	
–40°C to 125°C	SOIC (D)	Tube of 75	TL7705BQD	TL7705BQD

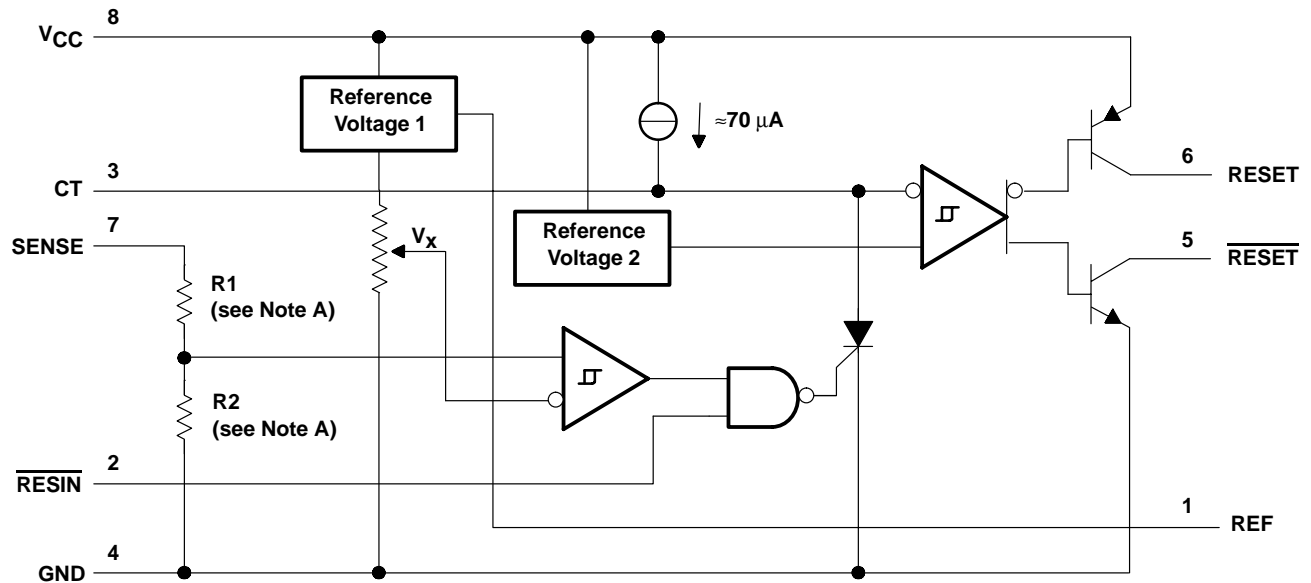
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

The TL7705BM is obsolete
and no longer is supplied.

SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



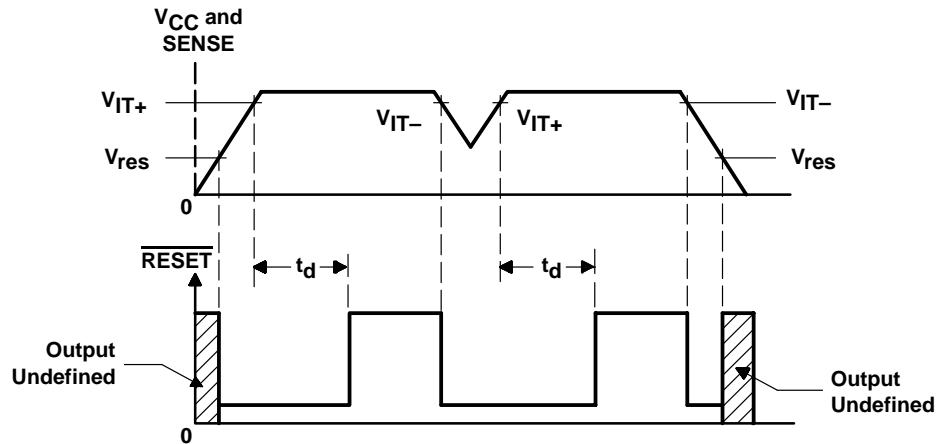
Pin numbers shown are for the D, JG, and P packages.

NOTE A: TL7702B: R1 = 0 Ω, R2 = open, $V_X = V_{REF1}$

TL7705B: R1 = 23 kΩ, R2 = 10 kΩ, nominal, $V_X \approx 1.43$ V

TL7733B: R1 = 11.3 kΩ, R2 = 10 kΩ, nominal, $V_X \approx 1.43$ V

typical timing diagram



TL7702B, TL7705B, TL7733B SUPPLY-VOLTAGE SUPERVISORS

The TL7705BM is obsolete
and no longer is supplied.

SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I : $\overline{\text{RESIN}}$	–0.3 V to 20 V
SENSE	–0.3 V to 20 V
High-level output current, I_{OH} (RESET)	–30 mA
Low-level output current, I_{OL} (RESET)	30 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package	97°C/W
P package	85°C/W
Operating virtual junction temperature, T_J	150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or U packages	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P packages	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.6	18	V
V_{IH}	High-level input voltage	$\overline{\text{RESIN}}$	2	18	V
V_{IL}	Low-level input voltage	$\overline{\text{RESIN}}$	0	0.8	V
V_I	Input voltage	SENSE	0	18	V
I_{OH}	High-level output current	RESET		–20	mA
I_{OL}	Low-level output current	RESET		20	mA
T_A	Operating free-air temperature range	TL77xxBC	0	70	°C
		TL77xxBI	–40	85	
		TL7705BQ	–40	125	
		TL7705BM	–55	125	

The TL7705BM is obsolete
and no longer is supplied.

SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONST		TL77xxBC TL77xxBI TL7705BQ			UNIT	
					MIN	TYP	MAX		
VOH	High-level output voltage, RESET		IOH = −16 mA		VCC−1.5			V	
VOL	Low-level output voltage, RESET		IOL = 16 mA		0.4			V	
Vref	Reference voltage, REF		Iref = −500 μA,	TA = 25°C	2.48	2.53	2.58	V	
VIT−	Negative-going input threshold voltage at SENSE input	TL7702B	TA = 25°C		2.505	2.53	2.555	V	
		TL7705B			4.5	4.55	4.6		
		TL7733B			3.03	3.08	3.13		
		TL7702B	TA = full range‡		2.48	2.53	2.58		
		TL7705B			4.45	4.55	4.65		
		TL7733B			3	3.08	3.16		
Vhys	Hysteresis, SENSE (VIT+ − VIT−)	TL7702B	VCC = 3.6 V to 18 V, TA = 25°C		10			mV	
		TL7705B			30				
		TL7733B			10				
Vres§	Power-up reset voltage		IOL at RESET = 2 mA, TA = 25°C		1			V	
II	Input current	RESIN		VI = 0.4 V to VCC		−10			μA
		SENSE	TL7702B	VI = Vref to 18 V		−0.1 −2			
IOH	High-level output current, RESET		VO = 18 V, See Figure 1		50			μA	
IOL	Low-level output current, RESET		VO = 0 V, See Figure 1		−50			μA	
ICC	Supply current		VSENSE = 15 V, RESIN ≥ 2 V		1.8 3			mA	
			VCC = 18 V, TA = full range‡		3.5				

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

‡ Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –40°C to 125°C for the Q-suffix device.

§ This is the lowest voltage at which RESET becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL77xxBC TL77xxBI TL7705BQ			UNIT
					MIN	TYP	MAX	
t _{PLH}	Propagation delay time from low- to high-level output	RESIN	RESET	See Figures 1, 2, and 3		270	500	ns
t _{PHL}	Propagation delay time from high- to low-level output	RESIN	RESET	See Figures 1, 2, and 3		270	500	ns
t _w	Effective pulse duration	RESIN		See Figure 2		150		ns
		SENSE				100		
t _r	Rise time		RESET	See Figures 1 and 3			75	ns
t _f	Fall time					150	200	
t _r	Rise time		RESET	See Figures 1 and 3			75	ns
t _f	Fall time						50	

TL7702B, TL7705B, TL7733B SUPPLY-VOLTAGE SUPERVISORS

The TL7705BM is obsolete
and no longer is supplied.

SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITION†	TL7705BM			UNIT
					MIN	TYP	MAX	
V _{OH}	High-level output voltage, RESET			I _{OH} = −16 mA	V _{CC} −1.5			V
V _{OL}	Low-level output voltage, RESET			I _{OL} = 16 mA	0.4			V
V _{ref}	Reference voltage, REF			I _{ref} = −500 μA, T _A = 25°C	2.48	2.53	2.58	V
V _{IT−}	Negative-going input threshold voltage at SENSE input		TL7702B	T _A = 25°C	2.505	2.53	2.555	V
			TL7705B		4.5	4.55	4.6	
			TL7702B	T _A = −55°C to 125°C	2.48	2.53	2.58	
			TL7705B		4.45	4.55	4.65	
V _{hys}	Hysteresis, SENSE (V _{IT+} − V _{IT−})		TL7702B	V _{CC} = 3.6 V to 18 V, T _A = 25°C	10			mV
			TL7705B		30			
V _{res} ‡	Power-up reset voltage			I _{OL} at RESET = 2 mA, T _A = 25°C	1			V
I _I	Input current	RESIN		V _I = 0.4 V to V _{CC}	−10			μA
		SENSE	TL7702B	V _I = V _{ref} to V _{CC} − 1.5 V	−0.1 −2			
I _{OH}	High-level output current, RESET			V _O = 18 V	50			μA
I _{OL}	Low-level output current, RESET			V _O = 0	−50			μA
I _{CC}	Supply current			V _{SENSE} = 15 V, RESIN ≥ 2 V	1.8		3	mA
				V _{CC} = 18 V, T _A = −55°C to 125°C	4			

[†] All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

[‡] This is the lowest value at which RESET becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

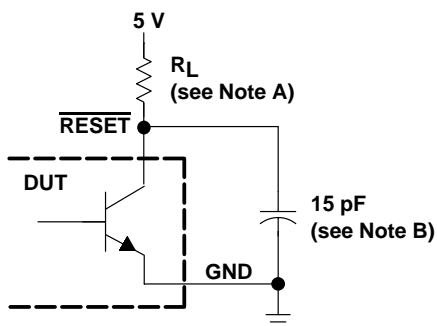
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7705BM			UNIT
					MIN	TYP	MAX	
t _{PLH}	Propagation delay time from low- to high-level output	RESIN	RESET	See Figures 1, 2, and 3		270	500*	ns
t _{PHL}	Propagation delay time from high- to low-level output	RESIN	RESET	See Figures 1, 2, and 3		270	500*	ns
t _w	Effective pulse duration	RESIN		See Figure 2		150		ns
		SENSE				100		
t _r	Rise time		RESET	See Figures 1 and 3		75*		ns
t _f	Fall time					150	200*	
t _r	Rise time		RESET	See Figures 1 and 3		75	150*	ns
t _f	Fall time						50*	

* On products compliant to MIL-PRF-38535, these parameters are not production tested.

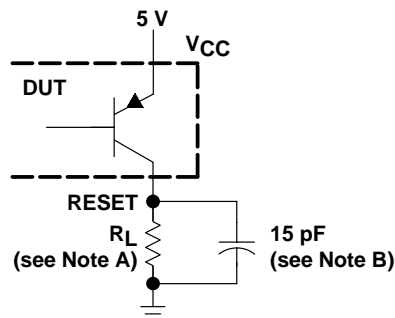


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



RESET OUTPUT CONFIGURATION



RESET OUTPUT CONFIGURATION

NOTES: A. For I_{OL} and I_{OH} , $R_L = 10\text{ k}\Omega$. For all switching characteristics, $R_L = 511\text{ }\Omega$.
B. This figure includes jig and probe capacitance.

Figure 1. RESET and RESET Output Configurations



WAVEFORMS

Figure 2. Input Pulse Definition

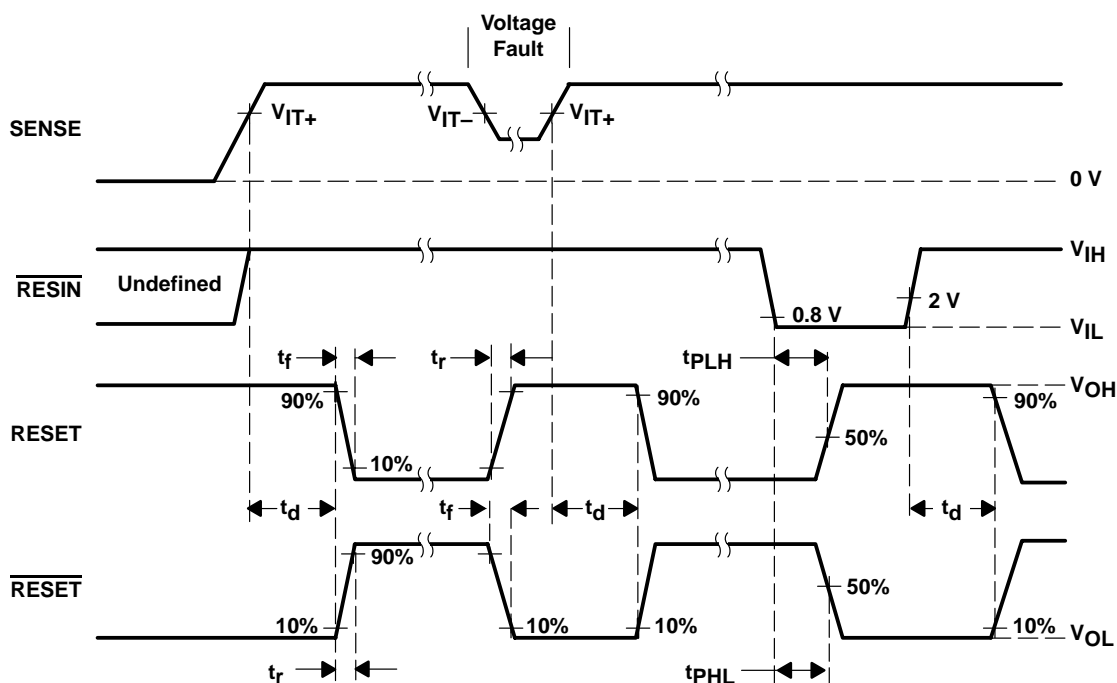


Figure 3. Voltage Waveforms

TYPICAL CHARACTERISTICS†

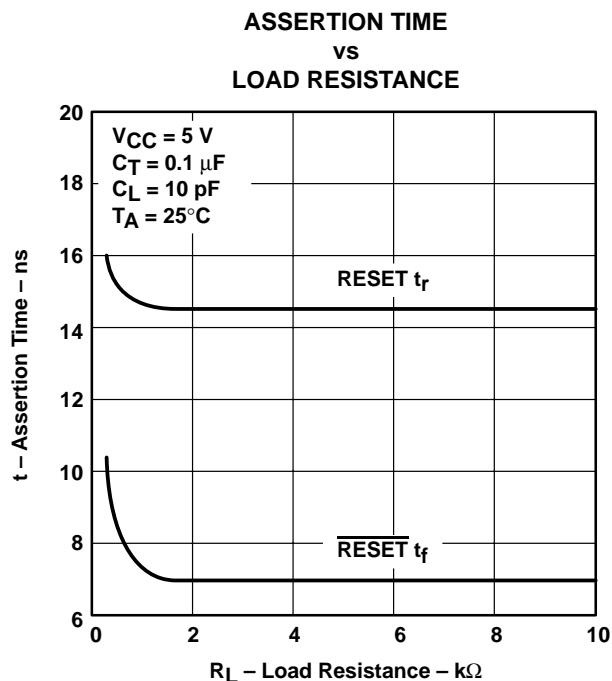


Figure 4

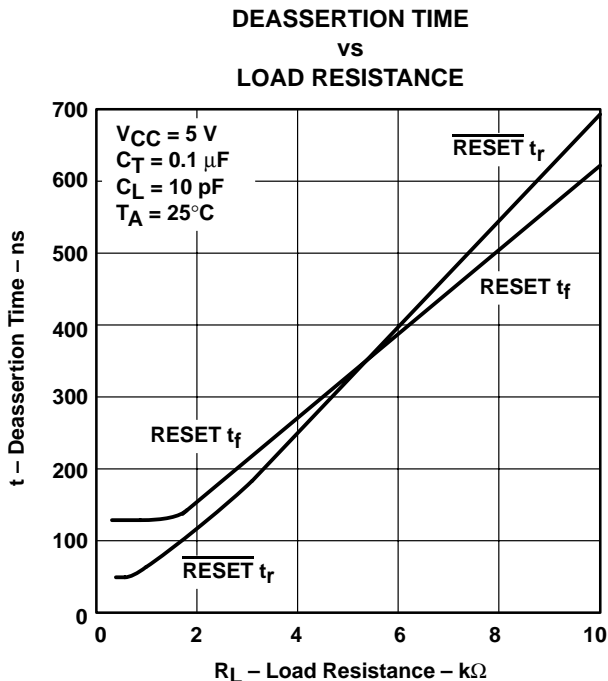


Figure 5

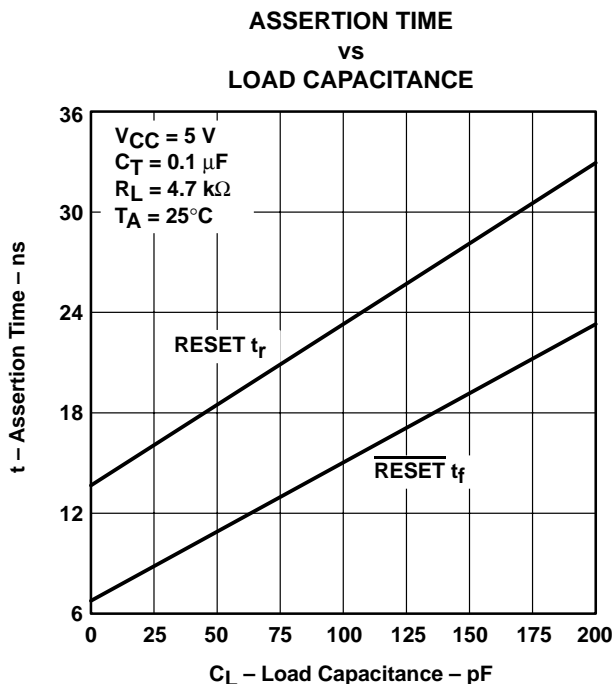


Figure 6

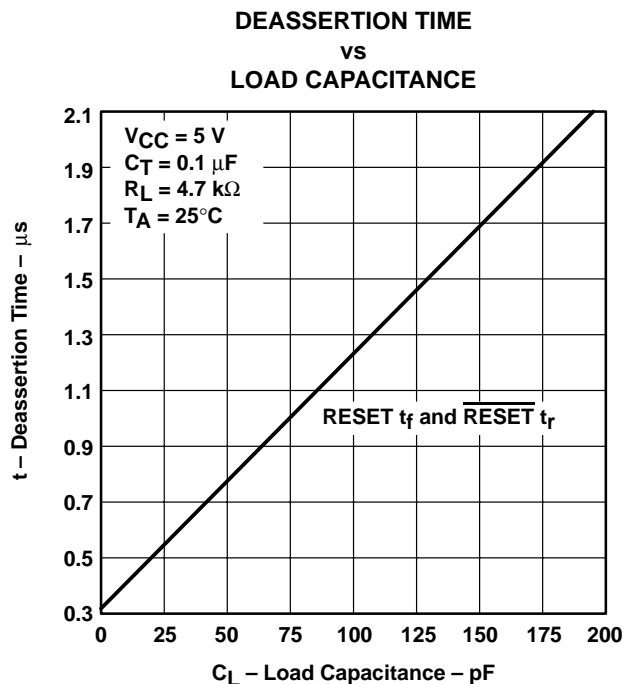


Figure 7

† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

APPLICATION INFORMATION

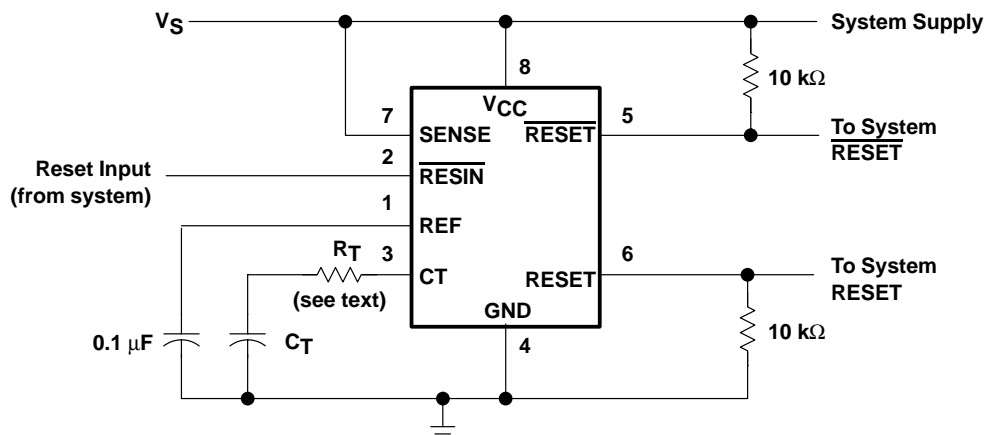


Figure 8. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC} , a current-limiting resistor in series with C_T is recommended. During normal operation, the timing capacitor is charged by the onboard current source to approximately V_{CC} or an internal voltage clamp (≈ 7.1 -V Zener), whichever is less. When the circuit then is subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on CT exceeds that on V_{CC} . This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below V_{T-} .

Texas Instruments performs a 100% electrical screen to verify that the outputs do not switch with 1 mA forced into the CT terminal. Adding the external resistor, R_T , prevents false triggering. Its value is calculated as follows:

$$\frac{V_{(CT)} - V_{T-}}{R_T}$$

Where:

$$\begin{aligned} V_{(CT)} &= V_{CC} \text{ or } 7.1 \text{ V, whichever is less} \\ V_{T-} &= 4.55 \text{ V (nom)} \\ R_T &= \text{value of series resistor required} \end{aligned}$$

For $V_{CC} = 5 \text{ V}$:

$$\frac{5 - 4.55}{R_T} < 1 \text{ mA}$$

Therefore,

$$R_T > 450 \text{ } \Omega$$

Using a 20%-tolerance resistor, R_T should be greater than 560 Ω .

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T , but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply-voltage fault condition.

Both outputs of the TL770xB should be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-88685042A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
5962-8868504HA	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	
5962-88685052A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
5962-8868505HA	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	
5962-8868505PA	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL7702BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7702BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7702BID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7702BIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7702BIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TL7702BMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL7702BMJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL7702BMJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL7702BMUB	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	
TL7702BQD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL7702BQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL7702BQP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL7705BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7705BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7705BID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL7705BIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TL7705BIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7705BMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL7705BMJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL7705BMJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL7705BMUB	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	
TL7705BQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7705BQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7705BQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7705BQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7705BQP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL7733BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7733BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7733BID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TL7733BIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL7733BIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL7733BIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7702BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7702BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7702BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705BQDR	SOIC	D	8	2500	367.0	367.0	35.0
TL7733BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7733BIDR	SOIC	D	8	2500	340.5	338.1	20.6

JG (R-GDIP-T8)

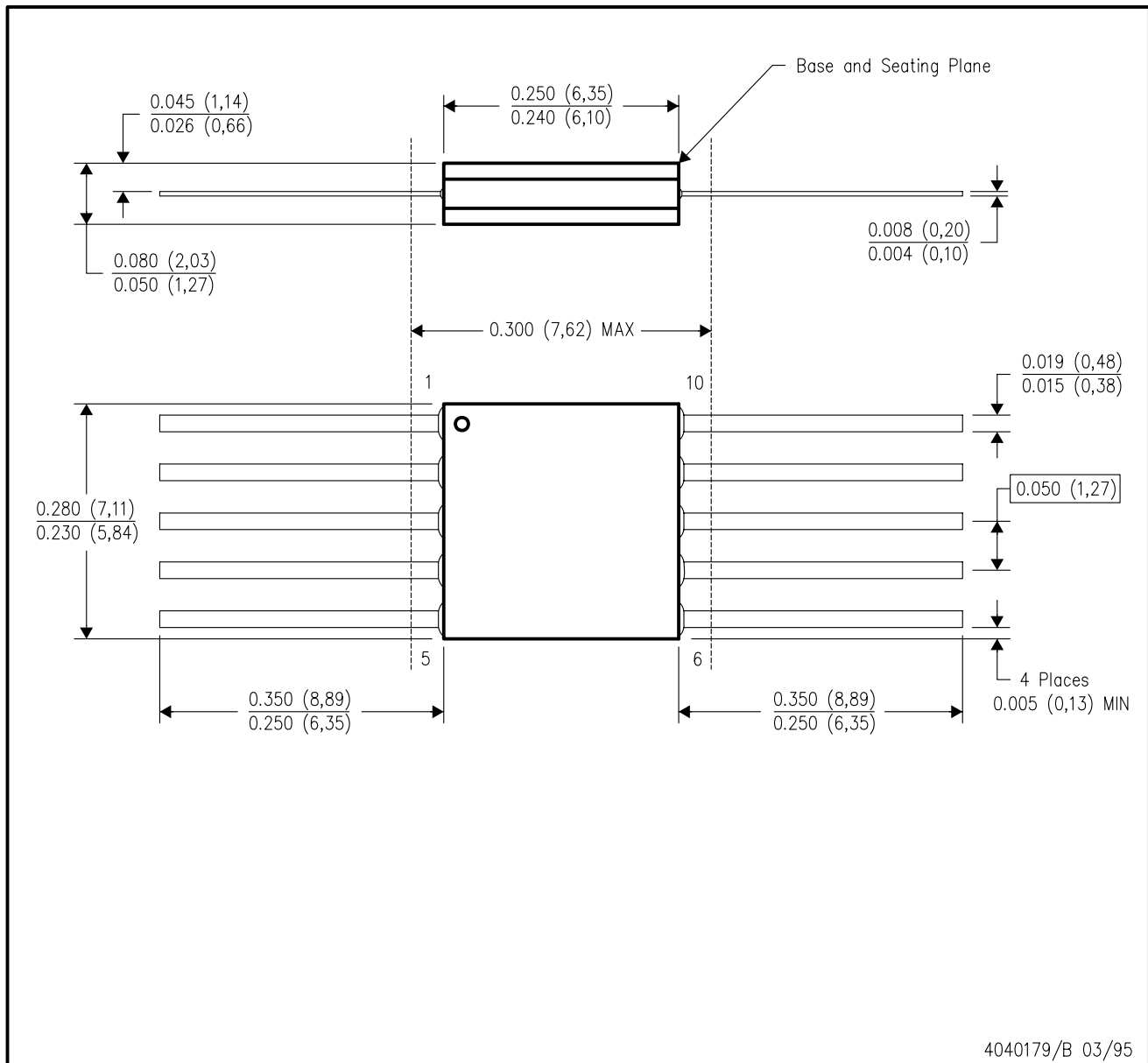
CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification.
 - E. Falls within MIL STD 1835 GDIP1-T8

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community e2e.ti.com