- **Industrial Temperature Version of the TFB2022A With an Operating Range of −20°C to 85°C**
- **Parallel-Protocol Support Is Fully Compliant to Futurebus+ Standard (IEEE Std 896.1−1991)**
- **Interfaces Easily to a Variety of Popular Microprocessors Such as SPARC™, 680x0, 88xxx, 80x86, and Alpha AXP™**
- **Can Be Used in Conjunction With the TFB2002A Futurebus+ I/O Controller or Standalone With a User-Defined Controller**
- **64 Data Channels and 8 Parity Channels on Board**
- **Supports 32 or 36 Bits of Addressing**
- **On-Board Address Decoding Determines Whether Transaction Is to Host Memory, Extended Unit Space, Message-Passing Mailbox, or Other CSR Location**
- **Parallel-Protocol-Related CSR Locations Are Provided on Chip**
- **Provides Support for Module Live Insertion**
- **Handles Both Packet and Compelled Transfers**
- **Capable of Buffering up to 256 Bytes Per Transaction**

description

The TFB2022AI data path unit (DPU) is a member of the Texas Instruments Futurebus+ (FB+) chip set. This chip set provides an integrated approach to the Futurebus+ interface that reduces new-product design time, allows more functionality per circuit board, improves overall interface reliability, and reduces end-user down time through built-in test capabilities. The Futurebus+ chip set is capable of supporting 32- or 64-bit data widths in any combination on both the host-bus interface (HIF) and Futurebus+. The address width is programmable to be 32 bits or 36 bits (with either data width).

The TFB2022AI may be used with a TFB2002B Futurebus+ I/O controller to provide a complete 64-bit Profile-B interface. It allows great flexibility in the design of the system and in the host features that may be supported. It may also be used with a user-defined controller to provide a variety of performance features. When used together, the TFB2022AI and TFB2002B provide the Futurebus+ and host-bus protocol control for the first 64 bits of data and 36 bits of address. The TFB2022AI contains a bidirectional FIFO for high-speed transmission of data in either compelled or packet mode, address control for 36 bits of address, and related CSR locations. All Profile-A- and Profile-B-required CSRs are implemented either on this device or the TFB2002B.

The TFB2022AI is optimized for Profile-B modules. Several processors may reside on a single module with the DPU as long as they do not require the DPU/IOC to understand cache-coherent operation. The module may contain memory or I/O units in addition to processors. The TFB2022AI is best suited for I/O or memory modules.

The MS<1:0> signals provide a preaddress decode mechanism, enabling the user to implement simplified decode logic in the logic interface. These signals indicate whether an access is being made to host memory, extended units space, host CSR space, or to a message mailbox.

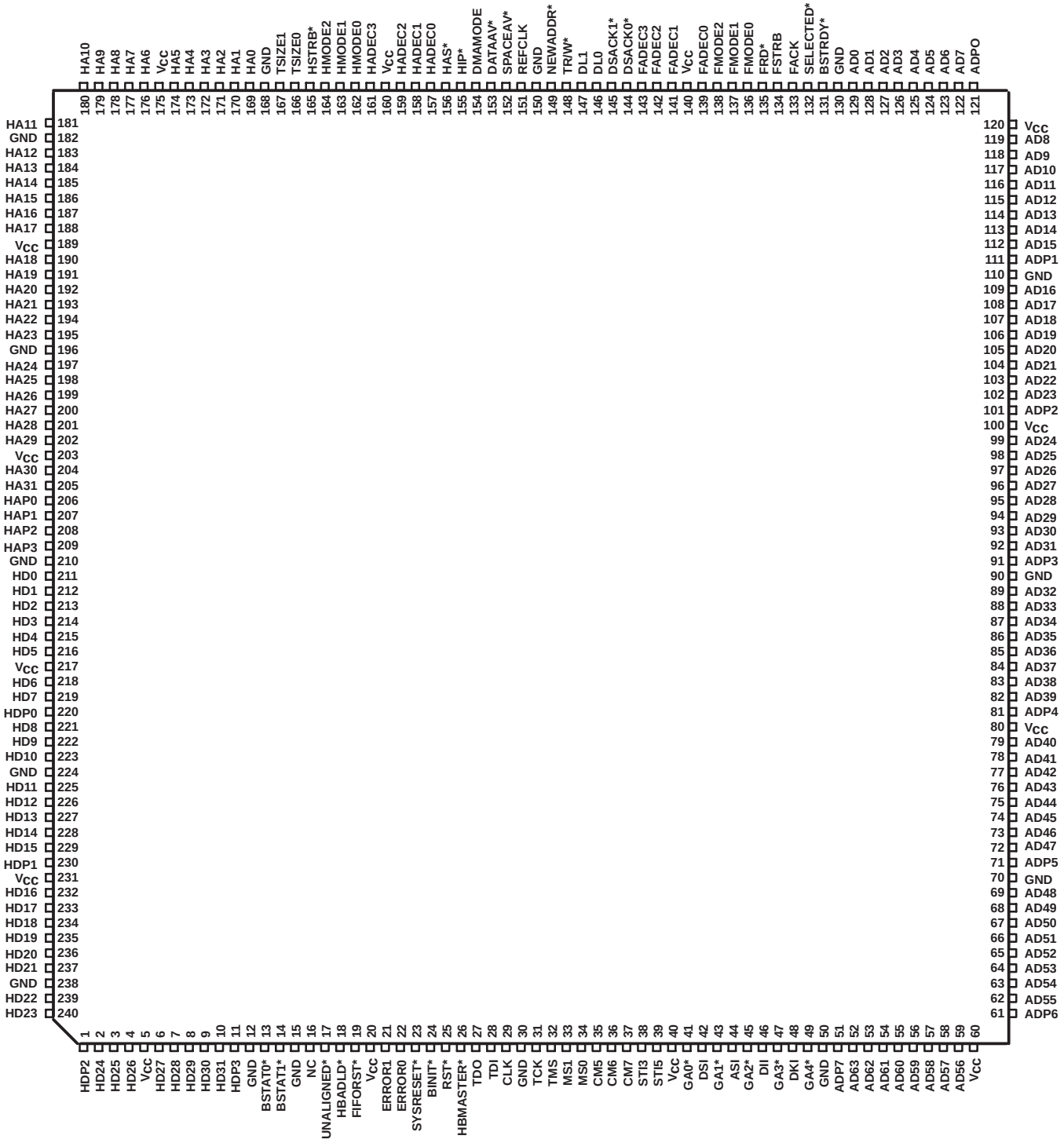
The TFB2022AI is offered in a 240-pin metal quad flat package (MFP). The TFB2022AI is characterized for operation over the industrial temperature range of −20°C to 85°C.

NOTE: To maintain consistency with the notation used in the Futurebus+ standard (IEEE Std 896.1−1991), an active-low signal is denoted herein by use of the trailing asterisk (*) on the signal name.

SPARC is a trademark of Sun Microsystems, Inc.
Alpha AXP is a trademark of Digital Equipment Corporation.

terminal assignments

MFP PACKAGE
(TOP VIEW)



NC − No internal connection

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Terminal Functions

host interface

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
BSTAT<1:0>*	14, 13	I	Host interface	Host-interface status: HH Normal HL Reserved LH Bus error LL Backoff/retry
BSTRDY*	131	I	Host interface	Burst ready
CLK	29	I	Host interface	Clock input. CLK is the processor clock for synchronous transactions on the host side. Up to 25 MHz is recommended.
DL<1:0>	147, 146	I	Host interface	Host-interface data length: LL 64 bytes LH 32 bytes HL 16 bytes HH 8 bytes
DSACK<1:0>*	145, 144	I	Host interface	Data acknowledge: Single mode (TBST* = high): LL Complete cycle, data bus port 32 LH Reserved HL Reserved HH Insert wait state Burst mode (TBST* = low): LL Low speed, 32-bit burst capable LH High speed, 32-bit burst capable HL Low speed, 64-bit burst capable HH High speed, 64-bit burst capable
HA<31:0>	205−204, 202−197, 195−190, 188−183, 181−176, 174−169	I/O	Host interface	Host-interface address or upper quadlet of data
HAP<3:0>	209−206	I/O	Host interface	Extended host-interface address or parity for upper quadlet of host interface data
HAS*	156	I	Host interface	Host-interface address strobe
HD<31:0>	10−6, 4−2, 240−239, 237−232, 229−225, 223−221, 219−218, 216−211	I/O	Host interface	Lower quadlet of host-interface data
HDP<3:0>	11, 1, 230, 220	I/O	Host interface	Parity for lower quadlet of host-interface data
HIP*	155	I	Host interface	Host-interface transaction in progress
TR/W*	148	I	Host interface	Host-interface read or write
TSIZE<1:0>	167, 166	I/O	Host interface	Host-interface transaction size: LL Word (32 bits or greater) LH Byte (8 bits) HL Half word (16 bits) HH Three bytes (24 bits)

Terminal Functions

other module interface signals

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
MS<1:0>	33, 34	O	Module	Memory decode of the host address: LL Unselected LH Host memory HL Host-unit space HH CSR space
REFCLK	151	I	Module	Clock input. A 25-MHz, 50%±5% duty-cycle signal is recommended; any frequency between 25 MHz and 33 MHz and duty cycle of 50%±5% can be tolerated. REFCLK determines packet-mode transfer speed.

interface to TFB2002A

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
DATAAV*	153	O	TFB2002B IOC	Data available in FIFO. In compelled mode, DATAAV* indicates if any data is in the FIFO. In packet or burst mode, DATAAV* indicates if a packet or burst data of length encoded on Futurebus+ packet size or the DL<1:0> lines is available.
DMAMODE	154	I	TFB2002B IOC	DMA operation is occurring. FMODE and HMODE are modified for this function.
ERROR<1:0>	21, 22	O	TFB2002B IOC	Futurebus+ error indicators: LL No error LH Futurebus+ parity error HL Packet longitudinal error HH Host-interface-data parity error
FADEC<3:0>	143, 142, 141, 139	O	TFB2002B IOC	Futurebus+ address decode: LLLL Unselected LLLH Host memory LLHL Host-extended-unit space LLHH Host CSR LHLL Broadcast mailbox LHLH Reserved LHHL Reserved LHHH Reserved HLLL Mailbox address HLLH Packet-mode-capable memory address HLHL Reserved HLHH Reserved HHLL Reserved HHLH DPU CSR HHHL Broadcast CSR (non-DPU) HHHH Broadcast CSR (DPU)
FIFORST*	19	I	TFB2002B IOC	FIFO reset. FIFORST* resets the FIFO pointers
FACK	133	O	TFB2002B IOC	Futurebus+ acknowledge. Futurebus+ event complete
FMODE<2:0>	138, 137, 136	I	TFB2002B IOC	Futurebus+ mode. FMODE<2:0> indicates to the TFB2022AI what action is to be taken in the Futurebus+ interface: LLL Compelled-mode Futurebus+ LLH Packet-mode Futurebus+ LHL Partial transfer LHH Disconnect data for master write HLL Reserved HLH Reserved HHL Disconnect data for split requestor HHH Reserved

Terminal Functions

interface to TFB2002A (continued)

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
FRD*	135	I	TFB2002B IOC	Futurebus+ read/write indicator: L = read (move data from Futurebus+ to FIFO); H = write (move data from FIFO to Futurebus+)
FSTRB	134	I	TFB2002B IOC	Futurebus+ strobe: perform next Futurebus+ event
HADEC<3:0>	161, 159, 158, 157	O	TFB2002B IOC	Host address decode. Address decoding for the host-interface address: Slave encoding: / Master encoding: LLLL Unselected / LLLL Unselected LLLH Host memory / LLLH Memory address compelled LLHL Host-unit space / LLHL Maximum burst capable or extended unit space LLHH Host CSR / LLHH Memory address 64-byte burst LHLL Broadcast mailbox / LHLL 32-byte-memory-address capable LHLH Reserved / LHLH 16-byte-memory-address capable LHHL Split response hit / LHHL 8-byte-memory-address capable LHHH Futurebus+ CSR address / LHHH Reserved HLLL Reserved / HLLL Reserved HLLH Broadcast CSR address / HLLH Reserved HLHL Reserved / HLHL Reserved HLHH Reserved / HLHH Reserved HHLL Reserved / HHLL Reserved HHLH DPU CSR / HHLH Reserved HHHL Reserved / HHHL Reserved HHHH Reserved / HHHH Reserved
HBADLD*	18	I	TFB2002B IOC	Host address load. Futurebus+ has been granted for the requested transaction
HBMASTER*	26	I	TFB2002B IOC	Host master. Indicates host-interface mastership
HMODE<2:0>	164, 163, 162	I	TFB2002B IOC	Host mode. HMODE<2:0> indicates to the TFB2022AI what action is to be taken in the host interface: LLL Reserved LLH Between FIFO and host interface (single transfer), between TFB2022AI resident CSR and host interface, or between TFB2022AI resident CSR and FIFO LHL From FIFO to TFB2022AI resident CSR LHH Reserved HLL Reserved HLH Between FIFO and host bus (burst mode) HHL Reserved HHH Reserved
HSTRB*	165	I	TFB2002B IOC	Host strobe. Perform next host-interface request as indicated in HMODE<2:0>
NEWADDR*	149	I	TFB2002B IOC	New address. Increment address in the TFB2022AI address register
SELECTED*	132	I	TFB2002B IOC	Module selected. Futurebus+ transaction uses this module. The DPU is used as a slave of the Futurebus+ transaction.
SPACEAV*	152	O	TFB2002B IOC	Space available in FIFO. In compelled mode, SPACEAV* indicates that space is available in the FIFO for another transfer. In packet or burst mode, SPACEAV* indicates that space is available in the FIFO for another packet or burst.
UNALIGNED*	17	O	TFB2002 IOC	FB+ slaved partial unaligned operation

Terminal Functions

JTAG test port

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
TCK	31	I	Module	JTAG test clock
TDI	28	I	Module	JTAG test data in
TDO	27	O	Module	JTAG test data out
TMS	32	I	Module	JTAG test-mode select

reset port

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
BINIT*	24	I	Module	Bus interface reset. Signal indicating that a bus-interface reset is required
RST*	25	I	Module	Module power-up reset. RST* resets all logic; output signals go to their inactive states, and 3-state outputs and bidirectional signals take on the high-impedance state.
SYSRESET*	23	I	Module	System reset required. Signal indicating that a system reset is required

Futurebus+ Interface

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
AD<63:0>	52−59, 62−69, 72−79, 82−89, 92−99, 102−109, 112−119, 122−129	I/O	Futurebus+	Multiplexed Futurebus+ address and data
ADP<7:0>	51, 61, 71, 81, 91, 101, 111, 121	I/O		Futurebus+ parity
ASI	44	I	Futurebus+	Futurebus+ address synchronization strobe
CM<7:5>	37, 36, 35	I	Futurebus+	Futurebus+ command bits
DSI, DKI, DII	42, 48, 46	I	Futurebus+	Futurebus+ data path synchronization signals in: data strobe (DSI), data acknowledge (DKI), data acknowledge inverse (DII)
GA<4:0>	49, 47, 45, 43, 41	I	Futurebus+	Geographical address
STI5, STI3	39, 38	I	Futurebus+	Futurebus+ status

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range, V_I (at any input) . . . . . −0.5 V to 7 V
Output voltage range, V_O . . . . . −0.5 V to 7 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Power dissipation . . . . . 2 W
Operating free-air temperature range, T_A . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
MFP	6250 mW	50 mW/°C	4000 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature range, T_A	−20		85	°C

electrical characteristics over recommend operating free-air temperature range (unless otherwise noted)

PARAMETER		MACRO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Input threshold voltage	IPI04LK	$V_I = V_{CC}$ or 0 V, $I_I = \pm 1$ µA, $C_L = 7.4$ pF		1.3		V
V_{OH}	High-level output voltage	OPI43LK	$I_{OH} = -4$ mA	3.7			V
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA			0.5	V
V_{OH}	High-level output voltage	OPI83LK	$I_{OH} = -8$ mA	3.7			V
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V
V_{OH}	High-level output voltage	OPIH3LK	$I_{OH} = -12$ mA	3.7			V
V_{OL}	Low-level output voltage		$I_{OL} = 12$ mA			0.5	V
V_{OH}	High-level output voltage	OPJ43LK	$I_{OH} = -4$ mA	3.7			V
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA			0.5	V
V_{OH}	High-level output voltage	OPJ83LK	$I_{OH} = -8$ mA	3.7			V
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA			0.5	V

macros

Table 1 lists the internal and external buffer macros used in the TFB2022AI design. To use this table, find the pin of interest and note the macro name(s). If there is an entry only in the input macro column, the pin is an input. If there is an entry only in the output macro column, the pin is an output. If there is an entry in both columns, this is a 3-state bidirectional pin. The macro(s) are also listed in the electrical characteristics table.

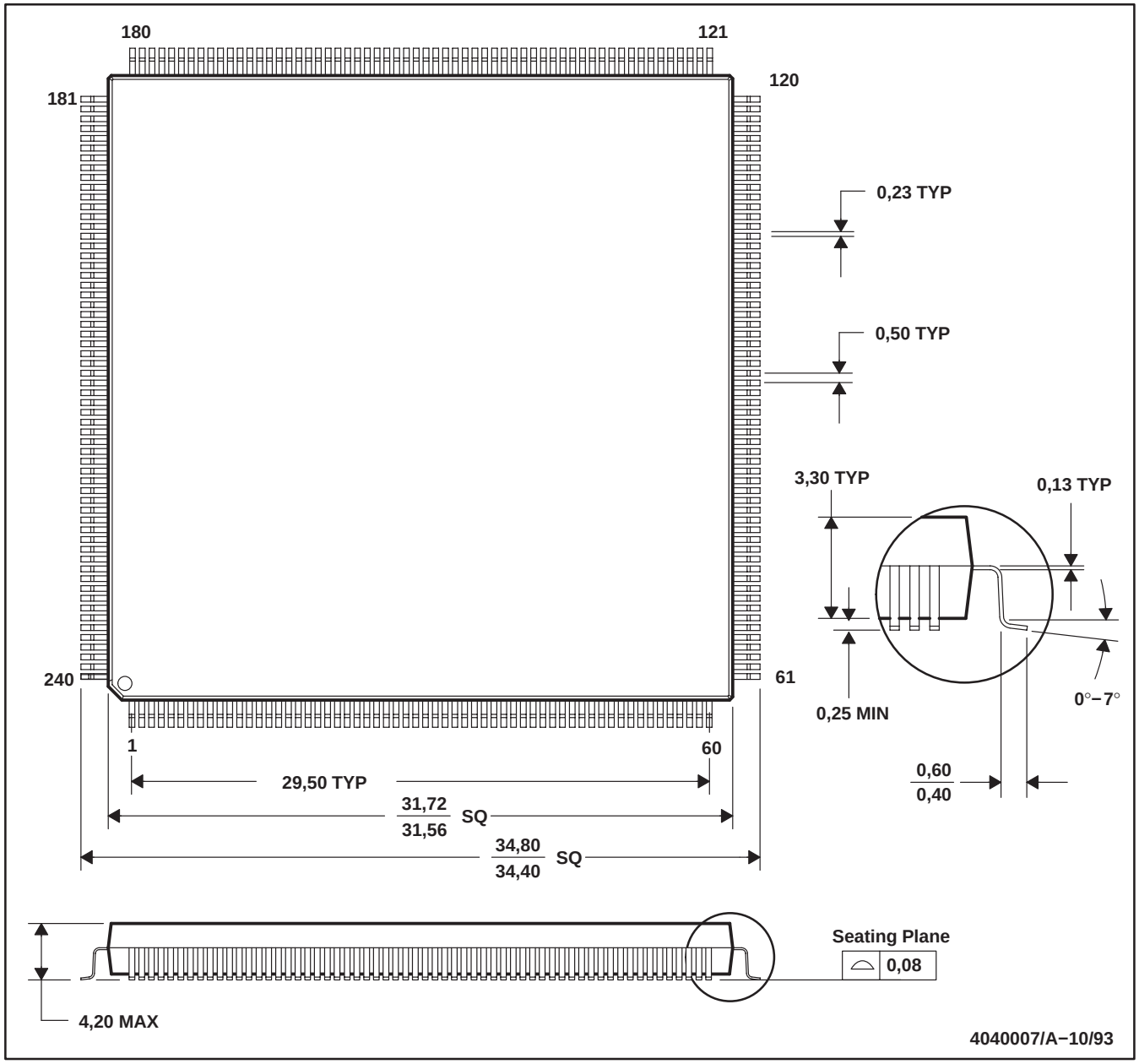
Table 1. TFB2022AI (DPU) Pin Names and Macro Numbers

PIN NAME	INPUT MACRO	OUTPUT MACRO
AD<63:0>	IPI04LK	OPJ43LK
ADP<7:0>	IPI04LK	OPJ43LK
ASI	IPI04LK	
BINIT*	IPI04LK	
BSTAT<1:0>*	IPI04LK	
BSTRDY*	IPI04LK	
CLK	IPI04LK	
CM<7:5>	IPI04LK	
DATAAV*		OPI43LK
DII	IPI04LK	
DKI	IPI04LK	
DL<1:0>	IPI04LK	
DMAMODE	IPI04LK	
DSACK<1:0>*	IPI04LK	
DSI	IPI04LK	
ERROR<1:0>		OPI43LK
FACK		OPI43LK
FADEC<3:0>		OPI43LK
FIFORST*	IPI04LK	
FMODE<2:0>	IPI04LK	
FRD*	IPI04LK	
FSTRB	IPI04LK	
GA<4:0>*	IPI04LK	
HA<31:0>	IPI04LK	OPJ83LK
HADEC<3:0>		OPI43LK

PIN NAME	INPUT MACRO	OUTPUT MACRO
HAP<3:0>	IPI04LK	OPJ83LK
HAS*	IPI04LK	
HBADLD*	IPI04LK	
HBMASTER*	IPI04LK	
HD<31:0>	IPI04LK	OPJ83LK
HDP<3:0>	IPI04LK	OPJ83LK
HIP*	IPI04LK	
HMODE<2:0>	IPI04LK	
HSTRB*	IPI04LK	
MS<1:0>		OPI83LK
NEWADDR*	IPI04LK	
REFCLK	IPI04LK	
RST*	IPI04LK	
SELECTED*	IPI04LK	
SPACEAV*		OPI43LK
STI<5,3>	IPI04LK	
SYSRESET*	IPIO4LK	
TCK	IPI04LK	
TDI	IPI04LK	
TDO		OPI43LK
TMS	IPI04LK	
TR/W*	IPI04LK	
TSIZE<1:0>	IPI04LK	OPIH3LK
UNALIGNED*		OPI43LK

MECHANICAL DATA

MFP/S-MQFP-G240 **METAL QUAD (MQUAD®) CAVITY-UP FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MQUAD is a registered trademark of Olin Corporation.
D. This quad flat package consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic. Ultrasonic cleaning of this package or boards with this package is not permitted.

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