- **Industrial Temperature Version of the TFB2002B With an Operating Range of –20°C to 85°C**
- **Provides Control Logic Necessary to Operate a Data Path Unit (TFB2022A) on Futurebus+**
- **Parallel-Protocol Support Is Fully Compliant to Futurebus+ Standard (IEEE Std 896.1–1991)**
- **Interfaces Easily to a Variety of Popular Microprocessors Such as SPARC™, R4000, 680x0, 88xxx, 80x86, and Alpha AXP™**
- **Provides Full Support for Futurebus+ Cache Commands (for Memory or I/O Modules in Shared-Memory Systems)**
- **Capable of Handling a Single Outstanding Split Transaction**
- **Parallel-Protocol-Related CSR Locations Are Provided on Chip**
- **Offers Autonomous Control for Futurebus+ and Host-Module Reads and Writes**

description

The TFB2002BI I/O controller (IOC) is a member of the Texas Instruments Futurebus+ (FB+) chip set. This chip set provides a highly integrated approach to the Futurebus+ interface that reduces new-product design time, allows more functionality per circuit board, improves overall interface reliability, and reduces end-user down time through built-in test capabilities. The Futurebus+ chip set is capable of supporting 32- or 64-bit data widths in any combination on both the host-bus interface (HIF) and Futurebus+. The address width is programmable to be 32 bits or 36 bits (with either data width).

The TFB2002BI contains the control logic necessary to translate Futurebus+ transactions into host bus transactions and vice versa. It contains a high-speed Futurebus+ handshake controller, a synchronous host bus controller, and reset-type determination logic.

When combined with a TFB2022A Futurebus+ data path unit (DPU), the TFB2002BI provides a complete 64-bit-wide interface to the Futurebus+. The TFB2002BI provides the necessary control logic for the data path unit to provide a complete interface to the Futurebus+ for a Profile-B-compliant module. It may also be used on I/O or memory modules in a cache-coherent system.

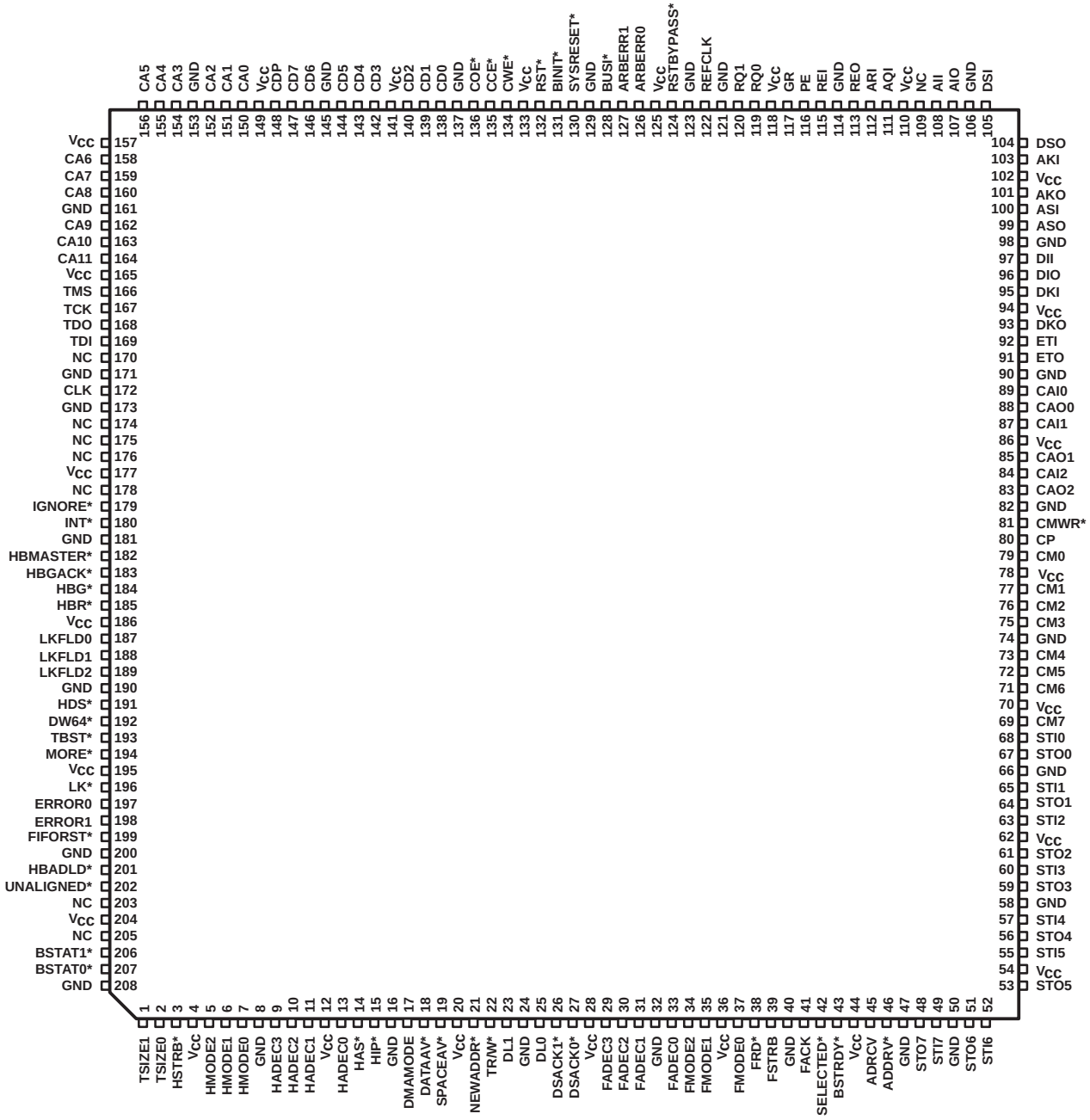
The TFB2002BI is offered in a 208-pin plastic quad flat package (PPM). The TFB2002BI is characterized for operation over the industrial temperature range of –20°C to 85°C.

NOTE: To maintain consistency with the notation used in the Futurebus+ standard (IEEE Std 896. 1–1991), an active-low signal is denoted herein by use of the trailing asterisk (*) on the signal name.

SPARC is a trademark of Sun Microsystems, Inc.
Alpha AXP is a trademark of Digital Equipment Corporation.

terminal assignments

PPM PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

host interface

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
BSTAT<1:0>*	206 207	I/O	Host interface	Host-interface status: HH Normal HL Reserved LH Bus error LL Backoff/retry
BSTRDY*	43	I/O	Host interface	Burst ready
CLK	172	I	Host interface	Clock input. CLK is the processor clock for synchronous transactions on the host side. Up to 25 MHz is recommended.
DL<1:0>	23, 25	I/O	Host interface	Host-interface data length: LL 64 bytes LH 32 bytes HL 16 bytes HH 8 bytes
DSACK<1:0>*	26 27	I/O	Host interface	Data acknowledge: Single mode (TBST* = high): Burst mode (TBST* = low): LL Complete cycle, data bus port 32 — LL Low speed, 32-bit burst capable LH Reserved — LH High speed, 32-bit burst capable HL Reserved — HL Low speed, 64-bit burst capable HH Insert wait state — HH High speed, 64-bit burst capable
DW64*	192	I/O	Host interface	Host-interface data width of 64 (burst mode only)
HAS*	14	I/O	Host interface	Host-interface address strobe
HBG*	184	I	Host interface	Host-interface grant input
HBGACK*	183	I/O (open collector)	Host interface	Host-interface grant acknowledge
HBR*	185	O (open collector)	Host interface	Host-interface request output
HDS*	191	I/O	Host interface	Host-interface data strobe
HIP*	15	I/O	Host interface	Host-interface transaction in progress
IGNORE*	179	I	Host interface	Ignore the current host transaction input. IGNORE* is supplied by the host-memory decoder when an access to private memory occurs. IGNORE* is optional and should be tied high if it is not used.
INT*	180	O (open collector)	Host interface	Host interrupt output. When an enabled interrupt condition occurs, INT* is driven low. Interrupts are cleared by writing a one to the appropriate bit in the interrupt register. The interrupt goes high during the write cycle to the interrupt register even if another interrupt is pending. Also used from FB+ CM<2:0> lines to a mastered HIF locked operation. These terminals are used as inputs when the IOC is a host-interface slave/FB+ master.
LK*	196	I/O	Host interface	Host cycle is locked (indivisible)
LKFLD0, LKFLD1, LKFLD2	187 188 189	I/O	Host interface	Locked-command bits passed from the host interface to FB+ or from FB+ to the host interface via the CM<2:0> lines during a mastered FB+ data phase in a locked operation. Also used from FB+ CM<2:0> lines to a mastered HIF locked operation. These terminals are used as inputs when the IOC is a host interface slave/FB+ master.

Terminal Functions

host interface (continued)

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
MORE*	194	I	Host interface	Host cycle is part of a longer transaction input. MORE* is used in DMA writes to indicate that this transaction should be included in the same tenure with the next host-interface transaction. MORE* is used in reads to indicate that MR* should be asserted during the Futurebus+ transaction.
TBST*	193	I/O	Host interface	Host-transaction burst request
TR/W*	22	I/O	Host interface	Host-interface read or write
TSIZE<1:0>	1, 2	I	Host interface	Host-interface transaction size input: LL Word (32 bits or greater) LH Byte (8 bits) HL Half word (16 bits) HH Three bytes (24 bits)

other module interface signals

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
ARBERR<1:0>	127, 126	I	Arbiter	Arbitration error input: LL No error LH ACO and AC1 asserted during phase 3 HL Arbitration comparison error HH Arbitration time-out error (phase 2 or 4)
REFCLK	122	I	Module	Clock input. A 25-MHz, 50% ± 5% duty-cycle signal is recommended; any frequency between 20 MHz and 40 MHz and duty cycle of 50% ± 5% can be tolerated.

CSR bus

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
CA<11:0>	164, 163, 162, 160, 159, 158, 156, 155, 154, 152, 151, 150	I	CSR bus	CSR bus address
CD<7:0>	147, 146, 144, 143, 142, 140, 139, 138	I/O	CSR bus	CSR bus data
CDP	148	I/O	CSR bus	CSR bus data odd parity
CCE*	135	I	CSR bus	CSR bus chip enable
COE*	136	I	CSR bus	CSR bus output enable
CWE*	134	I	CSR bus	CSR bus write enable

Terminal Functions

interface to TFB2022A

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
DATAAV*	18	I	TFB2022A DPU	Data available in FIFO. In compelled mode, DATAAV* indicates if any data is in the FIFO. In packet or burst mode, DATAAV* indicates if a packet or burst data of length encoded on the Futurebus packet size or the DL<1:0> lines is available.
DMAMODE	17	O	TFB2022A DPU	DMA operation is occurring. DMAMODE turns off critical word first on the TFB2022A.
ERROR<1:0>	198, 197	I	TFB2022A DPU	Futurebus+ error indicators: LL No error LH Futurebus+ parity error HL Packet longitudinal parity error HH Host-bus parity error
FADEC<3:0>	29, 30 31, 33	I	TFB2022A DPU	Futurebus+ address decode: LLLL Unselected LLLH Host memory LLHL Host extended-unit space LLHH Host CSR LHLL Broadcast mailbox LHLH Reserved LHHL Reserved LHHH Reserved HLLL Mailbox address HLLH Packet-mode-capable memory address HLHL Reserved HLHH Reserved HHLL Reserved HHLH DPU CSR HHHL Broadcast CSR (non-DPU) HHHH Broadcast CSR (DPU)
FIFORST*	199	O	TFB2022A DPU	FIFO reset. FIFORST* resets the FIFO pointers.
FACK	41	I	TFB2022A DPU	Futurebus+ acknowledge. FACK indicates Futurebus+ event is complete
FMODE<2:0>	34, 35, 37	O	TFB2022A DPU	Futurebus+ mode. FMODE<2:0> indicates to the TFB2022A what action is to be taken in the Futurebus+ interface: LLL Compelled-mode Futurebus+ LLH Packet-mode Futurebus+ LHL Partial transfer LHH Disconnect data for master write HLL Reserved HLH Reserved HHL Disconnect data for split requestor HHH Reserved
FRD*	38	O	TFB2022A DPU	Futurebus+ read/write indicator: L = read from Futurebus+ to FIFO; H = write from FIFO to Futurebus+
FSTRB	39	O	TFB2022A DPU	Futurebus+ strobe. FSTRB performs next Futurebus+ event

Terminal Functions

interface to TFB2022A (continued)

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
HADEC<3:0>	9, 10, 11, 13	I	TFB2022A DPU	Host address decode. Address decoding for the host-interface address: Slave encoding: / Master encoding: LLLL Unselected / LLLL Unselected LLLH Host memory / LLLH Memory address compelled LLHL Host extended-unit space / LLHL Maximum capable burst or extended unit space LLHH Host CSR / LLHH Memory address 64-byte burst LHLL Broadcast mailbox / LHLL 32-byte-memory-address capable LHLH Reserved / LHLH 16-byte-memory-address capable LHHL Split response hit / LHHL 8-byte-memory-address capable LHHH Futurebus+ CSR address / LHHH Reserved HLLL Reserved / HLLL Reserved HLLH Broadcast CSR address / HLLH Reserved HLHL Reserved / HLHL Reserved HLHH Reserved / HLHH Reserved HHLL Reserved / HHLL Reserved HHLH DPU CSR / HHLH Reserved HHHL Reserved / HHHL Reserved HHHH Reserved / HHHH Reserved
HBADLD*	201	O	TFB2022A DPU	Host address load. Futurebus+ has been granted for the requested transaction output.
HBMASTER*	182	O	TFB2022A DPU	Host master. This device is mastering the host bus transaction.
HMODE<2:0>	5, 6, 7	O	TFB2022A DPU	Host mode. HMODE<2:0> indicates to the TFB2022A what action is to be taken in the host interface: LLL Reserved LLH Between FIFO and host interface (single transfer), between TFB2022A resident CSR and host interface, or between TFB2022A resident CSR and FIFO LHL From FIFO to TFB2022A resident CSR. LHH Reserved HLL Reserved HLH Between FIFO and host interface (burst mode) HHL Reserved HHH Reserved
HSTRB*	3	O	TFB2022A DPU	Host strobe. HSTRB* performs next host-interface request as indicated in HMODE<2:0>.
NEWADDR*	21	O	TFB2022A DPU	New address. NEWADDR* increments address in the TFB2022A address register.
SELECTED*	42	O	TFB2022A DPU	Module selected. Futurebus+ transaction uses this module. The DPU is used as a slave of the Futurebus+ transaction
SPACEAV*	19	I	TFB2022A DPU	Space available in FIFO. In compelled mode, SPACEAV* indicates that space is available in the FIFO for another transfer. In packet or burst mode, SPACEAV* indicates that space is available in the FIFO for another packet or burst
UNALIGNED*	202	I	TFB2022A DPU	FB+ slave partial unaligned operation

Terminal Functions

JTAG test port

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
TCK	167	I	Module	JTAG test clock
TDI	169	I	Module	JTAG test data in
TDO	168	O	Module	JTAG test data out
TMS	166	I	Module	JTAG test-mode select

reset port

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
AQI	111	I		Arbitration handshake. AQI is used to determine if the arbitration bus has been idle for 1 μs. If the arbitration bus is not implemented, this signal should be tied low.
ARI	112	I		Arbitration handshake. ARI is used to determine if the arbitration bus has been idle for 1 μs. If the arbitration bus is not implemented, this signal should be tied high.
BINIT*	131	O	Module	Bus interface reset. BINIT* is an open-collector signal indicating that a bus interface reset is required.
BUSI*	128	O		Bus idle. Bus has been idle for longer than 1 μs, and REO is asserted.
REI	115	I		Futurebus+ reset in
REO	113	O		Futurebus+ reset out
RST*	132	I	Module	Module power-up reset. RST* resets all logic; output signals go to their inactive states, state outputs and bidirectional signals take on the high-impedance state.
SYSRESET*	130	O	Module	System reset required. SYSRESET* is an open-collector signal indicating that a system reset is required.
RSTBYPASS*	124	I	Module	Reset bypass. Bypass auto alignment after power up.

Terminal Functions

Futurebus+ interface

TERMINAL NAME	TERMINAL NO.	I/O	FROM/TO	DESCRIPTION
ADRCV	45	O	Futurebus+	Transceiver receiver enable
ADDRV*	46	O	Futurebus+	Transceiver driver enable
ASI, AKI, AII	100, 103, 108	I	Futurebus+	Futurebus+ address synchronization signals: address strobe (ASI), address acknowledge (AKI), address acknowledge inverse (AII)
ASO, AKO, AIO	99, 101, 107	O	Futurebus+	Futurebus+ address synchronization signals: address strobe (ASO), address acknowledge (AKO), address acknowledge inverse (AIO)
CAI<2:0>	84, 87, 89	I	Futurebus+	Futurebus+ capability bits
CAO<2:0>	83, 85, 88	O	Futurebus+	Futurebus+ capability bits
CM<7:0>, CP	69, 71, 72, 73, 75, 76, 77, 79, 80	I/O	Futurebus+	Futurebus+ command bits and parity
CMWR*	81	O	Futurebus+	Transceiver control for command: H = read, L = write
DSI, DKI, DII	105, 95, 97	I	Futurebus+	Futurebus+ data-path-synchronization input signals: data strobe (DSI), data acknowledge (DKI), data acknowledge inverse (DII)
DSO, DKO, DIO	104, 93, 96	O	Futurebus+	Futurebus+ data-path-synchronization output signals: data strobe (DSO), data acknowledge (DKO), data acknowledge inverse (DIO)
ETI	92	I	Futurebus+	Futurebus+ end-of-tenure in
ETO	91	O	Futurebus+	Futurebus+ end-of-tenure out
GR	117	I	Futurebus+	Futurebus+ mastership has been granted (bus tenure may begin when ETI is released).
PE	116	I	Futurebus+	Futurebus+ preemption has occurred.
RQ<1:0>	120, 119	O	Futurebus+	Futurebus+ is requested at level 1 or level 0. RQO is used for DMA operations; RQ1 is used for all other operations.
STI<7:0>	49, 52, 55, 57, 60, 63, 65, 68	I	Futurebus+	Futurebus+ status in
STO<7:0>	48, 51, 53, 56, 59, 61, 64, 67	O	Futurebus+	Futurebus+ status out

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I (at any input) . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Power dissipation . . . . . 500 mW
Operating free-air temperature range, T_A . . . . . –20°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PPM	3175 mW	25.4 mW/°C	2032 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	–0.5		0.8	V
Operating free-air temperature range, T_A	–20		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MACRO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Input threshold voltage	IPI04LK	V_I = V_{CC} or 0 V, I_I = ±1 µA, C_L = 7.4 pF		1.3		V
V_{IT+}	Positive-going input threshold voltage	IPI09LK			1.6		V
V_{IT-}	Negative-going input threshold voltage				1.2		V
V_{OL}	Low-level output voltage (open drain)	OPI82LK	I_{OL} = 8 mA			0.5	V
V_{OH}	High-level output voltage	OPI43LK	I_{OH} = –4 mA	3.7			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
V_{OH}	High-level output voltage	OPI83LK	I_{OH} = –8 mA	3.7			V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.5	V
V_{OH}	High-level output voltage	OPIH3LK	I_{OH} = –12 mA	3.7			V
V_{OL}	Low-level output voltage		I_{OL} = 12 mA			0.5	V
V_{OH}	High-level output voltage	OPJ83LK	I_{OH} = –8 mA	3.7			V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.5	V

macros

Table 1 lists the internal and external buffer macros used in the TFB2002BI design. To use this table, find the pin of interest and note the macro name(s). If there is an entry only in the input macro column, the pin is an input. If there is an entry only in the output macro column, the pin is an output. If there is an entry in both columns, this is a 3-state bidirectional pin. The macro(s) are also listed in the electrical characteristics table.

Table 1. TFB2002BI (IOC) Pin Names and Macro Numbers

PIN NAME	INPUT MACRO	OUTPUT MACRO
ADDRV*		OPIH3LK
ADRCV		OPIH3LK
AII	IPI04LK	
AIO		OPI43LK
AKI	IPI04LK	
AKO		OPI43LK
AQI	IPI04LK	
ARBERR<1:0>	IPI04LK	
ARI	IPI04LK	
ASI	IPI04LK	
ASO		OPI43LK
BINIT*		OPI43LK
BSTAT<1:0>*	IPI04LK	OPIH3LK
BSTRDY*	IPI04LK	OPIH3LK

PIN NAME	INPUT MACRO	OUTPUT MACRO
BUSI*		OPI43LK
CA<11:0>	IPI04LK	
CAI<2:0>	IPI04LK	
CAO<2:0>		OPI43LK
CCE*	IPI04LK	
CD<7:0>	IPI04LK	OPJ83LK
CDP	IPI04LK	OPJ83LK
CLK	IPI04LK	
CM<7:0>	IPI04LK	OPI43LK
CMWR*		OPI43LK
COE*	IPI04LK	
CP	IPI04LK	OPI43LK
CWE*	IPI04LK	
DATAAV*	IPI04LK	

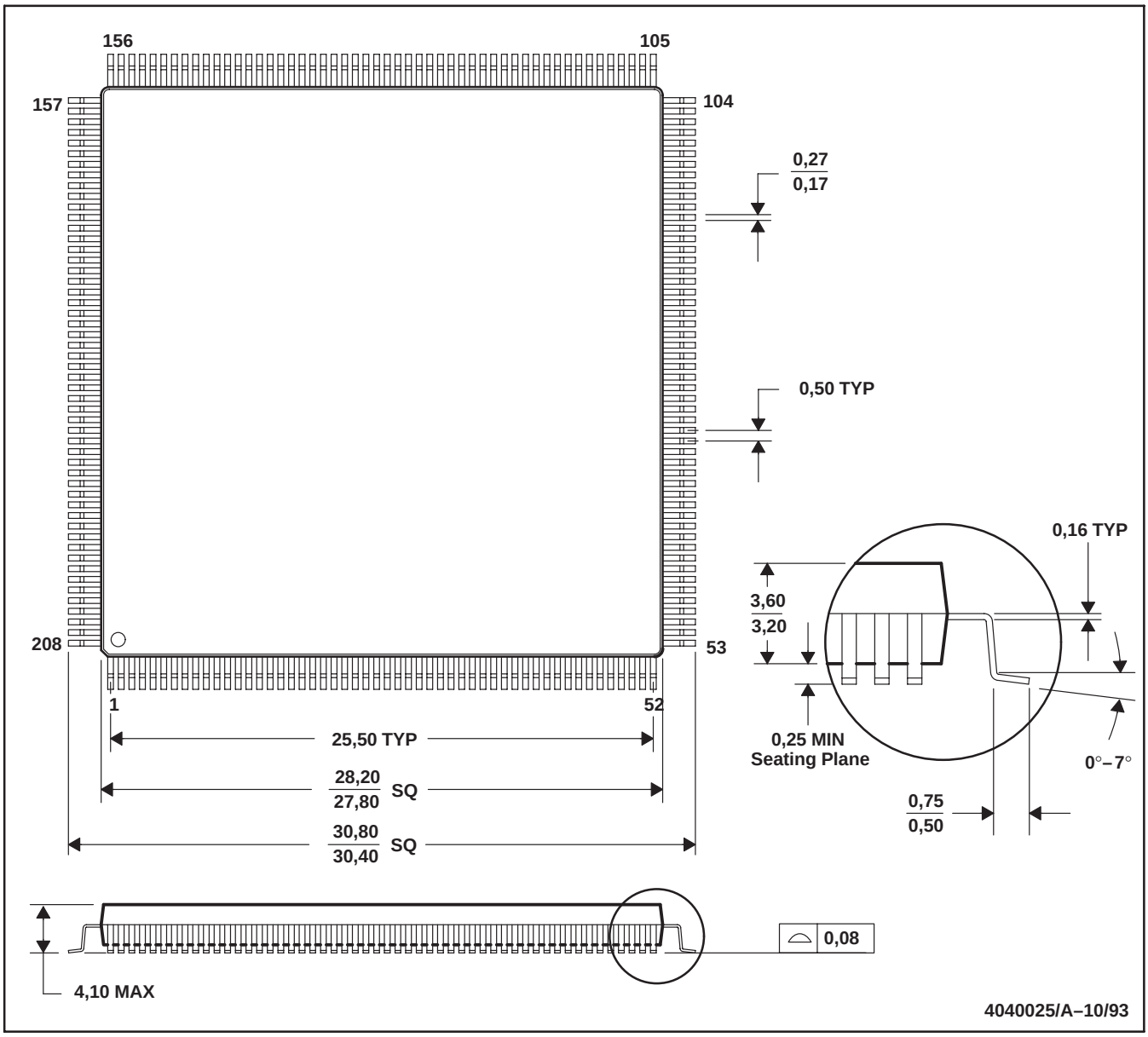
Table 1. TFB2002BI (IOC) Pin Names and Macro Numbers (Continued)

PIN NAME	INPUT MACRO	OUTPUT MACRO
DII	IPI04LK	
DIO		OPI43LK
DKI	IPI04LK	
DKO		OPI43LK
DL<1:0>	IPI04LK	OPIH3LK
DMAMODE		OPI43LK
DSACK<1:0>*	IPI04LK	OPIH3LK
DSI	IPI04LK	
DSO		OPI43LK
DW64*	IPI04LK	OPIH3LK
ERROR<1:0>	IPI04LK	
ETI	IPI04LK	
ETO		OPI43LK
FACK	IPI04LK	
FADEC<3:0>	IPI04LK	
FIFORST*		OPI43LK
FMODE<2:0>		OPI43LK
FRD*		OPI43LK
FSTRB		OPI43LK
GR	IPI04LK	
HADEC<3:0>	IPI04LK	
HAS*	IPI04LK	OPIH3LK
HBADLD*		OPI43LK
HBG*	IPI04LK	
HBGACK*	IPI04LK	OPIH3LK
HBMASTER*		OPI43LK
HBR*		OPI82LK
HDS*	IPI04LK	OPIH3LK
HIP*	IPI04LK	OPIH3LK

PIN NAME	INPUT MACRO	OUTPUT MACRO
HMODE<2:0>		OPI43LK
HSTRB*		OPI43LK
IGNORE*	IPI04LK	
INT*		OPI82LK
LK*	IPI04LK	OPIH3LK
LKFLD0, 1, 2	IPI04LK	OPI43LK
MORE*	IPI04LK	
NEWADDR*		OPI43LK
PE	IPI04LK	
REFCLK	IPI04LK	
REI	IPI04LK	
REO		OPI43LK
RQ<1:0>		OPI43LK
RST*	IPI09LK	
RSTBYPASS*	IPI04LK	
SELECTED*		OPI43LK
SPACEAV*	IPI04LK	
STI<7:0>	IPI04LK	
STO<7:0>		OPI43LK
SYSRESET*		OPI83LK
TBST*	IPI04LK	OPIH3LK
TCK	IPI04LK	
TDI	IPI04LK	
TDO		OPI43LK
TMS	IPI04LK	
TR/W*	IPI04LK	OPIH3LK
TSIZE<1:0>	IPI04LK	
UNALIGNED*	IPI04LK	

MECHANICAL DATA

PPM/S-PQFP-G208 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-143.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TFB2002BIPPM	OBSOLETE	QFP	PPM	208		TBD	Call TI	Call TI
TFB2002BMHFHB	OBSOLETE	CFP	HFH	256		TBD	Call TI	Call TI
TFB2002BPPM	OBSOLETE	QFP	PPM	208		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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