DATA SHEET

TEA0665
TEA0665T
Dolby B and C type noise reduction circuit

Product specification
File under Integrated Circuits, IC01

May 1992

Philips
Semiconductors

PHILIPS

GENERAL DESCRIPTION

The TEA0665 is designed for use in Dolby[1] B and Dolby C type audio Noise Reduction (NR) systems. The device provides the high and low level stages for one channel of a Dolby C-type NR system, including NR ON/OFF switching and all electronic switching necessary for Dolby C-type systems. In addition the TEA0665 includes a preamplifier for the record and playback functions and a multiplex buffer amplifier. The circuit offers two different line-output levels (–6 and 0 dBm) and a low-pass filter, which can be fed into the signal path in playback mode.

Features

- Few external components required
- Included RECORD/PLAY preamplifiers plus multiplex filter buffer amplifier
- Two different line-output levels
- All electronic switching

PACKAGE OUTLINES

TEA0665: 28-lead DIL; plastic (SOT117); SOT117-1; 1996 September 9.

TEA0665T: 28-lead mini-pack; plastic (SO28; SOT136A); SOT136-1; 1996 September 9.

(1) Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111 U.S.A., from whom licensing and application information must be obtained. Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

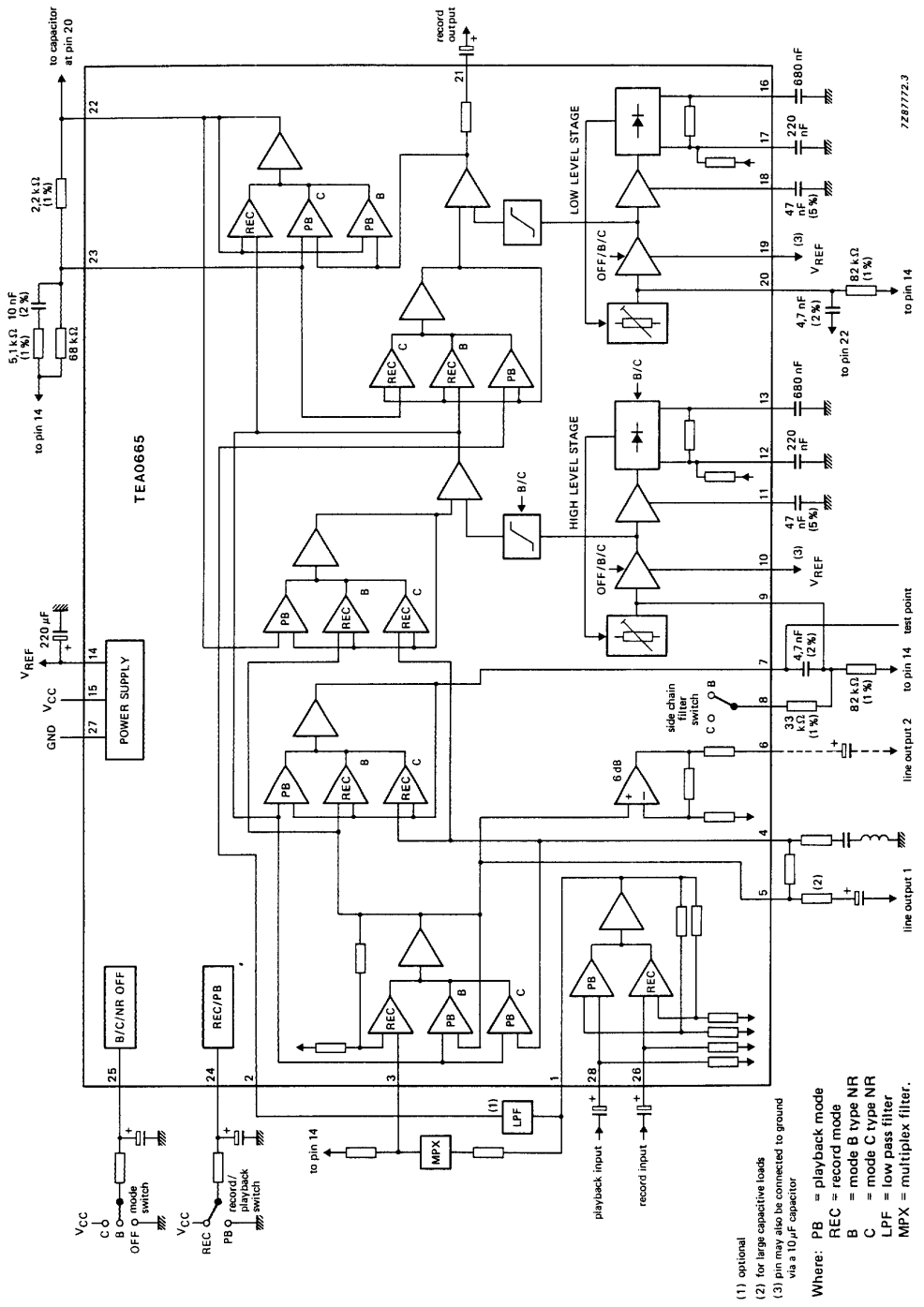


Fig.1 Block diagram and application circuit.

PINNING

1	PREAMP OUT	record/playback preamplifier output
2	PB BUFFER IN	play back amplifier input buffer
3	REC BUFFER IN	record amplifier input buffer
4	SSN	spectral skewing network
5	LINE OUT 1	line output 1
6	LINE OUT 2	line output 2
7	HLS SC IN	high level stage side chain input
8	SC SW	side chain filter switch
9	HLC SC	high level stage side chain
10	HLS AC GND	high level stage AC ground
11	HLS HP	high level stage high pass filter
12	HLS INT	high level stage integrating filter
13	HLS INT	high level stage integrating filter
14	V_{REF}	reference voltage
15	V_{CC}	positive supply voltage
16	LLS INT	low level stage integrating filter
17	LLS INT	low level stage integrating filter
18	LLS HP	low level stage high pass filter
19	LLS AC GND	low level stage AC ground
20	LLS SC	low level stage side chain
21	REC OUT	record output
22	AS	anti-saturation filter
23	AS	anti-saturation filter
24	REC/PB SW	record/playback switch input
25	MODE SW	mode switch input
26	REC IN	record input
27	GND	ground
28	PB IN	playback input

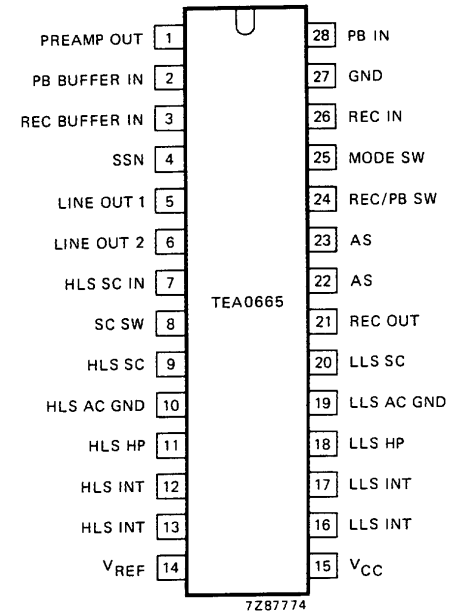


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	V_{CC}	max.	18	V
Input voltage (pins 26 and 28)	V_I	max.	–0,3 to V_{CC}	V
Total power dissipation	P_{tot}		600	mW
Storage temperature range	T_{stg}		–55 to + 150	°C
Operating ambient temperature range	T_{amb}		–40 to + 85	°C

CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 15 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = –6 dBm at test point pin 7; test circuit Fig.5; record mode; unless otherwise specified.

PARAMETER	CONDITIONS			SYMBOL	MIN.	TYP.	MAX.	UNIT
	MODE	F (KHZ)						
Supply								
Supply voltage range	C	–	note 1					
single				V_{CC}	8	14	16	V
(split)				V_{CC}	(±4)	(±7)	(±8)	V
Supply current	OFF	–	no input					
			signal	I_{CC}	–	17	25	mA
Input sensitivity	C		note 2					
of record amplifier			pin 26	V_i	43	50	57	mV
of playback amplifier			pin 28	V_i	25	30	35	mV
Signal handling	C	1	V_{CC} = 8 V					
of record output			THD = 1%		12	15	–	dB
(note 3; see Fig.8)		1	V_{CC} = 14 V					
			THD = 1%		–	20	–	dB
Line output 1			note 3		–0,5	0	+0,5	dB
Line output 2;								
amplifier gain V_o/V_i				G_v	+5,5	+6	+6,5	dB
(pin 6 to pin 5)								
Total harmonic								
distortion	OFF	1	TPL = 0 dB[6]	THD	–	0,02	0,1	%
			TPL = + 10 dB	THD	–	0,05	0,3	%
Total harmonic								
distortion	B	1	TPL = 0 dB	THD	–	0,1	0,15	%
			TPL = + 10 dB	THD	–	0,08	0,3	%
		10	TPL = 0 dB	THD	–	0,06	0,1	%
Total harmonic								
distortion	C	1	TPL 0 dB	THD	–	0,15	0,3	%
			TPL + 10 dB	THD	–	0,13	0,5	%
Signal plus noise-	C		R_S = 10 kΩ					
to-noise ratio			CCIR/ARM					
			weighted	(S+N)/N	62	66	–	dB

PARAMETER	CONDITIONS			SYMBOL	MIN.	TYP.	MAX.	UNIT
	MODE	F (KHZ)						
Frequency response	B	2	TPL = –25 dB		–19,0	–18,0	–17,0	dB
		5	TPL = –40 dB		–30,7	–29,7	–28,7	dB
		10	TPL = –30 dB		–24,5	–23,5	–22,5	dB
	C	0,2	TPL = –40 dB		–33,4	–31,9	–30,4	dB
		1	TPL = –30 dB		–20,1	–18,6	–17,1	dB
		1	TPL = –20 dB		–16,1	–14,1	–12,1	dB
		5	TPL = –0 dB		–3,8	–2,3	–0,8	dB
		5	TPL = –20 dB		–19,1	–17,1	–15,1	dB
		5	TPL = –40 dB		–28,5	–26,5	–24,5	dB
Switching thresholds			note 4; pin 24					
for record				V_{24-27}	8,5	–	14	V
for playback				V_{24-27}	0	–	4	V
Switching thresholds			note 5; pin 25					
	OFF			V_{25-27}	0	–	3,5	V
(switch in open position)	B			V_{25-27}	–	7	–	V
(external voltage)	B			V_{25-27}	6,3	7	7,7	V
	C			V_{25-27}	10,8	–	14	V
Switch input current			pin 25					
	OFF		V_{25-27} = 0 V	$-I_{25}$	–	–	40	μA
	C		$V_{25-27} = V_{CC}$	I_{25}	–	–	40	μA
Frequency response shift as a function of temperature deviation, range –40 to +85 °C, measured as deviation from 25 °C	C			Δf	–	± 0,5	–	dB
as a function of voltage deviation, rang 8 to 16 V, measured as deviation from 14 V				Δf	–	± 0,1		dB
Input resistance								
			pin 26	R_{26-27}	35	50	65	kΩ
			pin 28	R_{28-27}	35	50	65	kΩ
Output resistance								
			pin 6	R_{6-27}	–	160	220	Ω
			pin 21	R_{21-27}	–	60	100	Ω

Notes to the characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 7 V.
2. Attenuation between pins 1 and 3 is 3,5 dB (MPX-filter).
   Playback input sensitivity is 45 mV if a switchable MPX-low pass filter is used in playback mode (pins 2 and 3 short-circuited).
3. System headroom is determined by the line output channel in use.
   For low supply voltages line output 2 (pin 6) will saturate at high signal levels. Headroom for line output 1 (pin 5) tracks with record output (pin 21).
4. The equation for REC/PB switch input voltage is:
   REC: $V_{24\text{-}27} > 0{,}55\ V_{CC} - V_{BE} + 1{,}5$ V,
   PB: $V_{24\text{-}27} < 0{,}45\ V_{CC} - V_{BE} - 1{,}5$ V.
5. The equation for C/B/OFF mode switch input voltage is:
   OFF: $V_{25\text{-}27} < 0{,}38\ V_{CC} - V_{BE} - 1$ V,
   B: $0{,}45\ V_{CC} < V_{25\text{-}27} < 0{,}55\ V_{CC}$ (external voltage),
   B: $0{,}5\ V_{CC}$ (switch in open position),
   C: $V_{25\text{-}27} > 0{,}75\ V_{CC} - V_{BE} + 1$ V.
   The voltage drop across the external time constant resistor must be taken in to account.
6. TPL is Test Point Level.

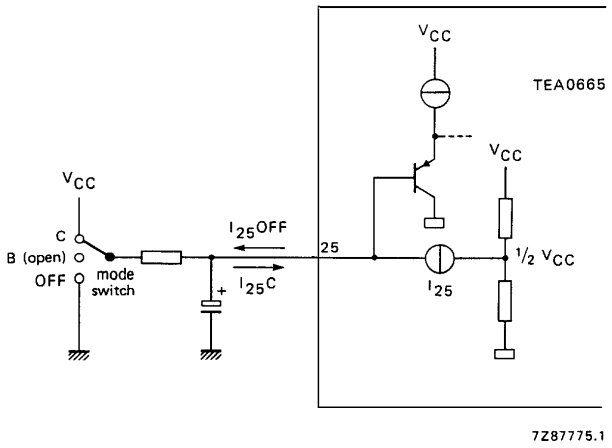


Fig.3 Mode switch input configuration.

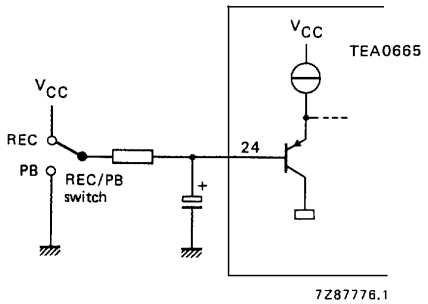


Fig.4 REC/PB switch input configuration.

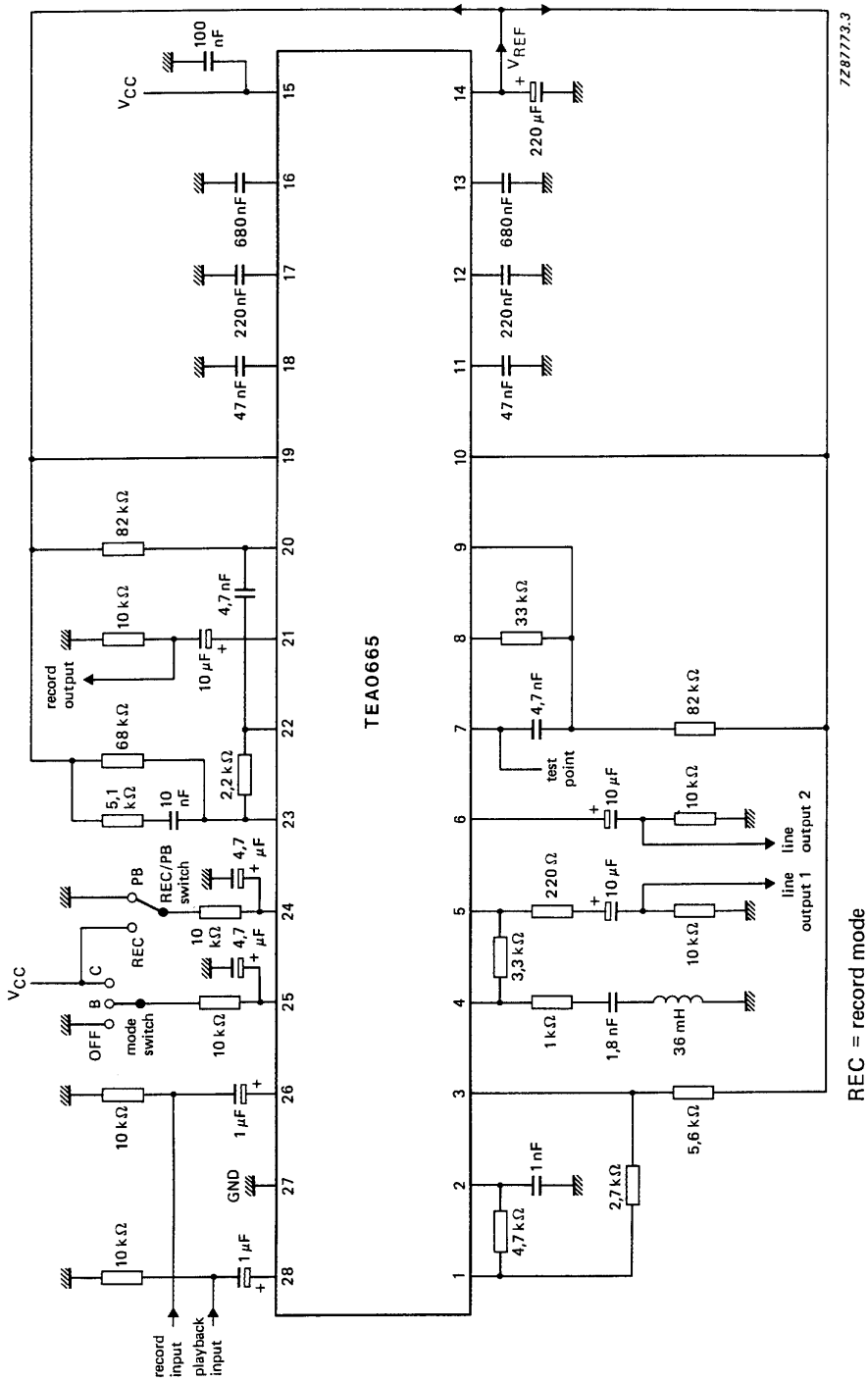


Fig.5 Test circuit.

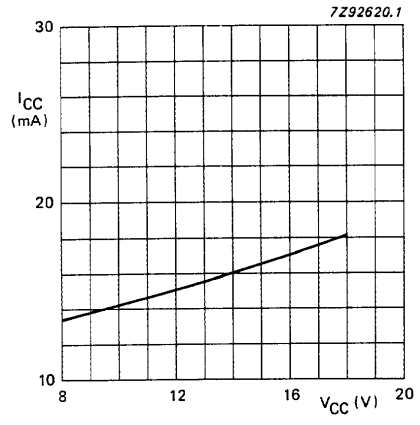


Fig.6 Supply current as a function of supply voltage; $I_{CC} = f(V_{CC})$; no input signal.

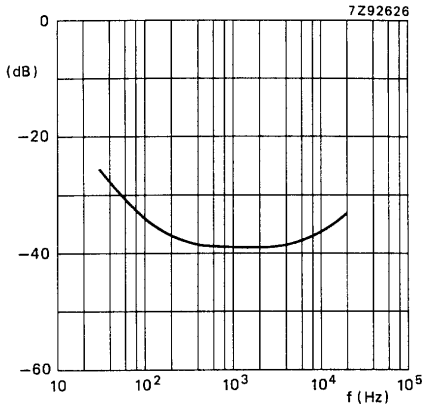


Fig.7 Power supply ripple rejection measured at REC OUT as a function of frequency; level at pin 15 = 100 mV (rms). R_G = 10 kΩ; record mode; NR OFF.

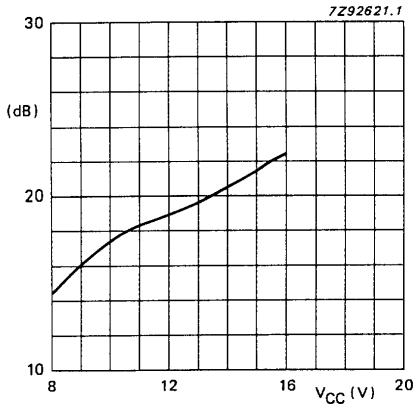


Fig.8 Signal handling = $f(V_{CC})$ measured at REC OUT as function of the supply voltage; THD = 1%.

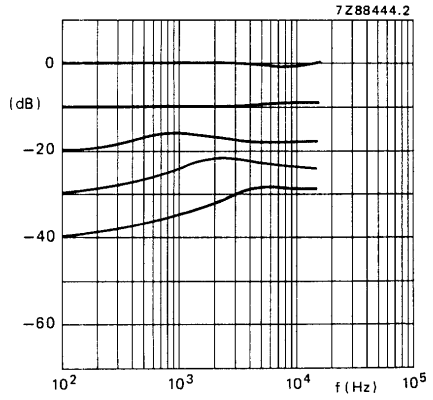


Fig.9 Encoder frequency response for B-mode.

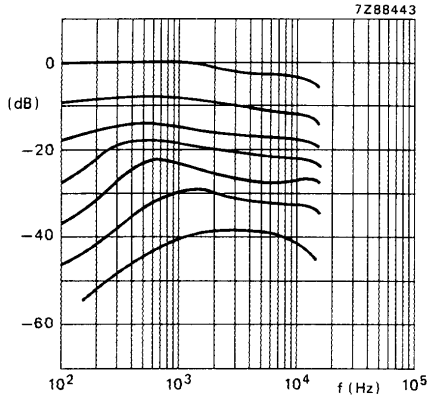


Fig.10 Encoder frequency response for C-mode.

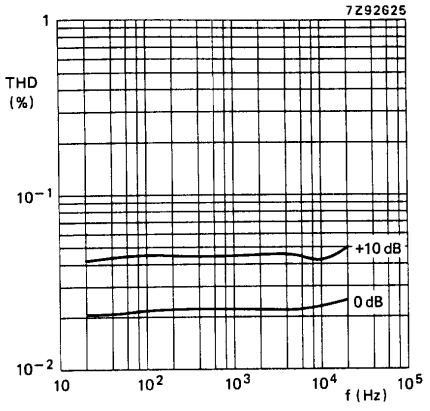


Fig.11 Total harmonic distortion measured at REC OUT as a function of frequency; for NR OFF mode; V_{CC} = 14 V; LPF 80 kHz.

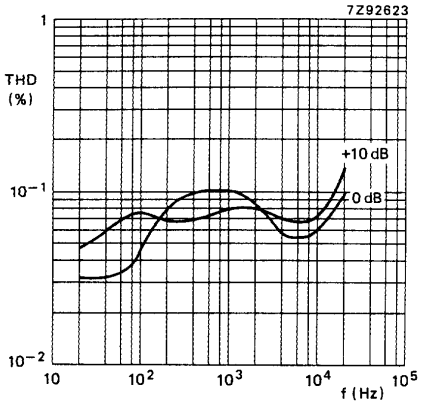


Fig.12 Total harmonic distortion measured at REC OUT as a function of frequency; for B-mode; V_{CC} = 14 V; LPF 80 kHz.

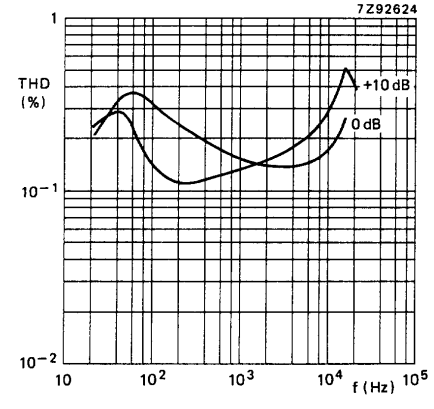


Fig.13 Total harmonic distortion measured at REC OUT as a function of frequency; for C-mode; V_{CC} = 14 V; LPF 80 kHz.

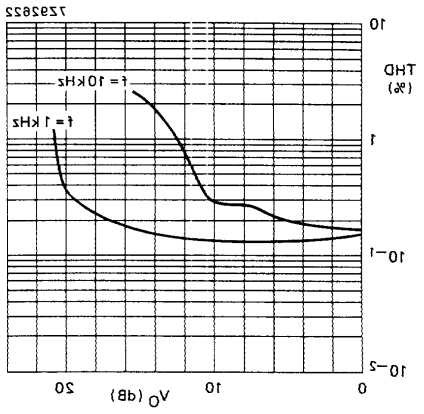


Fig.14 Total harmonic distortion as a function of the record output level (pin 21); for C-mode; V_{CC} = 14 V; LPF 80 kHz.

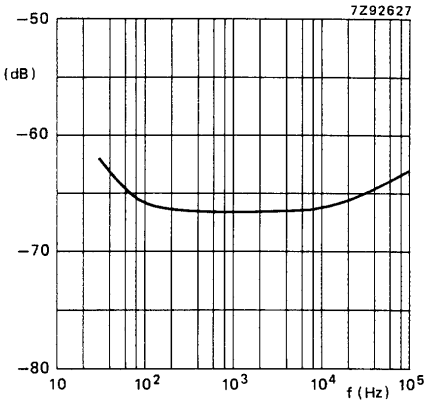
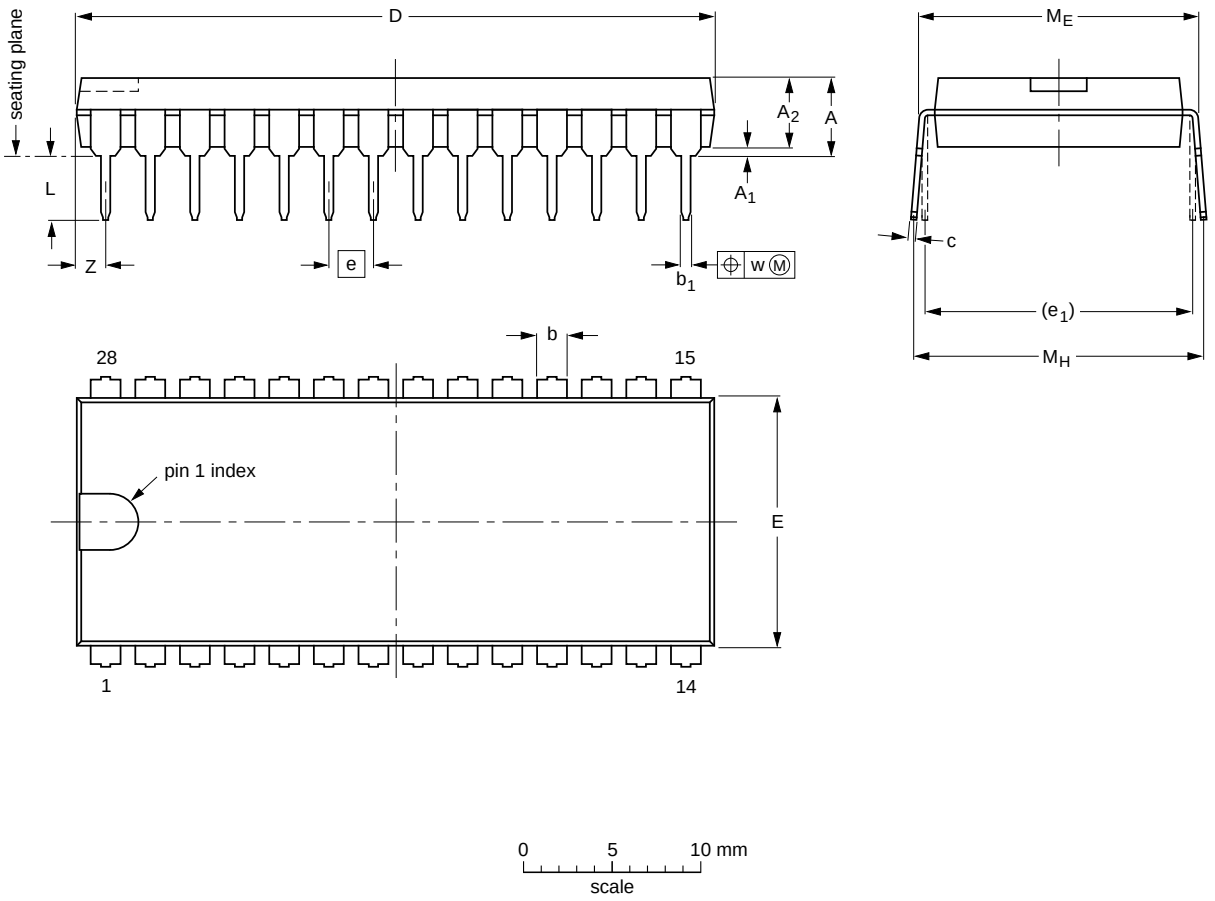


Fig.15 Crosstalk from record input (pin 26) to line output as a function of frequency in playback mode; record input level is 50 mV; NR OFF; R_G = 10 kΩ.

PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

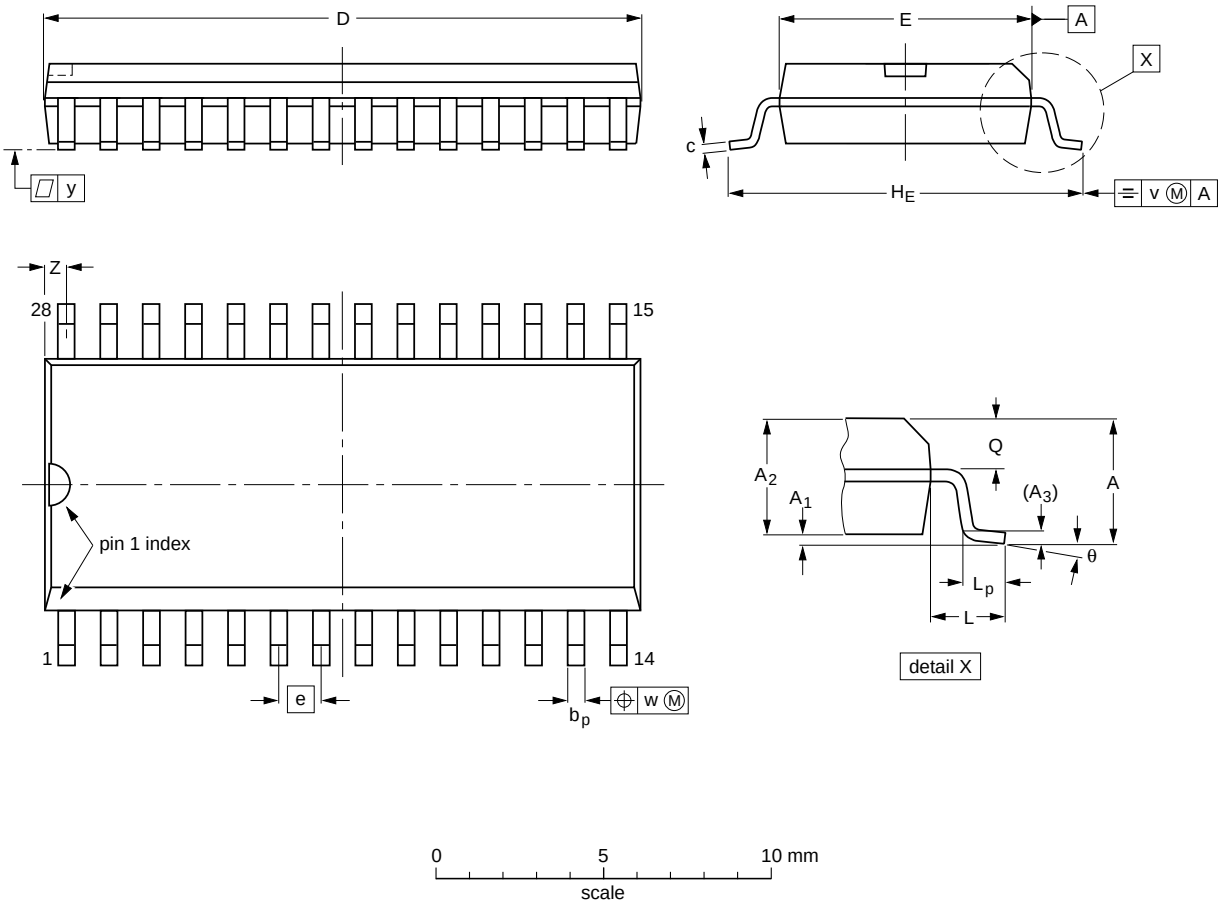
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.