DATA SHEET

TDA9813T
VIF-PLL with QSS-IF and dual FM-PLL demodulator

Product specification
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VIF-PLL with QSS-IF and dual FM-PLL demodulator

TDA9813T

FEATURES

- 5 V supply voltage
- Gain controlled wide band VIF amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Separate video amplifier for sound trap buffering with high video bandwidth
- VIF-AGC detector for gain control, operating as peak sync detector
- Tuner AGC with adjustable takeover point (TOP)
- AFC detector without extra reference circuit
- AC-coupled limiter amplifier for sound intercarrier signal
- Two alignment-free FM-PLL demodulators with high linearity
- SIF input for single reference QSS mode (PLL controlled); SIF-AGC detector for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- ESD protection for all pins.

GENERAL DESCRIPTION

The TDA9813T is an integrated circuit for vision IF signal processing and sound dual FM demodulation, with single reference QSS-IF in TV and VCR sets. For negative modulation standards only.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9813T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	5	5.5	V
I_P	supply current		93	109	125	mA
$V_{i\ VIF(rms)}$	vision IF input signal voltage sensitivity (RMS value)	–1 dB video at output	–	60	100	μV
$V_{o\ CVBS(p-p)}$	CVBS output signal voltage (peak-to-peak value)		1.7	2.0	2.3	V
B_{-3}	–3 dB video bandwidth on pin 8	C_L < 20 pF; R_L > 1 kΩ; AC load	7	8	–	MHz
S/N(W)	weighted signal-to-noise ratio for video		56	60	–	dB
$IM_{\alpha 1.1}$	intermodulation attenuation at ‘blue’	f = 1.1 MHz	58	64	–	dB
$IM_{\alpha 3.3}$	intermodulation attenuation at ‘blue’	f = 3.3 MHz	58	64	–	dB
$\alpha_{H(sup)}$	suppression of harmonics in video signal		35	40	–	dB
$V_{i\ SIF(rms)}$	sound IF input signal voltage sensitivity (RMS value)	–3 dB at intercarrier output	–	30	70	μV
$V_{o(rms)}$	audio output signal voltage for FM (RMS value)	B/G standard; 54% modulation	–	0.5	–	V
THD	total harmonic distortion	54% modulation	–	0.15	0.5	%
S/N(W)	weighted signal-to-noise ratio	54% modulation	–	60	–	dB

BLOCK DIAGRAM

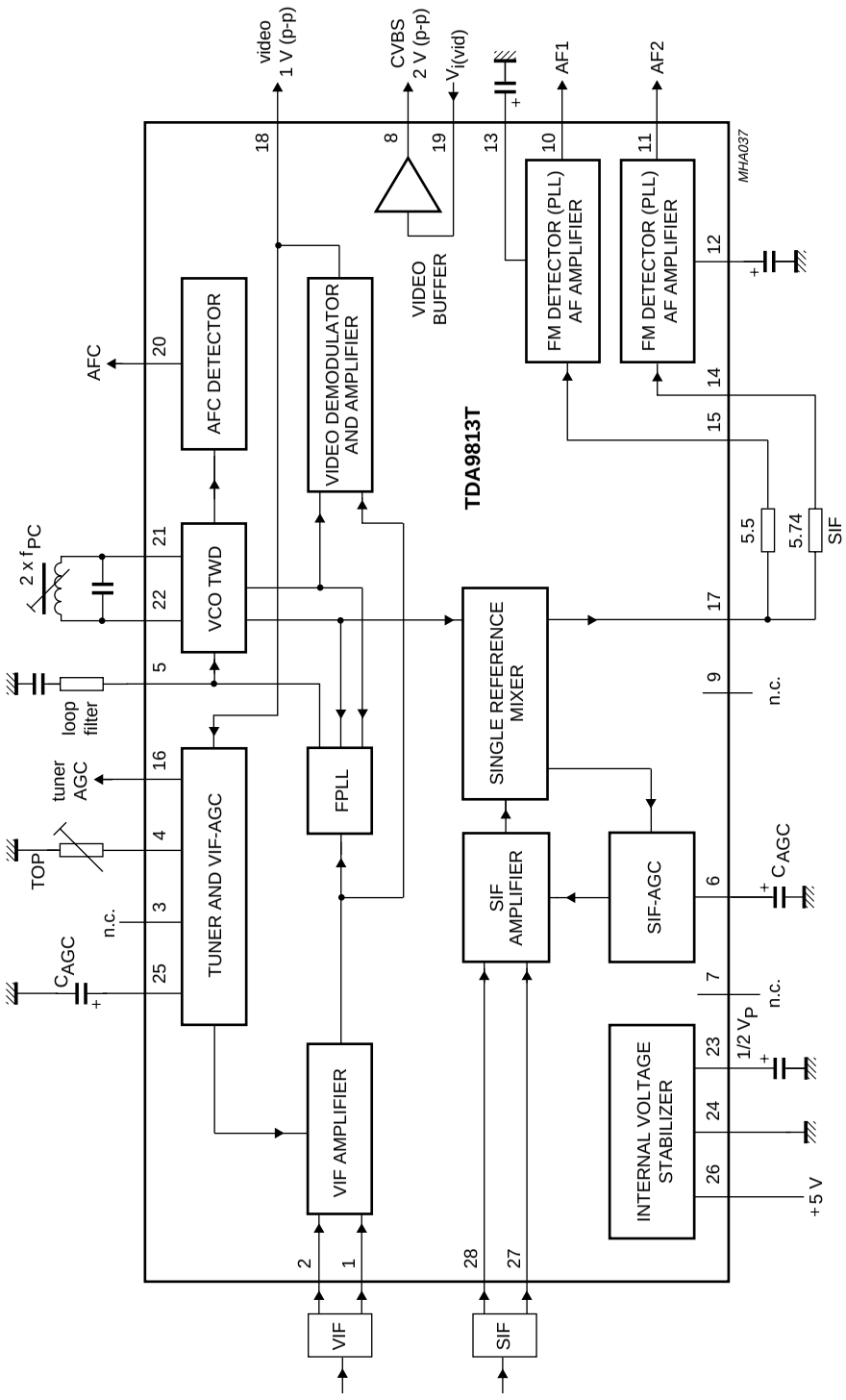


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF1}$	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	VIF differential input signal voltage 2
n.c.	3	not connected
TADJ	4	tuner AGC takeover adjust (TOP)
T_{PLL}	5	PLL loop filter
C_{SAGC}	6	SIF-AGC capacitor
n.c.	7	not connected
$V_{o\ CVBS}$	8	CVBS output signal voltage
n.c.	9	not connected
$V_{o\ AF1}$	10	audio voltage frequency output 1
$V_{o\ AF2}$	11	audio voltage frequency output 2
C_{DEC2}	12	decoupling capacitor 2
C_{DEC1}	13	decoupling capacitor 1
$V_{i\ FM2}$	14	sound intercarrier input voltage 2
$V_{i\ FM1}$	15	sound intercarrier input voltage 1
TAGC	16	tuner AGC output
$V_{o\ QSS}$	17	single reference QSS output voltage
$V_{o(vid)}$	18	composite video output voltage
$V_{i(vid)}$	19	video buffer input voltage
AFC	20	AFC output
VCO1	21	VCO1 reference circuit for $2f_{PC}$
VCO2	22	VCO2 reference circuit for $2f_{PC}$
C_{ref}	23	$\frac{1}{2}V_P$ reference capacitor
GND	24	ground
C_{VAGC}	25	VIF-AGC capacitor
V_P	26	supply voltage
$V_{i\ SIF1}$	27	SIF differential input signal voltage 1
$V_{i\ SIF2}$	28	SIF differential input signal voltage 2

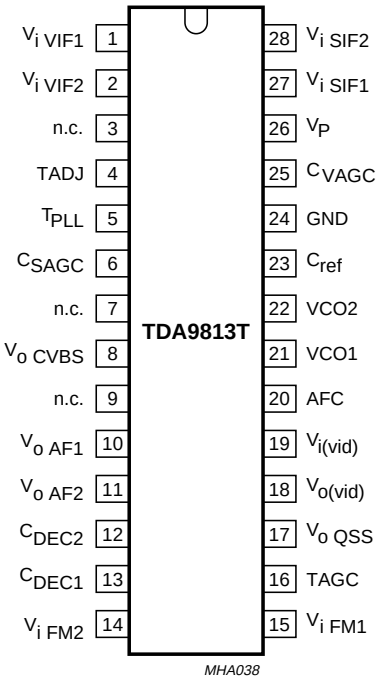


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The integrated circuit comprises the functional blocks as shown in Fig.1:

- Vision IF amplifier
- Tuner and VIF-AGC
- Frequency Phase Locked Loop (FPLL) detector
- VCO, Travelling Wave Divider (TWD) and AFC
- Video demodulator and amplifier
- Video buffer
- SIF amplifier and SIF-AGC
- Single reference Quasi Split Sound (QSS) mixer
- FM-PLL demodulator
- Internal voltage stabilizer and $\frac{1}{2}V_P$ reference.

Vision IF amplifier

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

Tuner and VIF-AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current (open-collector output).
The tuner AGC takeover point can be adjusted. This allows the tuner and the SAW filter to be matched to achieve the optimum IF input level.

The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level. Therefore the sync level of the video signal is detected.

Frequency Phase Locked Loop (FPLL) detector

The VIF amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors.
The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the frequency-phase detector (FPLL) and fed via the loop filter to the first variable capacitor. This control voltage is amplified and additionally converted into a current which represents the AFC output signal. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a TWD which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the ‘in phase’ signal of the travelling wave divider output.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics. The video output signal is 1 V (p-p) for nominal vision IF modulation.

Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used. This amplifier is featured with a high bandwidth and 7 dB gain. The input impedance is adapted for operating in combination with ceramic sound traps. The output stage delivers a nominal 2 V (p-p) positive video signal. Noise clipping is provided.

SIF amplifier and SIF-AGC

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF-AGC detector is related to the SIF input signals (average level of FM carriers) and controls the SIF amplifier to provide a constant SIF signal to the single reference QSS mixer.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 17. With this system a high performance hi-fi stereo sound processing can be achieved.

FM-PLL demodulator

Each FM-PLL demodulator consists of a limiter, an FM-PLL and an AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC-coupled in order to minimize the DC offset and to save pins for DC decoupling.

The second limiter is extended with an additional level detector consisting of a rectifier and a comparator. By means of this the AF2 signal is set to mute and the PLL VCO is switched off, if the intercarrier signal at pin 14 is below 1 mV (RMS) in order to avoid false identification of a stereo decoder. It should be noted that noise at pin 14 disables the mute state (at low SIF input signal), but this will not lead to false identification. This 'auto-mute' function can be disabled by connecting a 5.6 kΩ resistor from pin 14 to V_P (see Fig.11).

Furthermore the AF output signals can be muted by connecting a resistor between the limiter inputs pin 14 or pin 15 and ground.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM demodulator.

The AF amplifier consists of two parts:

1. The AF preamplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal. An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.
2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to FM or mute state, controlled by the mute switching voltage.

Internal voltage stabilizer and $\frac{1}{2}V_P$ reference

The band gap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals the constant reference voltage cannot be used because large output signals are required. Therefore these signals refer to half the supply voltage to achieve a symmetrical headroom, especially for the rail-to-rail output stage. For ripple and noise attenuation the $\frac{1}{2}V_P$ voltage has to be filtered via a low-pass filter by using an external capacitor together with an integrated resistor (f_g = 5 Hz). For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 26)	maximum chip temperature of 125 °C; note 1	0	5.5	V
V_n	voltage at pins 1 to 7, 9 to 16, 19, 20 and 23 to 28		0	V_P	V
$t_{s(max)}$	maximum short-circuit time		–	10	s
V_{16}	tuner AGC output voltage		0	13.2	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	ambient temperature		–20	+70	°C
V_{es}	electrostatic handling voltage	note 2	–300	+300	V

Notes

1. I_P = 125 mA; T_{amb} = 70 °C; $R_{th(j-a)}$ = 80 K/W.
2. Machine model class B (L = 2.5 µH).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; see Table 1 for input frequencies and carrier ratios (B/G standard); input level $V_{i\ IF\ 1\text{-}2}$ = 10 mV RMS value (sync-level); video modulation DSB; residual carrier: 10%; video signal in accordance with *"CCIR, line 17"*; measurements taken in Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 26)						
V_P	supply voltage	note 1	4.5	5	5.5	V
I_P	supply current		93	109	125	mA
Vision IF amplifier (pins 1 and 2)						
$V_{i\ VIF(rms)}$	input signal voltage sensitivity (RMS value)	–1 dB video at output	–	60	100	μV
$V_{i\ max(rms)}$	maximum input signal voltage (RMS value)	+1 dB video at output	120	200	–	mV
$\Delta V_{o(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range; Δf = 5.5 MHz	–	0.7	1	dB
G_{IFcr}	IF gain control range	see Fig.3	65	70	–	dB
$R_{i(diff)}$	differential input resistance	note 2	1.7	2.2	2.7	kΩ
$C_{i(diff)}$	differential input capacitance	note 2	1.2	1.7	2.5	pF
$V_{1,2}$	DC input voltage	note 2	–	3.4	–	V
True synchronous video demodulator; note 3						
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$	125	130	–	MHz
$\Delta f_{osc}/\Delta T$	oscillator drift as a function of temperature	oscillator is free-running; I_{AFC} = 0; note 4	–	–	$\pm 20 \times 10^{-6}$	K^{-1}
$V_{o\ ref(rms)}$	oscillator voltage swing at pins 21 and 22 (RMS value)		70	100	130	mV
$f_{PC\ CR}$	picture carrier capture range		±1.4	±1.8	–	MHz
t_{acq}	acquisition time	BL = 75 kHz; note 5	–	–	30	ms
$V_{i\ VIF(rms)}$	VIF input signal voltage sensitivity for PLL to be locked (RMS value; pins 1 and 2)	maximum IF gain; note 6	–	30	70	μV
Composite video amplifier (pin 18; sound carrier off)						
$V_{o\ video(p\text{-}p)}$	output signal voltage (peak-to-peak value)	see Fig.8	0.88	1.0	1.12	V
V/S	ratio between video (black-to-white) and sync level		1.9	2.33	3.0	–
$V_{18(sync)}$	sync voltage level		–	1.5	–	V
$V_{18(clu)}$	upper video clipping voltage level		V_P – 1.1	V_P – 1	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{18(cll)}$	lower video clipping voltage level		–	0.7	0.9	V
$R_{o,18}$	output resistance	note 2	–	–	10	Ω
$I_{int\ 18}$	internal DC bias current for emitter-follower		2.2	3.0	–	mA
$I_{18\ max(sink)}$	maximum AC and DC output sink current		1.6	–	–	mA
$I_{18\ max(source)}$	maximum AC and DC output source current		2.9	–	–	mA
B_{-1}	–1 dB video bandwidth	C_L < 50 pF; R_L > 1 kΩ; AC load	5	6	–	MHz
B_{-3}	–3 dB video bandwidth	C_L < 50 pF; R_L > 1 kΩ; AC load	7	8	–	MHz
$\alpha_{H(sup)}$	suppression of video signal harmonics	C_L < 50 pF; R_L > 1 kΩ; AC load; note 7a	35	40	–	dB
PSRR	power supply ripple rejection at pin 18	video signal; grey level; see Fig.9	32	35	–	dB
CVBS buffer amplifier (only) and noise clipper (pins 8 and 19)						
$R_{i,19}$	input resistance	note 2	2.6	3.3	4.0	kΩ
$C_{i,19}$	input capacitance	note 2	1.4	2	3.0	pF
$V_{I,19}$	DC input voltage		1.4	1.7	2.0	V
G_v	voltage gain	note 8	6.5	7	7.5	dB
$V_{8(clu)}$	upper video clipping voltage level		3.9	4.0	–	V
$V_{8(cll)}$	lower video clipping voltage level		–	1.0	1.1	V
$R_{o,8}$	output resistance	note 2	–	–	10	Ω
$I_{int\ 8}$	DC internal bias current for emitter-follower		2.0	2.5	–	mA
$I_{o,8\ max(sink)}$	maximum AC and DC output sink current		1.4	–	–	mA
$I_{o,10\ max(source)}$	maximum AC and DC output source current		2.4	–	–	mA
B_{-1}	–1 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load	8.4	11	–	MHz
B_{-3}	–3 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load	11	14	–	MHz
Measurements from IF input to CVBS output (pin 8; 330 Ω between pins 18 and 19, sound carrier off)						
$V_{o\ CVBS(p-p)}$	CVBS output signal voltage on pin 8 (peak-to-peak value)	note 8	1.7	2.0	2.3	V
$V_{o\ CVBS(sync)}$	sync voltage level		–	1.35	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_o	deviation of CVBS output signal voltage at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
$\Delta V_{o(blB/G)}$	black level tilt in B/G standard	gain variation; note 9	–	–	1	%
G_{diff}	differential gain	*"CCIR, line 330"*	–	2	5	%
φ_{diff}	differential phase	*"CCIR, line 330"*	–	1	2	deg
B_{-1}	–1 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load	5	6	–	MHz
B_{-3}	–3 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load	7	8	–	MHz
S/N(W)	weighted signal-to-noise ratio	see Fig.5 and note 10	56	60	–	dB
S/N	unweighted signal-to-noise ratio	see Fig.5 and note 10	49	53	–	dB
$IM\alpha_{1.1}$	intermodulation attenuation at 'blue'	f = 1.1 MHz; see Fig.6 and note 11	58	64	–	dB
	intermodulation attenuation at 'yellow'	f = 1.1 MHz; see Fig.6 and note 11	60	66	–	dB
$IM\alpha_{3.3}$	intermodulation attenuation at 'blue'	f = 3.3 MHz; see Fig.6 and note 11	58	64	–	dB
	intermodulation attenuation at 'yellow'	f = 3.3 MHz; see Fig.6 and note 11	59	65	–	dB
$\alpha_{pc(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics	–	2	5	mV
$\alpha_{H(sup)}$	suppression of video signal harmonics	note 7a	35	40	–	dB
$\alpha_{H(spur)}$	spurious elements	note 7b	40	–	–	dB
PSRR	power supply ripple rejection at pin 8	video signal; grey level; see Fig.9	25	28	–	dB
VIF-AGC detector (pin 25)						
I_{25}	charging current	note 9	0.75	1	1.25	mA
	discharging current		15	20	25	µA
t_{resp}	AGC response to an increasing VIF step	note 12	–	0.05	0.1	ms/dB
	AGC response to a decreasing VIF step		–	2.2	3.5	ms/dB
Tuner AGC (pin 16)						
$V_{i(rms)}$	IF input signal voltage for minimum starting point of tuner takeover (RMS value)	input at pins 1 and 2; R_{TOP} = 22 kΩ; I_{16} = 0.4 mA	–	2	5	mV
	IF input signal voltage for maximum starting point of tuner takeover (RMS value)	input at pins 1 and 2; R_{TOP} = 0 Ω; I_{16} = 0.4 mA	50	100	–	mV
$V_{o,16}$	permissible output voltage	from external source; note 2	–	–	13.2	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{sat,16}$	saturation voltage	I_{16} = 1.5 mA	–	–	0.2	V
$\Delta V_{TOP,16}/\Delta T$	variation of takeover point by temperature	I_{16} = 0.4 mA	–	0.03	0.07	dB/K
$I_{16(sink)}$	sink current	see Fig.3				
		no tuner gain reduction; V_{16} = 13.2 V	–	–	1	μA
		maximum tuner gain reduction	1.5	2	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20% to 80%	–	6	8	dB
AFC circuit (pin 20); see Fig.7 and note 13						
S	control steepness $\Delta I_{20}/\Delta f$	note 14	0.5	0.75	1.0	μA/kHz
$\Delta f_{IF}/\Delta T$	frequency variation by temperature	I_{AFC} = 0; note 5	–	–	$\pm 20 \times 10^{-6}$	K^{-1}
$V_{o,20}$	output voltage upper limit	see Fig.7 without external components	V_P – 0.6	V_P – 0.3	–	V
	output voltage lower limit		–	0.3	0.6	V
$I_{o,20(source)}$	output source current	see Fig.7	150	200	250	μA
$I_{o,20(sink)}$	output sink current		150	200	250	μA
$\Delta I_{20(p-p)}$	residual video modulation current (peak-to-peak value)		–	20	30	μA
Sound IF amplifier (pins 27 and 28)						
$V_{i\ SIF(rms)}$	input signal voltage sensitivity (RMS value)	–3 dB at intercarrier output pin 17	–	30	70	μV
$V_{i\ max(rms)}$	maximum input signal voltage (RMS value)	+1 dB at intercarrier output pin 17	50	70	–	mV
G_{SIFcr}	SIF gain control range	see Fig.4	60	67	–	dB
$R_{i(diff)}$	differential input resistance	note 2	1.7	2.2	2.7	kΩ
$C_{i(diff)}$	differential input capacitance	note 2	1.2	1.7	2.5	pF
$V_{I(27,28)}$	DC input voltage		–	3.4	–	V
$\alpha_{ct(SIF,VIF)}$	crosstalk attenuation between SIF and VIF input	between pins 1 and 2 and pins 27 and 28; note 15	50	–	–	dB
SIF-AGC detector (pin 6)						
I_6	charging current		8	12	16	μA
	discharging current		8	12	16	μA
Single reference QSS intercarrier mixer (B/G standard; pin 17)						
$V_{o(rms)}$	IF intercarrier level (RMS value)	SC_1; sound carrier 2 off	75	100	125	mV
B_{-3}	–3 dB intercarrier bandwidth	upper limit	7.5	9	–	MHz
$\alpha_{SC(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	2	–	mV
$R_{o,17}$	output resistance	note 2	–	–	25	Ω
$V_{O,17}$	DC output voltage		–	2.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{int\ 17}$	DC internal bias current for emitter-follower		1.5	1.9	–	mA
$I_{17\ max(sink)}$	maximum AC and DC output sink current		1.1	1.5	–	mA
$I_{17\ max(source)}$	maximum AC and DC output source current		3.0	3.5	–	mA
Limiter amplifier 1 (pin 15); note 16						
$V_{i\ FM(rms)}$	input signal voltage for lock-in (RMS value)		–	–	100	μV
$V_{i\ FM(rms)}$	input signal voltage (RMS value)	$\frac{S+N}{N}$ = 40 dB	–	300	400	μV
	allowed input signal voltage (RMS value)		200	–	–	mV
$R_{i,15}$	input resistance	note 2	480	600	720	Ω
$V_{I,15}$	DC input voltage		–	2.8	–	V
Limiter amplifier 2 (pin 14); note 16						
$V_{i\ FM(rms)}$	input signal voltage for lock-in (RMS value)		–	–	100	μV
$V_{i\ FM(rms)}$	input signal voltage (RMS value)	$\frac{S+N}{N}$ = 40 dB PLL1 has to be in locked mode; auto mute off	–	300	400	μV
	allowed input signal voltage (RMS value)		200	–	–	mV
	input signal voltage for no auto mute; PLL enabled (RMS value)		0.7	1	1.5	mV
HYS_{14}	hysteresis of level detector for auto mute		–3	–6	–8	dB
$R_{i,14}$	input resistance	note 2	480	600	720	Ω
$V_{I,14}$	DC input voltage		–	2.0	–	V
FM-PLL demodulator						
$f_{i\ FM(catch)}$	catching range of PLL	upper limit	7.0	–	–	MHz
		lower limit	–	–	4.0	MHz
$f_{i\ FM(hold)}$	holding range of PLL	upper limit	8.0	–	–	MHz
		lower limit	–	–	3.5	MHz
t_{acq}	acquisition time		–	–	4	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM operation (B/G standard; pins 10 and 11); notes 16 and 16a						
$V_{o\ AF10,11(rms)}$	AF output signal voltage (RMS value)	27 kHz (54% FM deviation); see Fig.11 and note 17				
		$R_x = R_y = 470\ \Omega$	200	250	300	mV
		$R_x = R_y = 0\ \Omega$	400	500	600	mV
$V_{o\ AF10,11(cl)}$	AF output clipping signal voltage level	THD < 1.5%	1.3	1.4	–	V
Δf_{AF}	frequency deviation	THD < 1.5%; note 17	–	–	±53	kHz
$\Delta V_o/\Delta T$	temperature drift of AF output signal voltage		–	3×10^{-3}	7×10^{-3}	dB/K
$V_{12,13}$	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 18	1.2	–	3.0	V
$R_{10,11}$	output resistance	note 2	–	–	100	Ω
$V_{10,11}$	DC output voltage	tracked with supply voltage	–	$\frac{1}{2}V_P$	–	V
$I_{10,11max(sink)}$	maximum AC and DC output sink current		–	–	1.1	mA
$I_{10,11max(source)}$	maximum AC and DC output source current		–	–	1.1	mA
B_{-3}	–3 dB video bandwidth		100	125	–	kHz
THD	total harmonic distortion		–	0.15	0.5	%
S/N(W)	weighted signal-to-noise ratio	FM-PLL only; with 50 µs de-emphasis; 27 kHz (54% FM deviation); *"CCIR 468-4"*	55	60	–	dB
$\alpha_{SC(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	–	75	mV
α_{AM}	AM suppression	50 µs de-emphasis; AM: f = 1 kHz; m = 0.3 refer to 27 kHz (54% FM deviation)	46	50	–	dB
$\alpha_{10,11}$	mute attenuation of AF signal		70	80	–	dB
$\Delta V_{10,11}$	DC jump voltage of AF output terminals for switching AF output to mute state and vice versa	FM-PLLs in lock mode; note 19	–	±50	±150	mV
PSRR	power supply ripple rejection at pins 10 and 11	$R_x = R_y = 0\ \Omega$; see Figs 9 and 11	22	28	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single reference QSS AF performance for FM operation (B/G standard); see Table 1 and notes 20, 21 and 22						
S/N(W)	weighted signal-to-noise ratio (SC_1/SC_2)	PC/SC_1 ratio at pins 1 and 2; 27 kHz (54% FM deviation); *"CCIR 468-4"*	40	–	–	dB
		black picture	53/48	58/55	–	dB
		white picture	50/46	55/52	–	dB
		6 kHz sine wave; black-to-white modulation	42/40	48/46	–	dB
		250 kHz square wave; black-to-white modulation; see note 2 in Fig.12	45/42	53/50	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	45/44	51/50	–	dB
		sound carrier subharmonics; f = 2.87 MHz ±3 kHz	46/45	52/51	–	dB

Notes

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as application information for designing the television receiver.
3. Loop bandwidth BL = 75 kHz (natural frequency f_n = 11 kHz; damping factor d ≈ 3.5; calculated with sync level within gain control range). Resonance circuit of VCO: $Q_0 > 50$; C_{ext} = 8.2 pF ±0.25 pF; C_{int} ≈ 8.5 pF (loop voltage approximately 2.7 V).
4. Temperature coefficient of external LC circuit is equal to zero.
5. $V_{i\,IF}$ = 10 mV RMS; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i\,IF}$ signal for nominal video signal.
7. Measurements taken with SAW filter G3962 (sound carrier suppression: 40 dB); loop bandwidth BL = 75 kHz:
   a) Modulation VSB; sound carrier **off**; $f_{video} > 0.5$ MHz.
   b) Sound carrier **on**; SIF SAW filter G9353; f_{video} = 10 kHz to 10 MHz.
8. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p), in event of CVBS video amplifier output typical 1 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (between pin 18 and pin 19).
9. The leakage current of the AGC capacitor should not exceed 1 μA. Larger currents will increase the tilt.
10. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value), on pin 8. B = 5 MHz weighted in accordance with *"CCIR 567"*.
11. The intermodulation figures are defined:

    $$\alpha_{1.1} = 20\ \log\left(\frac{V_0 \text{ at } 4.4\text{ MHz}}{V_0 \text{ at } 1.1\text{ MHz}}\right) + 3.6\ \text{dB}$$; $\alpha_{1.1}$ value at 1.1 MHz referenced to black/white signal;

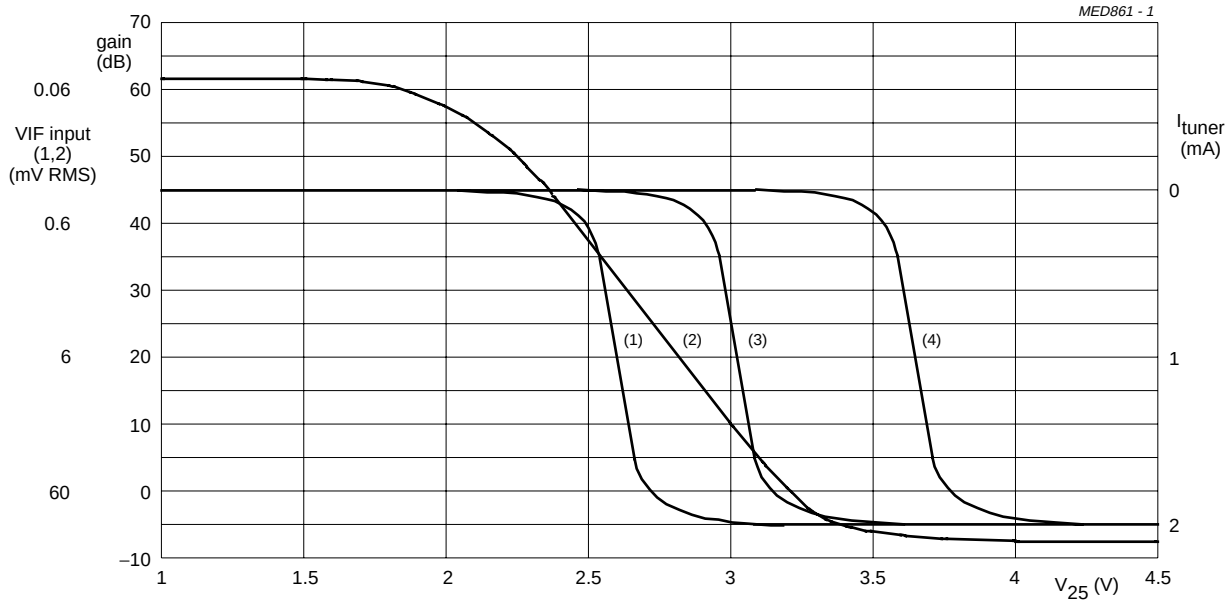
    $$\alpha_{3.3} = 20\ \log\left(\frac{V_0 \text{ at } 4.4\text{ MHz}}{V_0 \text{ at } 3.3\text{ MHz}}\right)$$; $\alpha_{3.3}$ value at 3.3 MHz referenced to colour carrier.

12. Response speed valid for a VIF input level range of 200 μV up to 70 mV.

13. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.7. The AFC steepness can be changed by the resistors at pin 20.
14. Depending on the ratio $\Delta C/C_0$ of the LC resonant circuit of VCO ($Q_0 > 50$; see note 3; $C_0 = C_{int} + C_{ext}$).
15. Source impedance: 2.3 kΩ in parallel to 12 pF (SAW filter); f_{IF} = 38.9 MHz.
16. Input level for second IF from an external generator with 50 Ω source impedance. AC-coupled with 10 nF capacitor, f_{mod} = 1 kHz, 27 kHz (54% FM deviation) of audio references. A VIF/SIF input signal is not permitted. Pins 6 and 25 have to be connected to positive supply voltage for minimum IF gain. S/N and THD measurements are taken at 50 μs de-emphasis. The not tested FM-PLL has to be locked to an unmodulated carrier.
    a) Second IF input level 10 mV RMS.
17. Measured with an FM deviation of 27 kHz the typical AF output signal is 500 mV RMS ($R_x = R_y = 0$ Ω; see Fig.11). By using $R_x = R_y = 470$ Ω the AF output signal is attenuated by 6 dB (250 mV RMS) and adapted to the stereo decoder family TDA9840. For handling an FM deviation of more than 53 kHz the AF output signal has to be reduced by using R_x and R_y in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended with $R_x = R_y = 470$ Ω.
18. The leakage current of the decoupling capacitor (2.2 μF) should not exceed 1 μA.
19. In the event of activated auto mute state the second FM-PLL oscillator is switched off, if the input signal at pin 14 is missing or too weak (see Fig.11). In the event of switching the second FM-PLL oscillator on by the auto mute stage an increased DC jump is the consequence. It should be noted that noise at pin 14 disables the mute state (at low SIF input signal), but this will not lead to false identification of the stereo decoder family TDA9840.
20. For all S/N measurements the used vision IF modulator has to meet the following specifications:
    a) Incidental phase modulation for black-to-white jump less than 0.5 degrees.
    b) QSS AF performance, measured with the television-demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (deviation 27 kHz) for 6 kHz sine wave black-to-white video modulation.
    c) Picture-to-sound carrier ratio; PC/SC_1 = 13 dB (transmitter).
21. Measurements taken with SAW filter G3962 (Siemens) for vision IF (suppressed sound carrier) and G9350 (Siemens) for sound IF (suppressed picture carrier). Input level $V_{i\ SIF}$ = 10 mV RMS, 27 kHz (54% FM deviation).
22. The PC/SC ratio at pins 1 and 2 is calculated as the addition of TV transmitter PC/SC ratio and SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N(W) values as noted. A different PC/SC ratio will change these values.

Table 1 Input frequencies and carrier ratios

DESCRIPTION	SYMBOL	B/G STANDARD	UNIT
Picture carrier	f_{PC}	38.9	MHz
Sound carrier	f_{SC1}	33.4	MHz
	f_{SC2}	33.158	MHz
Picture-to-sound carrier ratio	SC_1	13	dB
	SC_2	20	dB



(1) I_{tuner}; R_{TOP} = 22 kΩ.
(2) Gain.
(3) I_{tuner}; R_{TOP} = 11 kΩ.
(4) I_{tuner}; R_{TOP} = 0 Ω.

Fig.3 Typical VIF and tuner AGC characteristic.

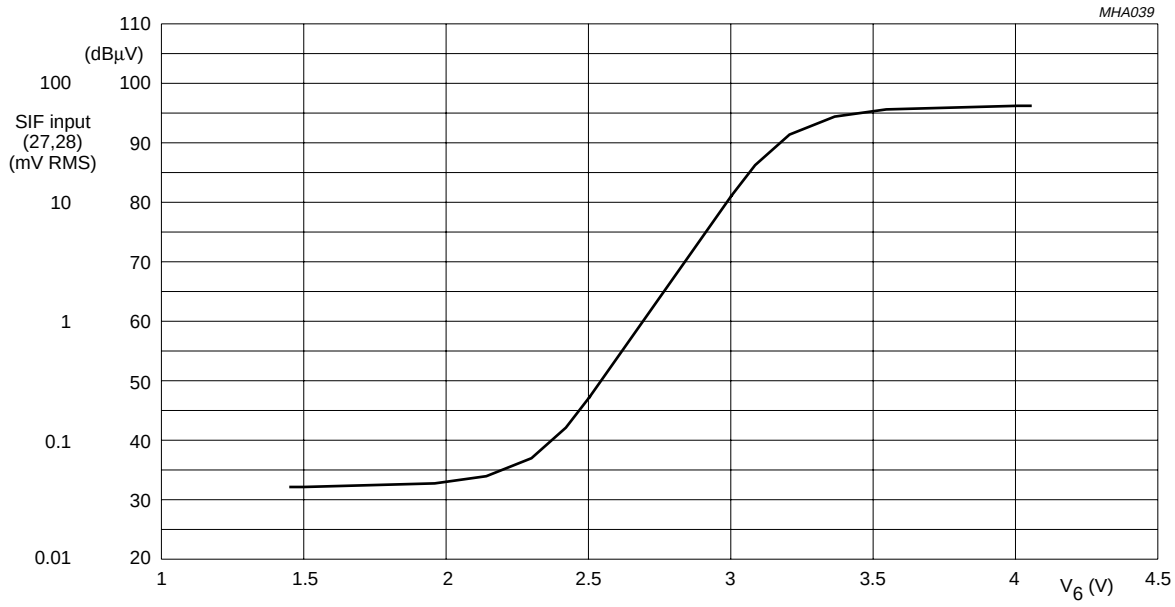


Fig.4 Typical SIF-AGC characteristic.

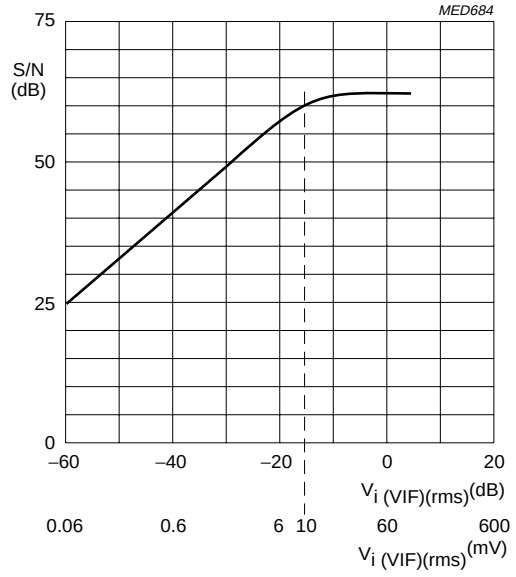
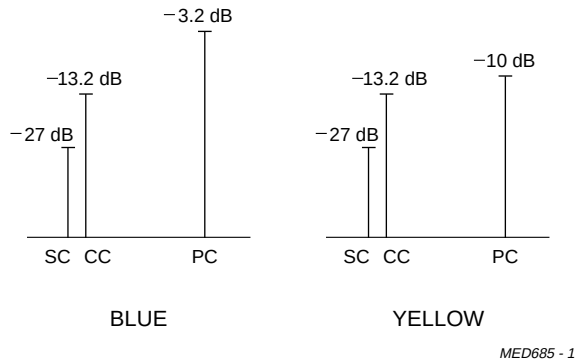


Fig.5 Typical signal-to-noise ratio as a function of IF input voltage.



SC = sound carrier, with respect to sync level.
CC = chrominance carrier, with respect to sync level.
PC = picture carrier, with respect to sync level.
The sound carrier levels are taking into account a sound shelf attenuation of 20 dB (SAW filter G1962).

Fig.6 Input signal conditions.

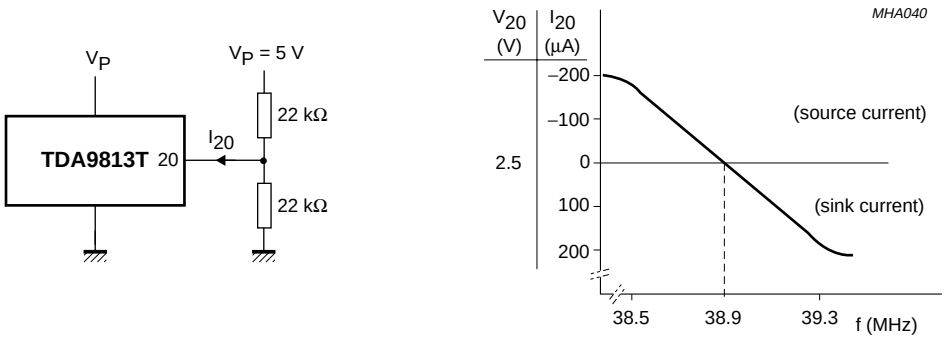


Fig.7 Measurement conditions and typical AFC characteristic.

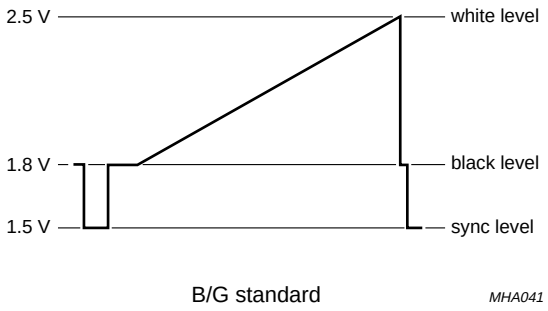


Fig.8 Typical video signal levels on output pin 18 (sound carrier **off**).

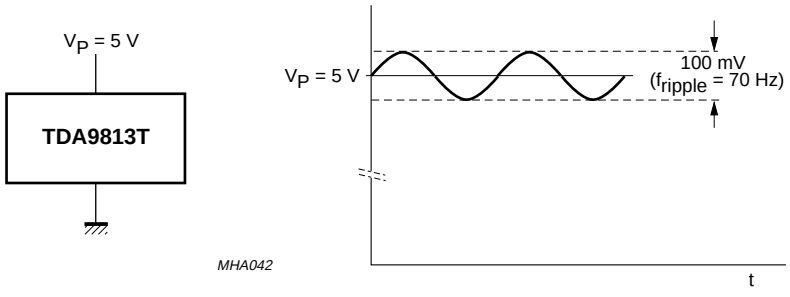
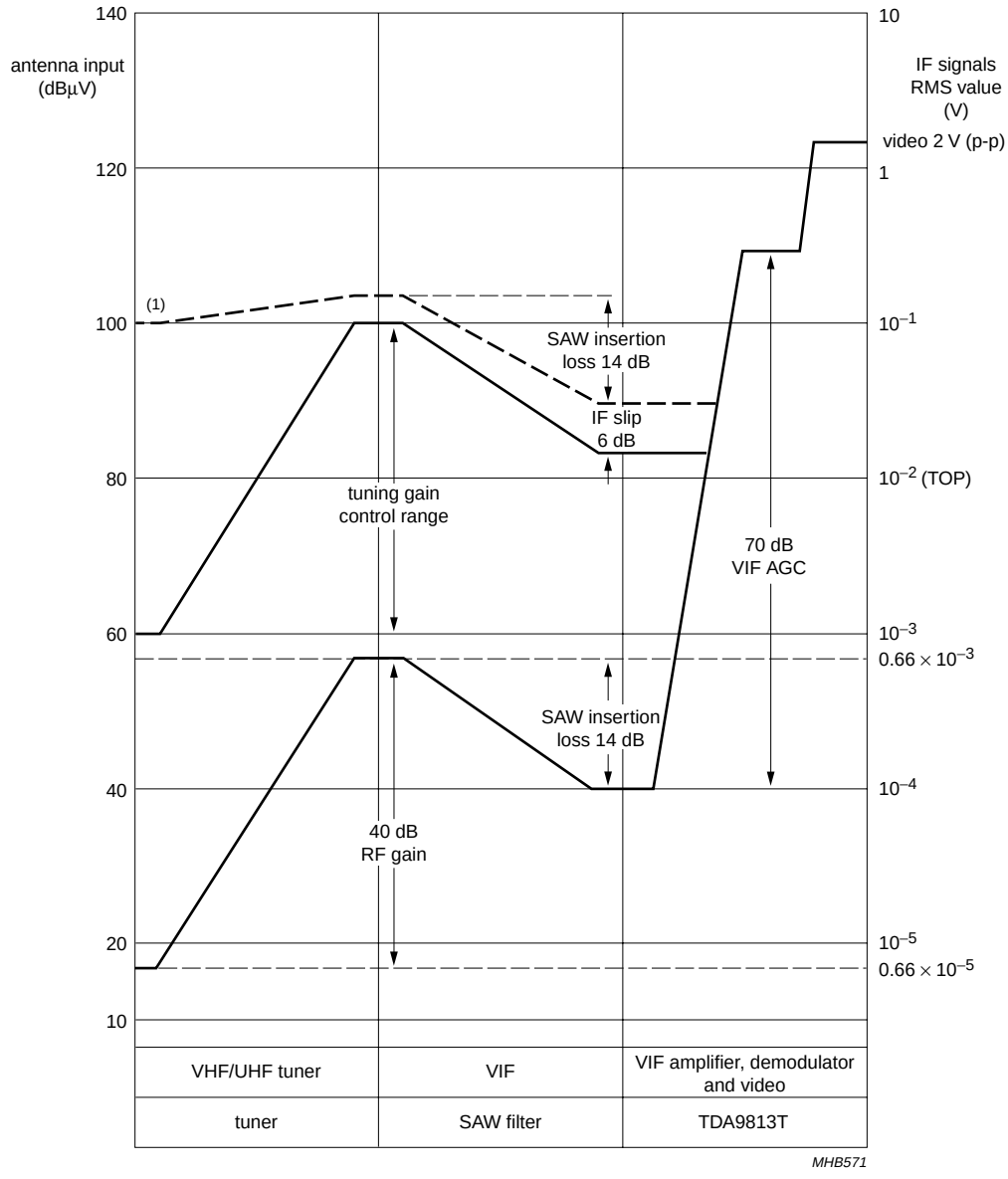


Fig.9 Ripple rejection condition.

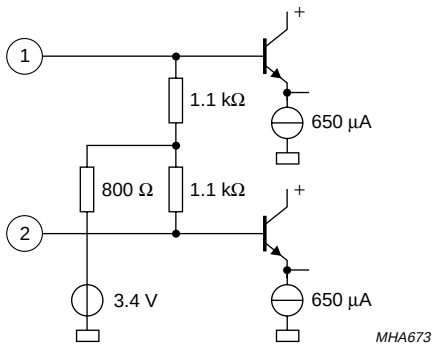
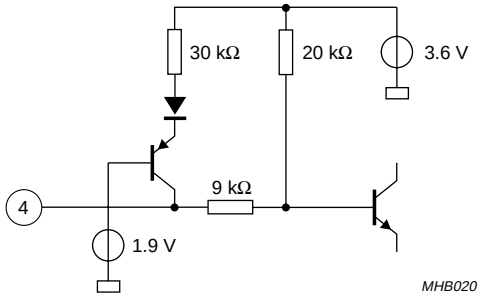
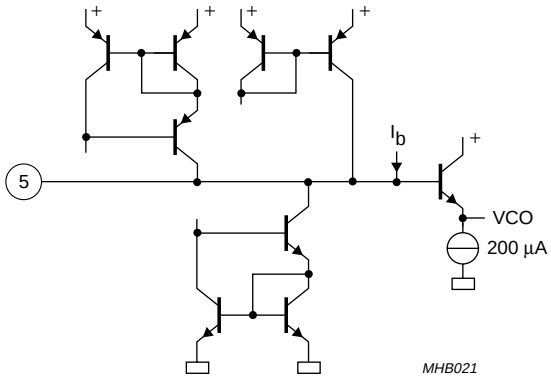


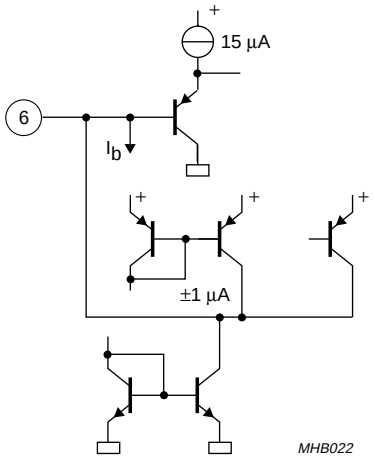
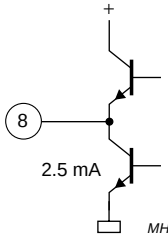
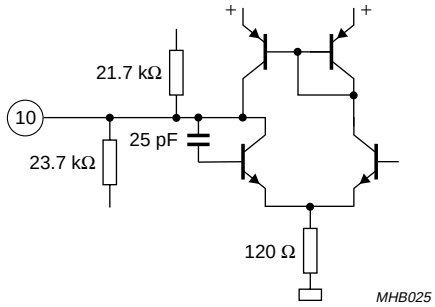
(1) Depends on TOP.

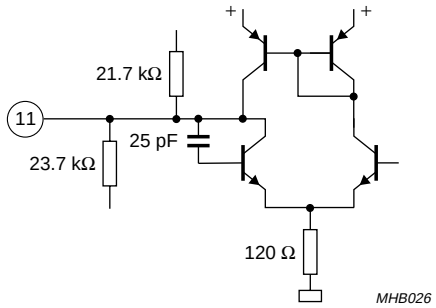
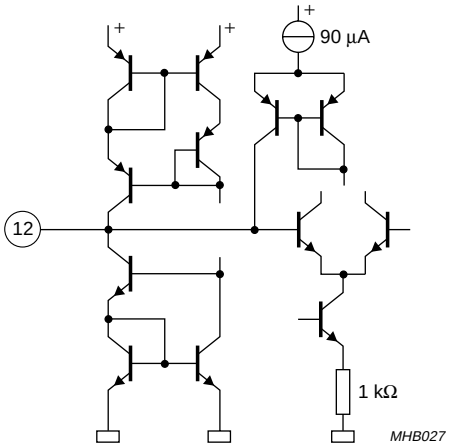
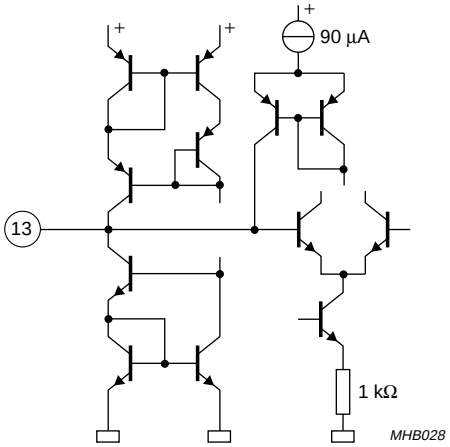
Fig.10 Front-end level diagram.

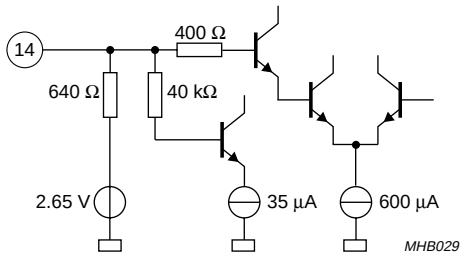
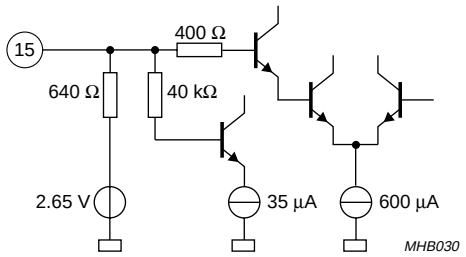
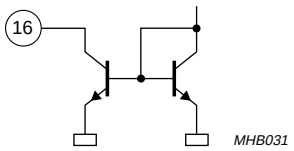
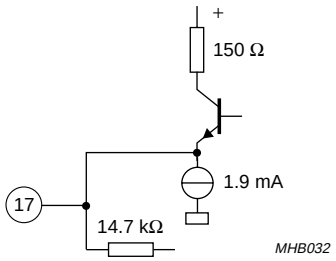
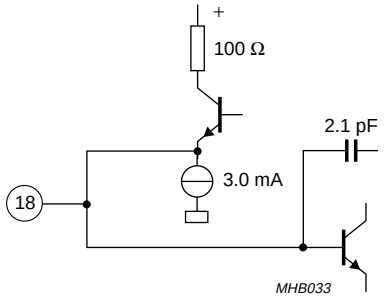
INTERNAL CIRCUITRY

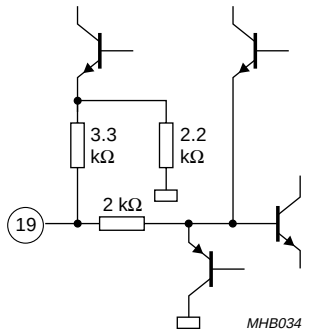
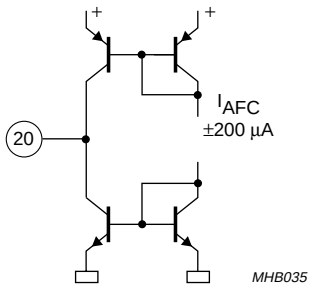
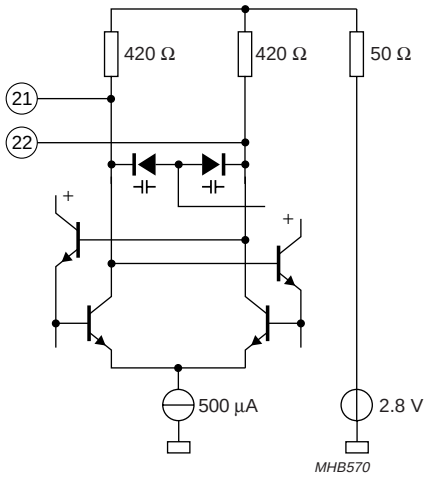
Table 2 Equivalent pin circuits and pin voltages

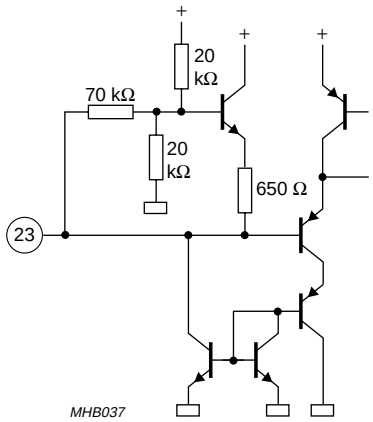
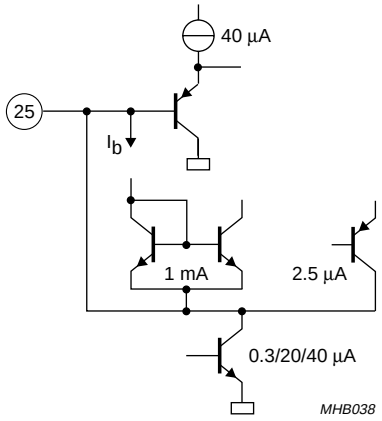
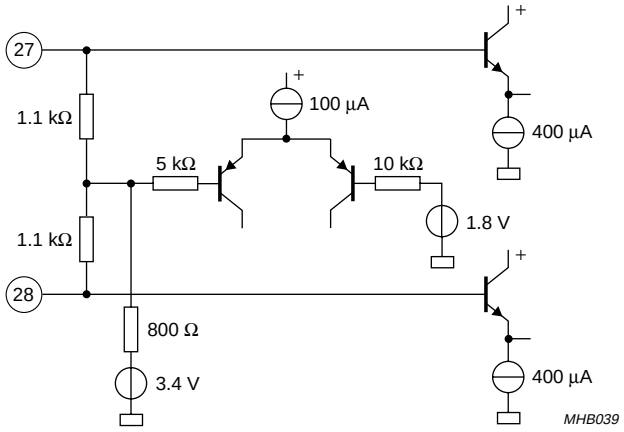
PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
1	$V_{i\ VIF1}$	3.4	
2	$V_{i\ VIF2}$	3.4	
3	n.c.	–	
4	TADJ	0 to 1.9	
5	T_{PLL}	1.5 to 4.0	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
6	C_{SAGC}	1.5 to 4.0	
7	n.c.	–	
8	$V_{o\ CVBS}$	sync level: 1.35	
9	n.c.	–	
10	$V_{o\ AF1}$	2.3	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
11	$V_{o\ AF2}$	2.3	
12	C_{DEC2}	1.2 to 3.0	
13	C_{DEC1}	1.2 to 3.0	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
14	$V_{i\ FM2}$	2.65	
15	$V_{i\ FM1}$	2.65	
16	TAGC	0 to 13.2	
17	$V_{o\ QSS}$	2.0	
18	$V_{o(vid)}$	sync level: 1.5	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
19	$V_{i(vid)}$	1.7	
20	AFC	0.3 to V_P – 0.3	
21	VCO1	2.7	
22	VCO2	2.7	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
23	C_{ref}	$\frac{1}{2}V_P$	
24	GND	0	
25	C_{VAGC}	1.5 to 4.0	
26	V_P	V_P	
27	$V_{i\ SIF1}$	3.4	
28	$V_{i\ SIF2}$	3.4	

TEST AND APPLICATION INFORMATION

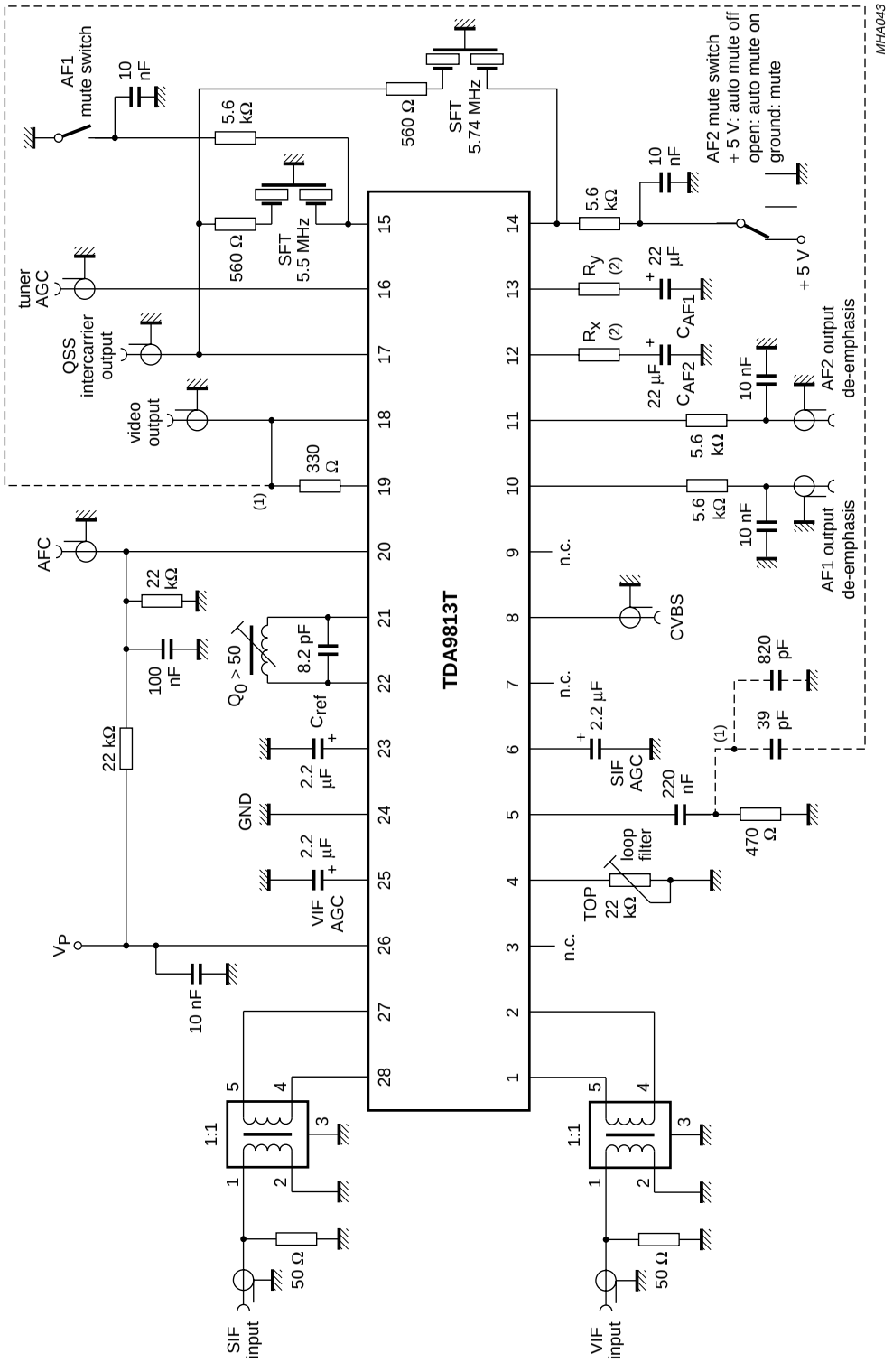


Fig.11 Test circuit.

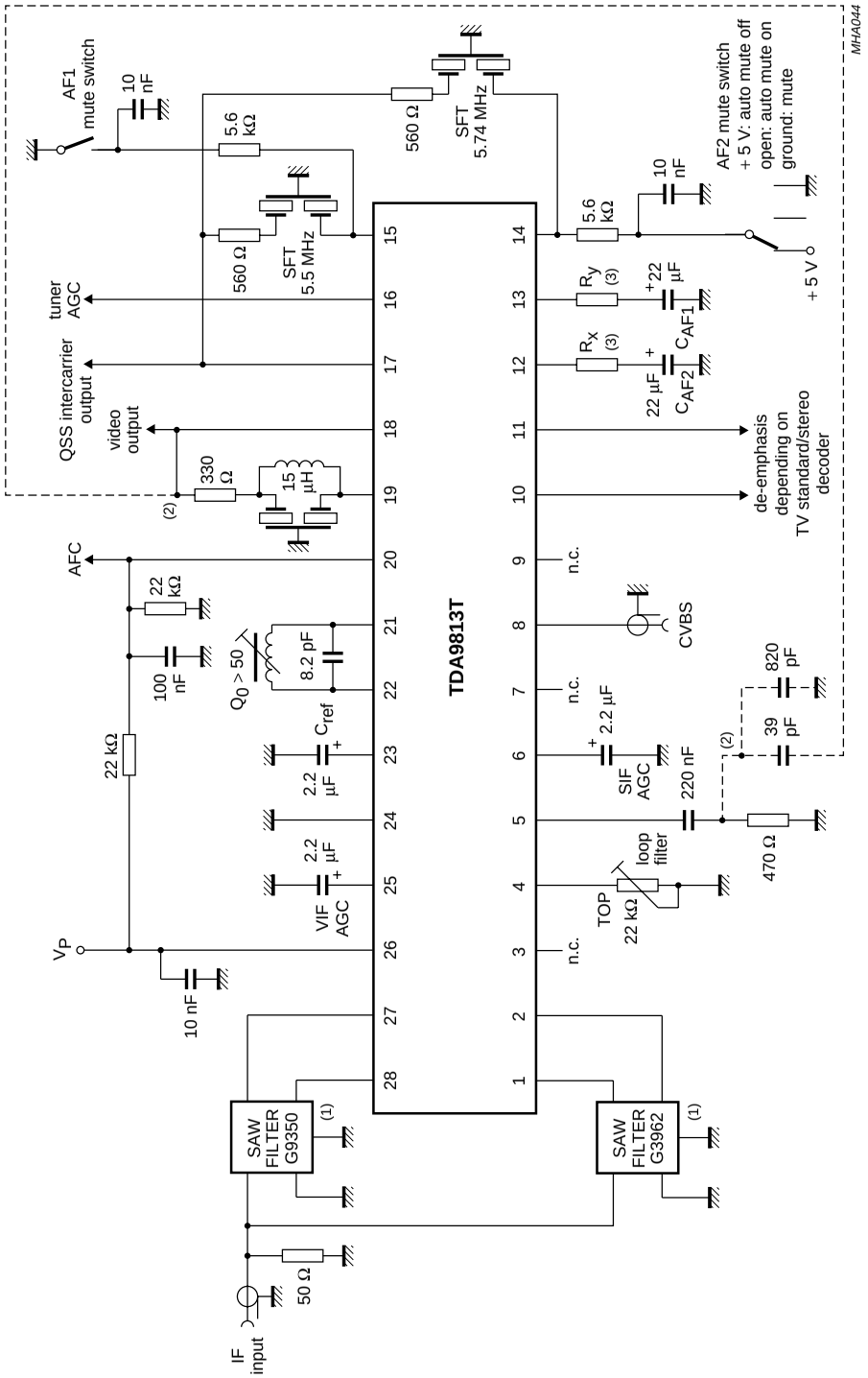
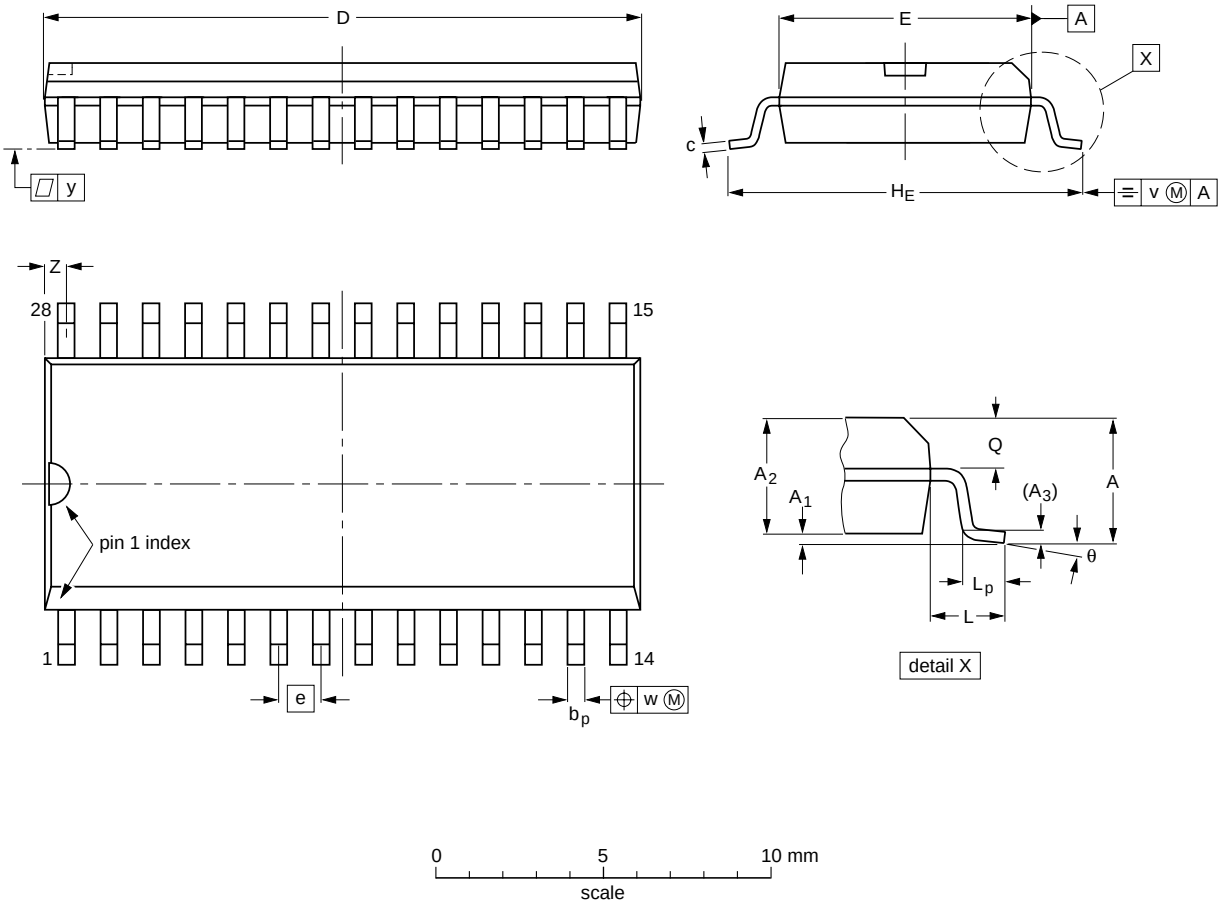


Fig.12 Application circuit.

(1) Depends on standard.
(2) Application for improved 250 kHz sound performance.
(3) See note 17 of Chapter "Characteristics".

PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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