

DATA SHEET

TDA8762

**10-bit high-speed low-power
analog-to-digital converter**

Product specification
Supersedes data of 1995 Feb 15
File under Integrated Circuits, IC02

1996 Mar 28

10-bit high-speed low-power analog-to-digital converter

TDA8762

FEATURES

- 10-bit resolution
- Sampling rate up to 40 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.4 effective bits at 4.43 MHz full-scale input at $f_{\text{clk}} = 40$ MHz)
- No missing codes guaranteed
- In range (IR) TTL output
- TTL compatible digital inputs and outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 380 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- $\Sigma\Delta$ modulators
- Medical imaging.

GENERAL DESCRIPTION

The TDA8762 is a 10-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
I_{CCA}	analog supply current		–	29	36	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output stages supply current		–	23	30	mA
INL	integral non-linearity	$f_{\text{clk}} = 40$ MHz; ramp input	–	± 0.75	± 1.5	LSB
DNL	differential non-linearity	$f_{\text{clk}} = 40$ MHz; ramp input	–	± 0.3	± 0.7	LSB
$f_{\text{clk(max)}}$	maximum clock frequency		40	–	–	MHz
P_{tot}	total power dissipation		–	380	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8762M/4	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	40

10-bit high-speed low-power analog-to-digital converter

TDA8762

BLOCK DIAGRAM

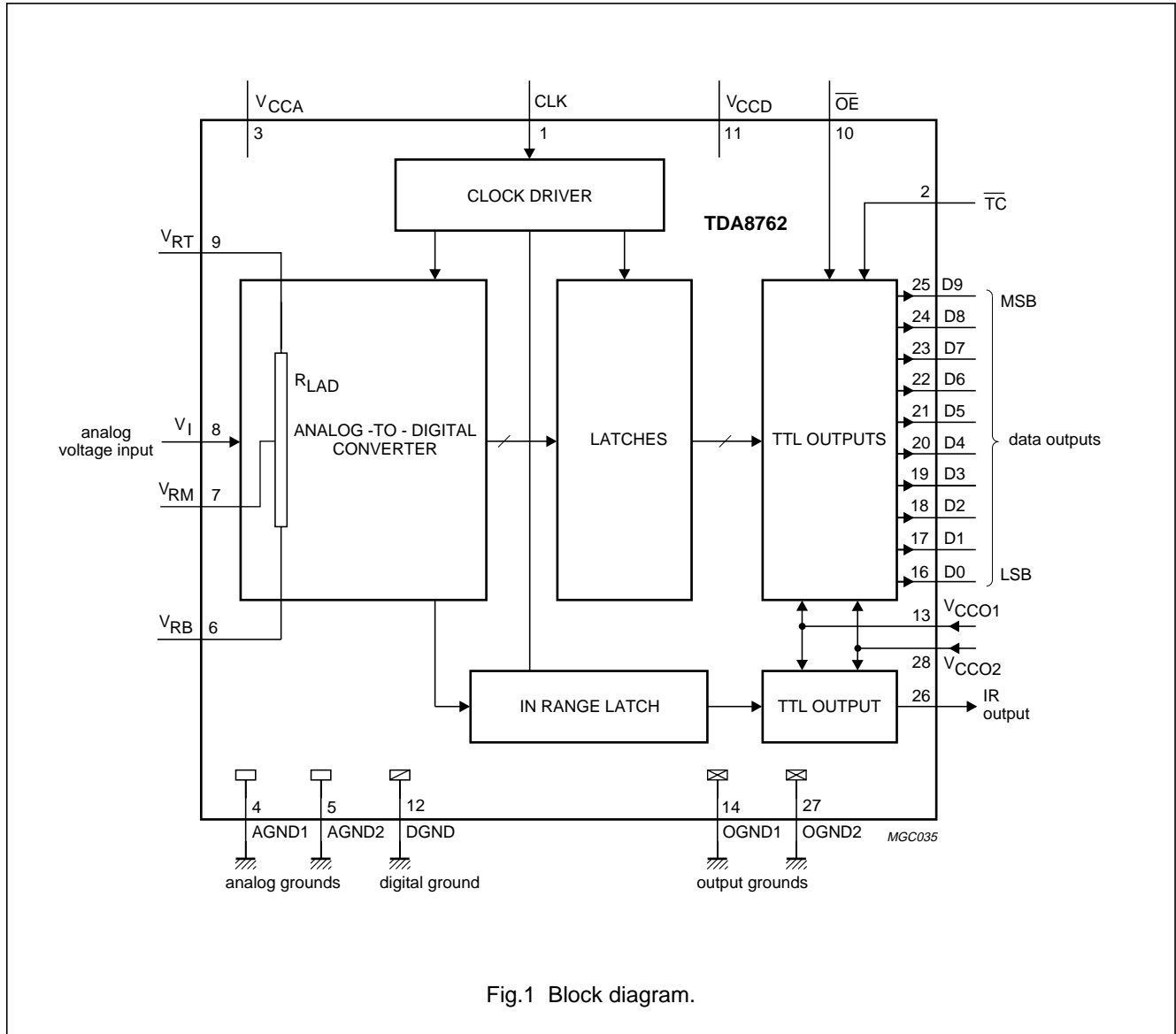


Fig.1 Block diagram.

10-bit high-speed low-power analog-to-digital converter

TDA8762

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
\overline{TC}	2	two's complement input (active LOW)
V _{CCA}	3	analog supply voltage (+5 V)
AGND1	4	analog ground 1
AGND2	5	analog ground 2
V _{RB}	6	reference voltage BOTTOM input
V _{RM}	7	reference voltage MIDDLE
V _I	8	analog input voltage
V _{RT}	9	reference voltage TOP input
\overline{OE}	10	output enable input (TTL level input, active LOW)
V _{CCD}	11	digital supply voltage (+5 V)
DGND	12	digital ground
V _{CCO1}	13	supply voltage for output stages 1 (+5 V)
OGND1	14	output ground 1
n.c.	15	not connected
D0	16	data output; bit 0 (LSB)
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (MSB)
IR	26	in range data output
OGND2	27	output ground 2
V _{CCO2}	28	supply voltage for output stages 2 (+5 V)

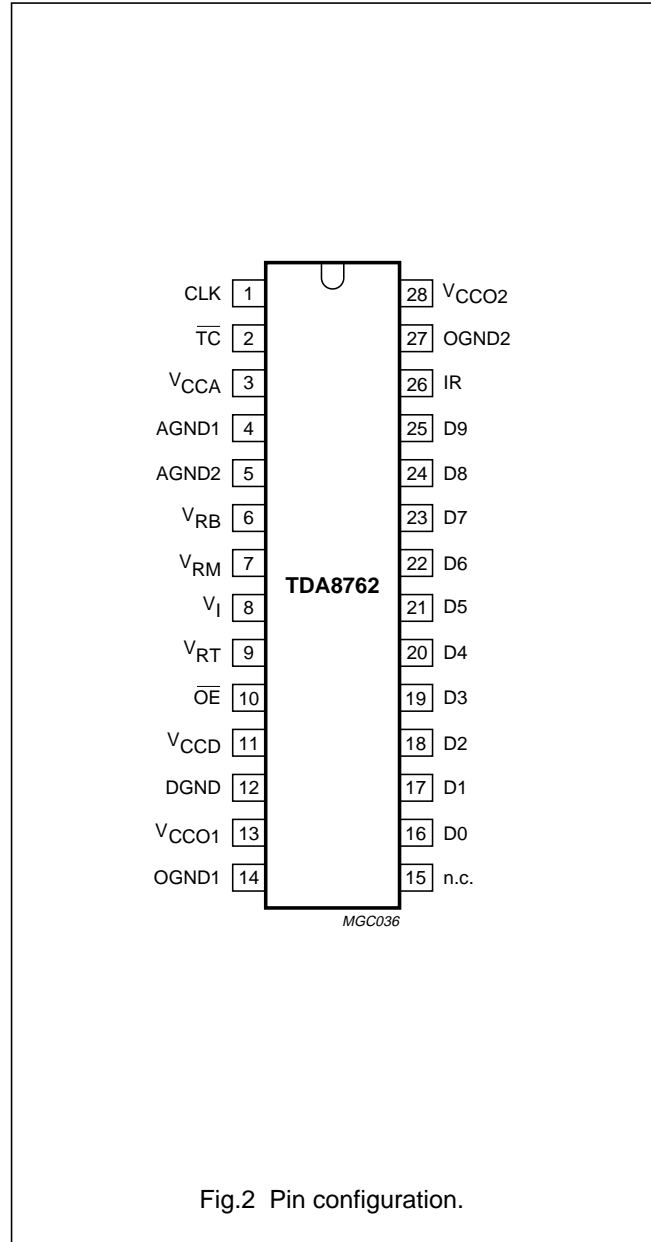


Fig.2 Pin configuration.

10-bit high-speed low-power analog-to-digital converter

TDA8762

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	-0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	-0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	-0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	$V_{CCA} - V_{CCD}$		-1.0	+1.0	V
	$V_{CCA} - V_{CCO}$		-1.0	+1.0	V
	$V_{CCD} - V_{CCO}$		-1.0	+1.0	V
V_I	input voltage	referenced to AGND	-0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	-	V_{CCD}	V
I_O	output current		-	10	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		-	+150	°C

Note

- The supply voltages V_{CCA} , V_{CCD} and V_{CCO} may have any value between -0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	110	K/W

10-bit high-speed low-power analog-to-digital converter

TDA8762

CHARACTERISTICS

$V_{CCA} = V_3$ to V_4 and $V_5 = 4.75$ to 5.25 V; $V_{CCD} = V_{11}$ to $V_{12} = 4.75$ to 5.25 V; $V_{CCO} = V_{13}$ and V_{28} to V_{14} and $V_{27} = 4.4$ to 5.25 V; AGND and DGND shorted together; $T_{amb} = 0$ to $+70$ °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $V_{I(p-p)} = 2.0$ V; $C_L = 15$ pF and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
ΔV_{CC}	voltage difference					
	$V_{CCA} - V_{CCD}$		-0.25	-	+0.25	V
	$V_{CCA} - V_{CCO}$		-0.4	-	+0.4	V
	$V_{CCD} - V_{CCO}$		-0.4	-	+0.4	V
I_{CCA}	analog supply current		-	29	36	mA
I_{CCD}	digital supply current		-	24	30	mA
I_{CCO}	output stages supply current	$C_L = 15$ pF; ramp input	-	23	30	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	V_{CCD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.4$ V	-1	0	+1	μ A
I_{IH}	HIGH level input current	$V_{clk} = 2.7$ V	-	-	20	μ A
Z_I	input impedance	$f_{clk} = 40$ MHz	-	2	-	k Ω
C_I	input capacitance	$f_{clk} = 40$ MHz	-	2	-	pF
INPUTS \overline{OE} AND \overline{TC} (REFERENCED TO DGND); see Table 2						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	-400	-	-	μ A
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	-	-	20	μ A
V_I (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW level input current	$V_I = 1.3$ V	-	0	-	μ A
I_{IH}	HIGH level input current	$V_I = 3.8$ V	-	70	-	μ A
Z_I	input impedance	$f_i = 4.43$ MHz	-	5	-	k Ω
C_I	input capacitance	$f_i = 4.43$ MHz	-	8	-	pF

10-bit high-speed low-power analog-to-digital converter

TDA8762

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.2	1.3	–	V
V_{RT}	reference voltage TOP		–	3.8	$V_{CCA} - 0.8$ V	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.8	2.5	3.0	V
I_{ref}	reference current		–	28	–	mA
R_{LAD}	resistor ladder		–	90	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1860	–	ppm
			–	167	–	m Ω /K
V_{osB}	offset voltage BOTTOM	note 2	–	220	–	mV
V_{osT}	offset voltage TOP	note 2	–	220	–	mV
$V_{I(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.5	2.06	2.5	V
Outputs						
DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW level output voltage	$I_O = 1$ mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 0$ mA	2.7	–	$V_{CCO} - 0.5$	V
		$I_O = -0.4$ mA	2.7	–	$V_{CCO} - 1.3$	V
		$I_O = -1$ mA	2.4	–	$V_{CCO} - 1.4$	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCO}	–20	–	+20	μ A
Switching characteristics						
CLOCK INPUT CLK; see Fig.4; note 1						
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
t_{CPH}	clock pulse width HIGH		8	–	–	ns
t_{CPL}	clock pulse width LOW		8	–	–	ns
Analog signal processing						
LINEARITY						
INL	integral non-linearity	$f_{clk} = 40$ MHz; ramp input	–	± 0.75	± 1.5	LSB
DNL	differential non-linearity	$f_{clk} = 40$ MHz; ramp input	–	± 0.3	± 0.7	LSB
OFER	offset error	middle code; $V_{RB} = 1.3$ V; $V_{RT} = 3.8$ V	–	± 1	–	LSB
GER	gain error (from device to device)	$V_{RB} = 1.3$ V; $V_{RT} = 3.8$ V; note 4	–	± 0.1	–	%

10-bit high-speed low-power analog-to-digital converter

TDA8762

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH ($f_{\text{clk}} = 40 \text{ MHz}$)						
B	analog bandwidth	full-scale sine wave; note 5	–	40	–	MHz
		75% full-scale sine wave; note 5	–	55	–	MHz
		small signal at mid-scale; $V_1 = \pm 10 \text{ LSB}$ at code 512; note 5	–	700	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.6; note 6	–	2.0	3	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.6; note 6	–	2.5	3.5	ns
HARMONICS ($f_{\text{clk}} = 40 \text{ MHz}$)						
h_1	fundamental harmonics (full scale)	$f_i = 4.43 \text{ MHz}$	–	–	0	dB
h_{all}	harmonics (full scale); all components second harmonics third harmonics	$f_i = 4.43 \text{ MHz}$	–	–70	–62	dB
			–	–75	–67	dB
THD	total harmonic distortion	$f_i = 4.43 \text{ MHz}$	–	–70	–	dB
SIGNAL-TO-NOISE RATIO; see Fig.8; note 7						
S/N	signal-to-noise ratio (full scale)	without harmonics; $f_{\text{clk}} = 40 \text{ MHz}$; $f_i = 4.43 \text{ MHz}$	57	59	–	dB
EFFECTIVE BITS; see Figs 7, 8 and 9; note 7						
EB	effective bits	$f_{\text{clk}} = 40 \text{ MHz}$	–	–	–	–
		$f_i = 4.43 \text{ MHz}$	–	9.4	–	bits
		$f_i = 7.5 \text{ MHz}$	–	9.3	–	bits
		$f_i = 10 \text{ MHz}$	–	9.0	–	bits
		$f_i = 15 \text{ MHz}$	–	8.7	–	bits
TWO-TONE; note 8						
TTIR	two-tone intermodulation rejection	$f_{\text{clk}} = 40 \text{ MHz}$	–	–70	–	dB
BIT ERROR RATE						
BER	bit error rate	$f_{\text{clk}} = 40 \text{ MHz}$; $f_i = 4.43 \text{ MHz}$; $V_1 = \pm 16 \text{ LSB}$ at code 512	–	10^{-13}	–	times/ sample

10-bit high-speed low-power analog-to-digital converter

TDA8762

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIFFERENTIAL GAIN; note 9						
G _{diff}	differential gain	f _{clk} = 40 MHz; PAL modulated ramp	–	0.5	–	%
DIFFERENTIAL PHASE; note 9						
φ _{diff}	differential phase	f _{clk} = 40 MHz; PAL modulated ramp	–	0.5	–	deg
Timing (f_{clk} = 40 MHz; C_L = 15 pF); see Fig.4; note 10						
t _{ds}	sampling delay time		–	–	2	ns
t _h	output hold time		5	–	–	ns
t _d	output delay time		–	10	14	ns
C _L	digital output load		–	15	40	pF
3-state output delay times; see Fig.5						
t _{dZH}	enable HIGH		–	45	50	ns
t _{dZL}	enable LOW		–	25	35	ns
t _{dHZ}	disable HIGH		–	12	15	ns
t _{dLZ}	disable LOW		–	12	15	ns

Notes

- In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.
- Analog input voltages producing code 0 up to and including code 1023:
 - V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
 - V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to code 1023 at T_{amb} = 25 °C.
- In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 1023 respectively) are connected to pins V_{RB} and V_{RT} via offset resistors R_{OB} and R_{OT} as shown in Fig.3.

a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter,

to cover code 0 to code 1023, is $.V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.824 \times (V_{RT} - V_{RB})$.

b) Since R_L, R_{OB} and R_{OT} have similar behaviour with respect to process and temperature variation, the ratio

$\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from part to part. Consequently variation of the output codes

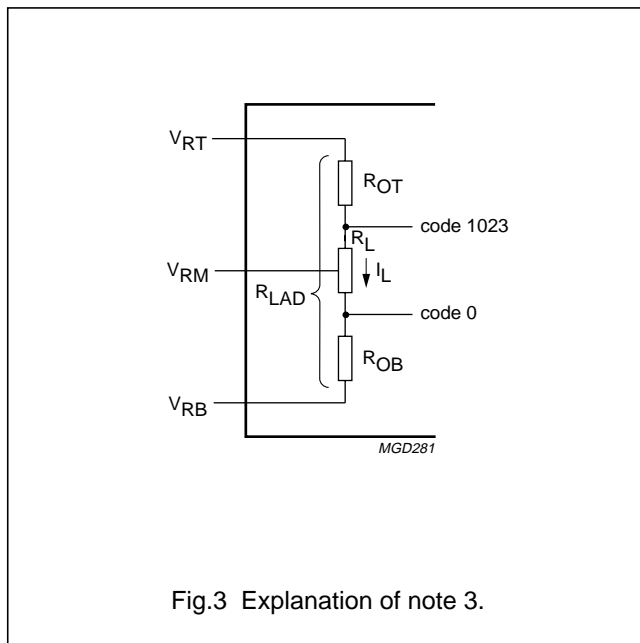
at a given input voltage depends mainly on the difference V_{RT} – V_{RB} and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.

4. $GER = \frac{(V_{1023} - V_0) - 2 V}{2 V} \times 100$.

10-bit high-speed low-power analog-to-digital converter

TDA8762

5. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
6. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
7. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: $S/N = EB \times 6.02 + 1.76$ dB.
8. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
9. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
10. Output data acquisition: the output data is available after the maximum delay time of t_d .



10-bit high-speed low-power analog-to-digital converter

TDA8762

Table 1 Output coding and input voltage (typical values; referenced to AGND, $V_{RB} = 1.3\text{ V}$, $V_{RT} = 3.8\text{ V}$)

STEP	$V_{I(p-p)}$	IR	BINARY OUTPUT BITS										TWO'S COMPLEMENT OUTPUT BITS										
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
U/F	<1.52	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1.52	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1
.
.
1022	.	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0	
1023	3.58	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	
O/F	>3.58	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	

Table 2 Mode selection

\overline{TC}	\overline{OE}	D9 TO D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

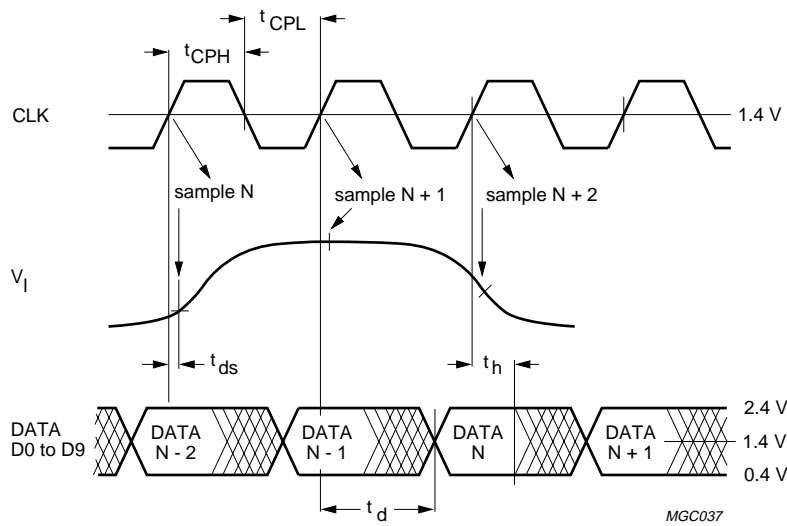
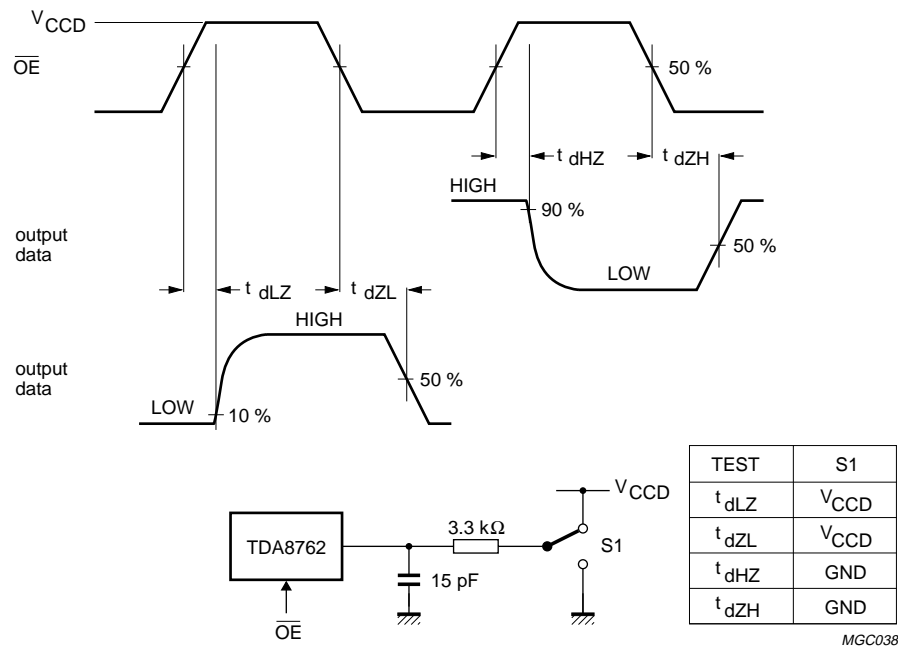


Fig.4 Timing diagram.

10-bit high-speed low-power analog-to-digital converter

TDA8762



$f_{OE} = 100 \text{ kHz}$.

Fig.5 Timing diagram and test conditions of 3-state output delay time.

10-bit high-speed low-power
analog-to-digital converter

TDA8762

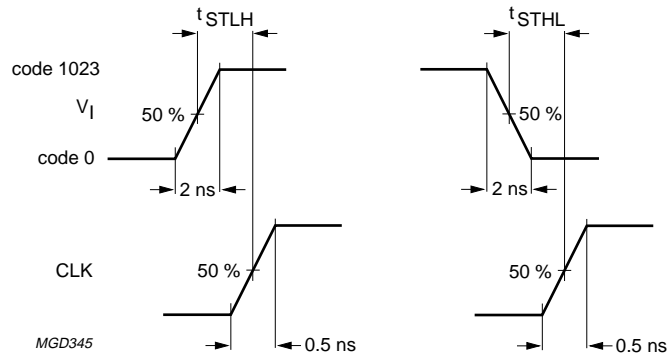
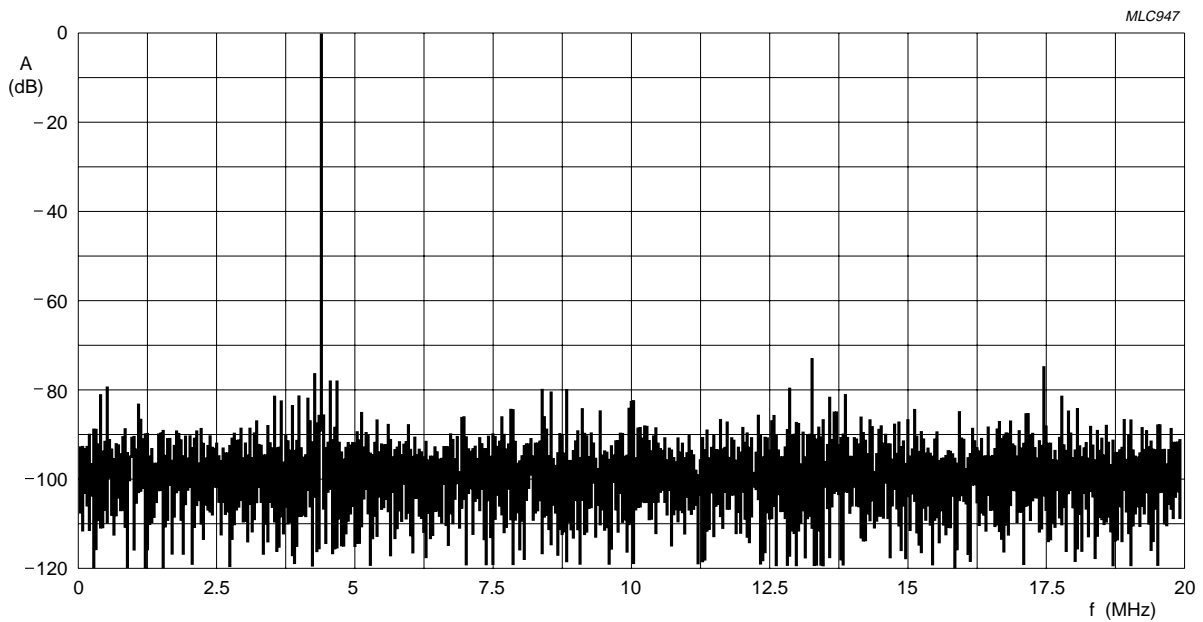


Fig.6 Analog input settling-time diagram.

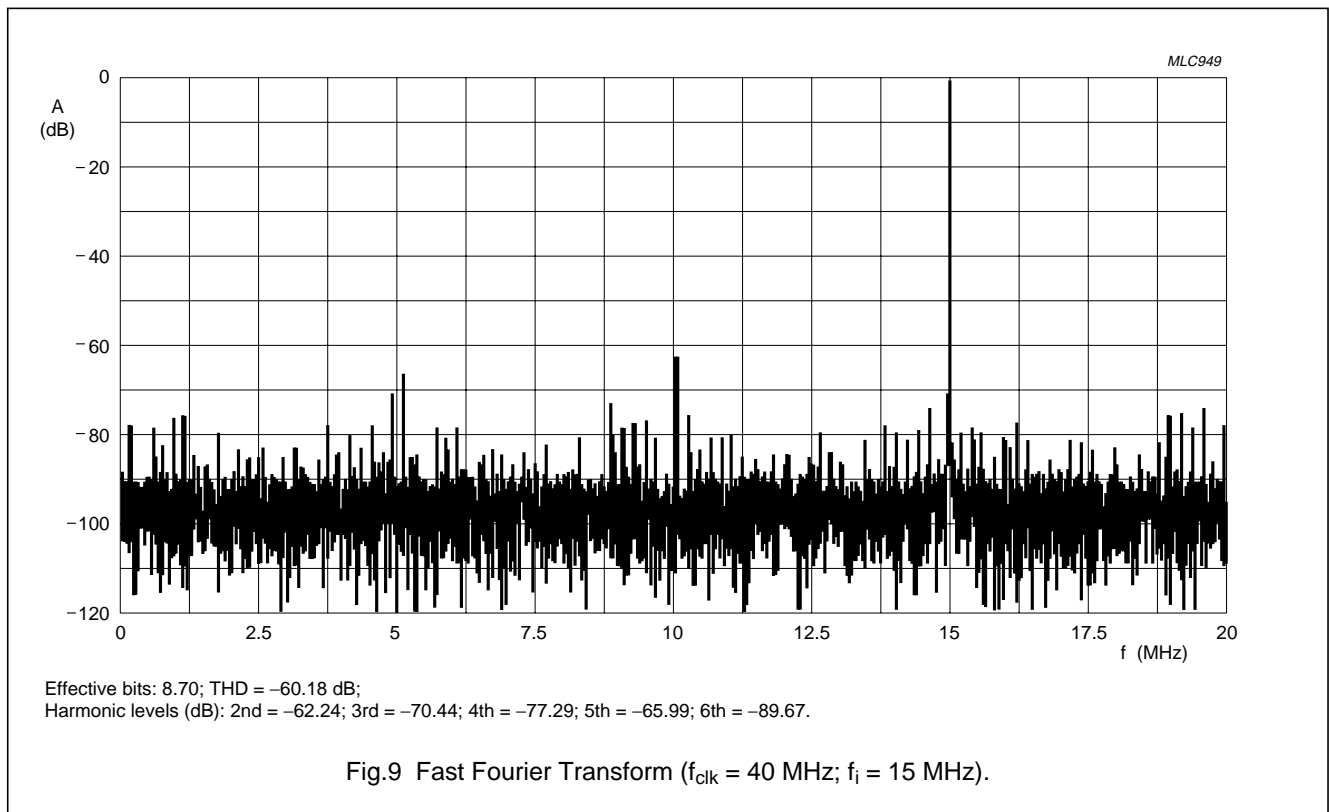
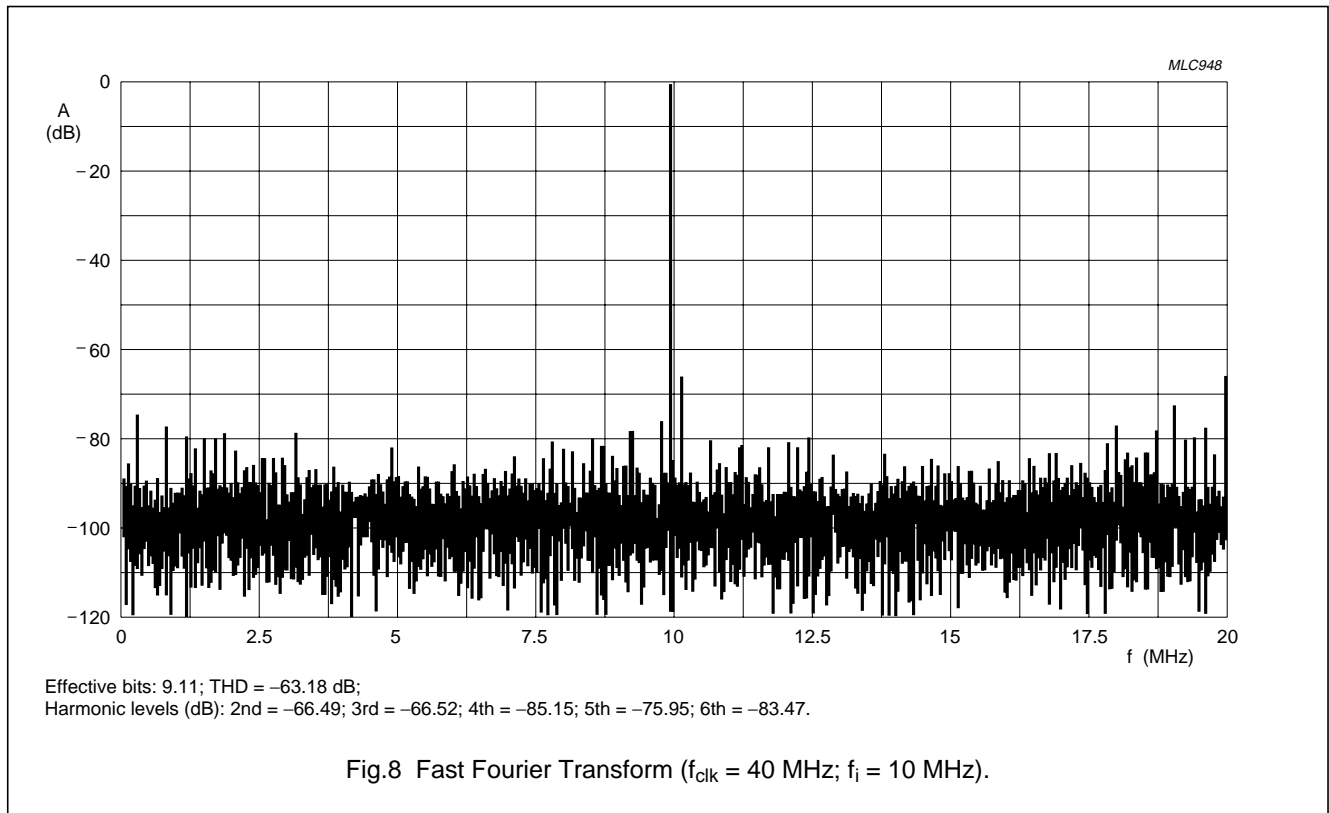


Effective bits: 9.46; THD = -71.19 dB;
Harmonic levels (dB): 2nd = -79.70; 3rd = -72.84; 4th = -81.54; 5th = -83.93; 6th = -86.47.

Fig.7 Fast Fourier Transform ($f_{clk} = 40$ MHz; $f_i = 4.43$ MHz).

10-bit high-speed low-power
analog-to-digital converter

TDA8762



10-bit high-speed low-power analog-to-digital converter

TDA8762

INTERNAL PIN CONFIGURATIONS

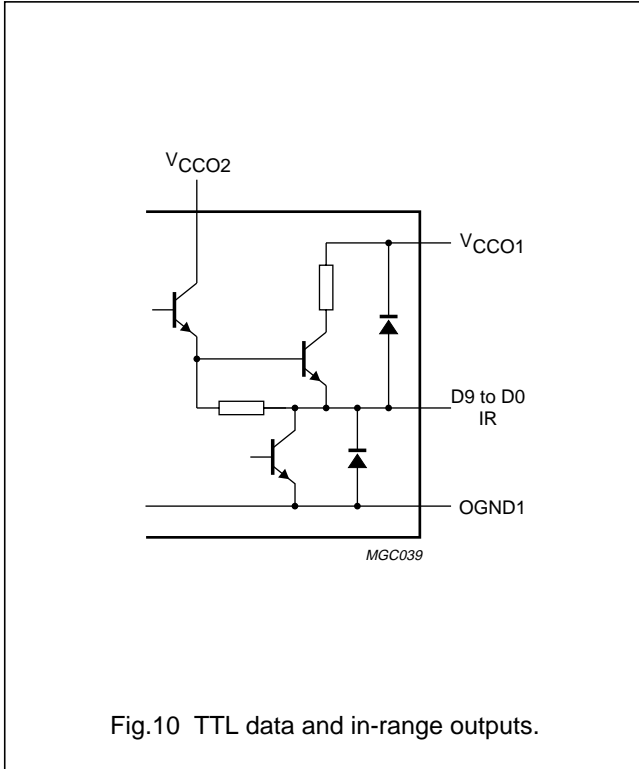


Fig.10 TTL data and in-range outputs.

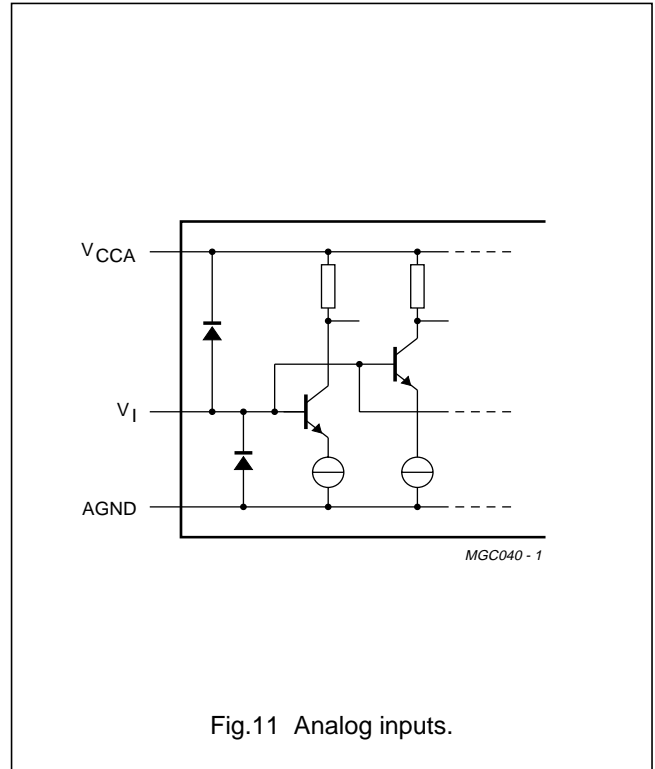


Fig.11 Analog inputs.

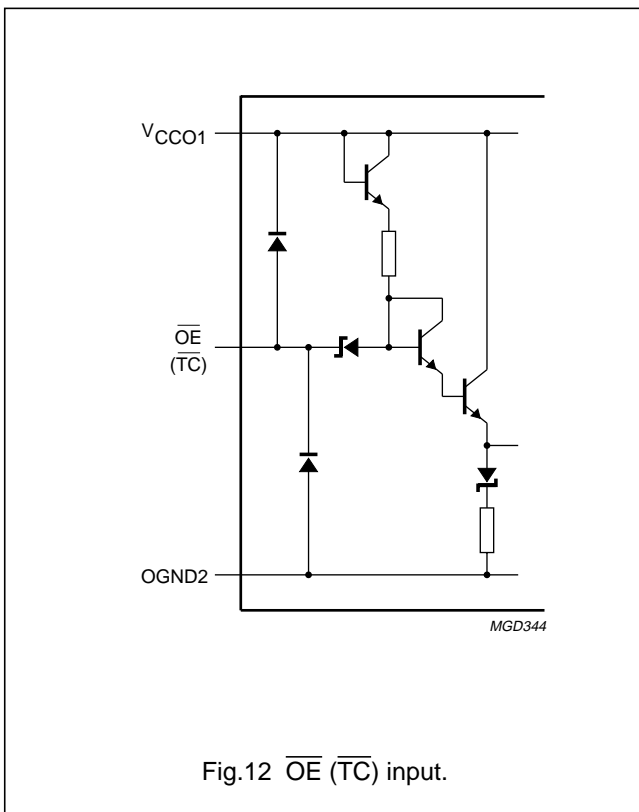


Fig.12 \overline{OE} (\overline{TC}) input.

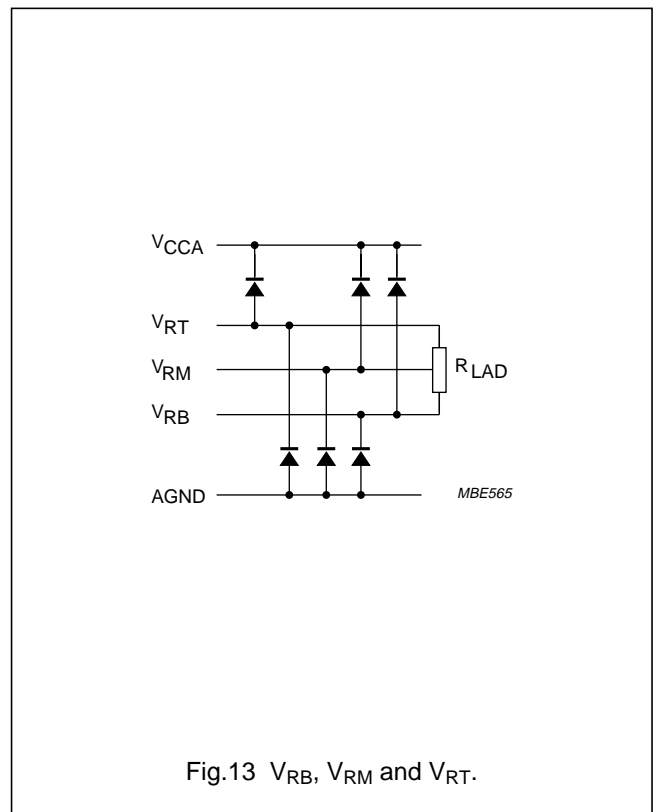


Fig.13 V_{RB} , V_{RM} and V_{RT} .

10-bit high-speed low-power
analog-to-digital converter

TDA8762

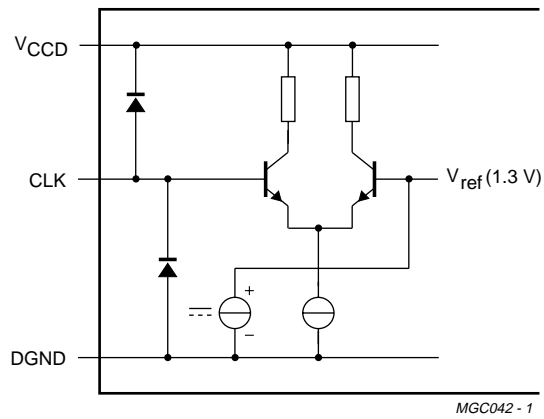


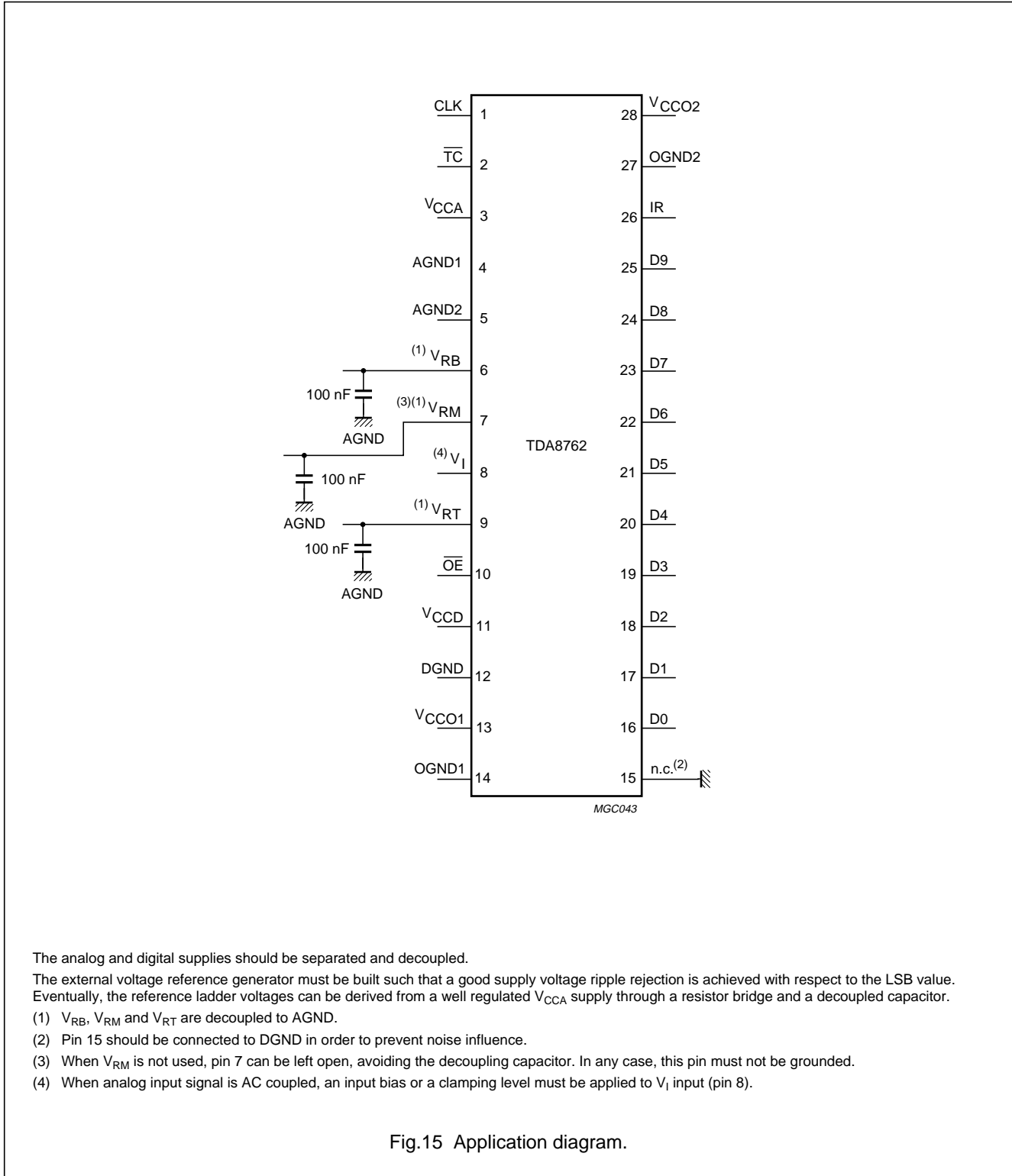
Fig.14 CLK input.

10-bit high-speed low-power analog-to-digital converter

TDA8762

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number "AN96025").



The analog and digital supplies should be separated and decoupled.

The external voltage reference generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{CCA} supply through a resistor bridge and a decoupled capacitor.

- (1) V_{RB}, V_{RM} and V_{RT} are decoupled to AGND.
- (2) Pin 15 should be connected to DGND in order to prevent noise influence.
- (3) When V_{RM} is not used, pin 7 can be left open, avoiding the decoupling capacitor. In any case, this pin must not be grounded.
- (4) When analog input signal is AC coupled, an input bias or a clamping level must be applied to V_I input (pin 8).

Fig.15 Application diagram.

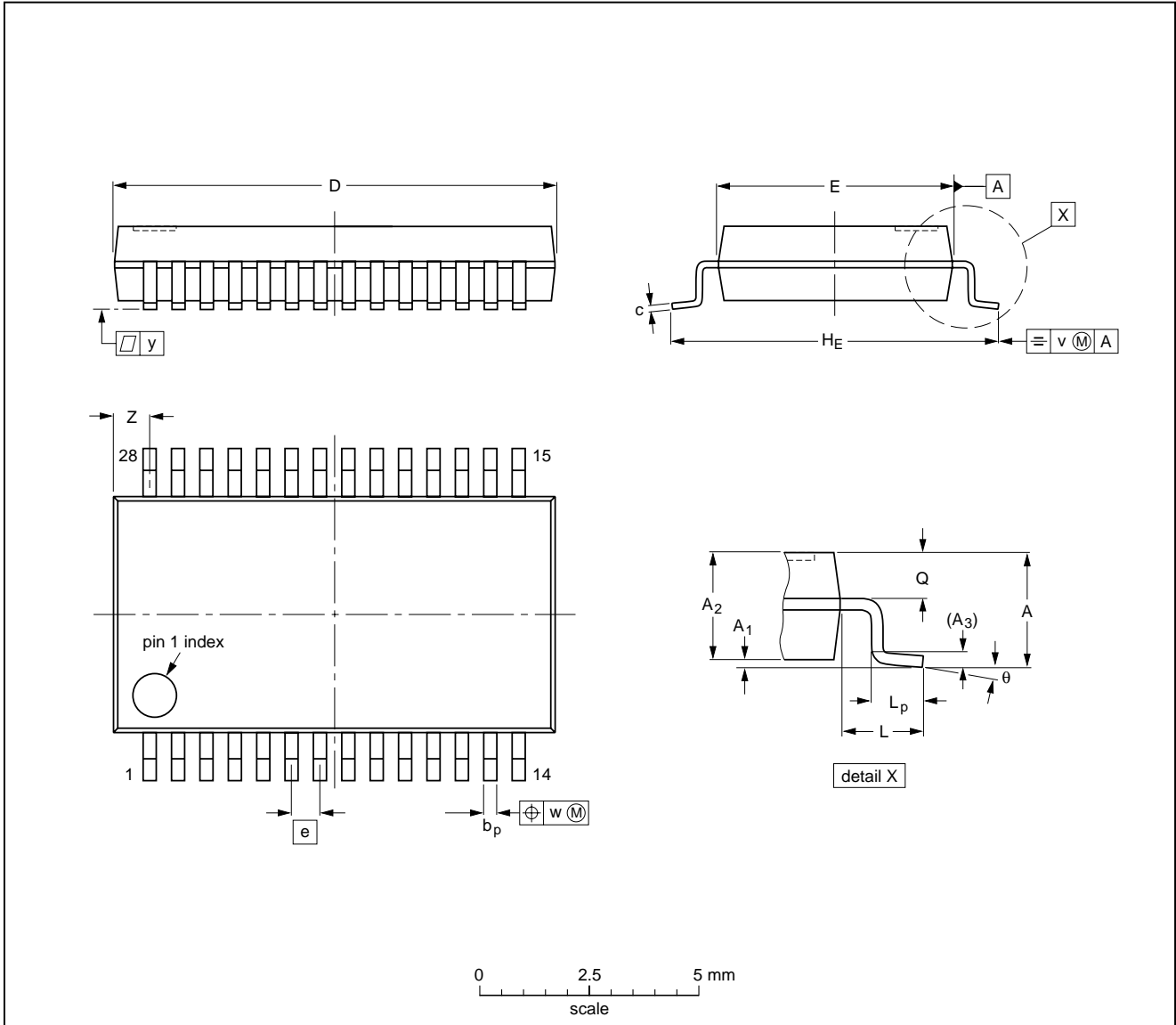
10-bit high-speed low-power analog-to-digital converter

TDA8762

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm

SOT341-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				93-09-08 95-02-04

10-bit high-speed low-power analog-to-digital converter

TDA8762

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

10-bit high-speed low-power analog-to-digital converter

TDA8762

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

10-bit high-speed low-power
analog-to-digital converter

TDA8762

NOTES

10-bit high-speed low-power
analog-to-digital converter

TDA8762

NOTES

10-bit high-speed low-power
analog-to-digital converter

TDA8762

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. (02) 805 4455, Fax. (02) 805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. (01) 60 101-1256, Fax. (01) 60 101-1250

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211,
Volodarski Str. 6, 220050 MINSK,
Tel. (172) 200 733, Fax. (172) 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. (359) 2 689 211, Fax. (359) 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS:
Tel. (800) 234-7381, Fax. (708) 296-8556

Chile: see South America

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. (852) 2319 7888, Fax. (852) 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300
COPENHAGEN S, Tel. (032) 88 2636, Fax. (031) 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. (358) 0-615 800, Fax. (358) 0-61580 920

France: 4 Rue du Port-aux-Vins, BP317,
92156 SURESNES Cedex,
Tel. (01) 4099 6161, Fax. (01) 4099 6427

Germany: P.O. Box 10 51 40, 20035 HAMBURG,
Tel. (040) 23 53 60, Fax. (040) 23 53 63 00

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. (01) 4894 339/4894 911, Fax. (01) 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block,
Dr. Annie Besant Rd. Worli, BOMBAY 400 018
Tel. (022) 4938 541, Fax. (022) 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. (01) 7640 000, Fax. (01) 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. (03) 645 04 44, Fax. (03) 648 10 07

Italy: PHILIPS SEMICONDUCTORS,
Piazza IV Novembre 3, 20124 MILANO,
Tel. (0039) 2 6752 2531, Fax. (0039) 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108, Tel. (03) 3740 5130, Fax. (03) 3740 5077

Korea: Philips House, 260-199 Itaewon-dong,
Yongsan-ku, SEOUL, Tel. (02) 709-1412, Fax. (02) 709-1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA,
SELANGOR, Tel. (03) 750 5214, Fax. (03) 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO,
TEXAS 79905, Tel. 9-5(800) 234-7831, Fax. (708) 296-8556

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. (040) 2783749, Fax. (040) 2788399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. (09) 849-4160, Fax. (09) 849-7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. (022) 74 8000, Fax. (022) 74 8341

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC,
MAKATI, Metro MANILA,
Tel. (63) 2 816 6380, Fax. (63) 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. (022) 612 2831, Fax. (022) 612 2327

Portugal: see Spain

Romania: see Italy

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. (65) 350 2000, Fax. (65) 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd.,
195-215 Main Road Martindale, 2092 JOHANNESBURG,
P.O. Box 7430 Johannesburg 2000,
Tel. (011) 470-5911, Fax. (011) 470-5494

South America: Rua do Rocio 220 - 5th floor, Suite 51,
CEP: 04552-903-SÃO PAULO-SP, Brazil,
P.O. Box 7383 (01064-970),
Tel. (011) 821-2333, Fax. (011) 829-1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. (03) 301 6312, Fax. (03) 301 4107

Sweden: Kottbygatan 7, Akalla. S-16485 STOCKHOLM,
Tel. (0) 8-632 2000, Fax. (0) 8-632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. (01) 488 2211, Fax. (01) 481 77 30

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. (886) 2 382 4443, Fax. (886) 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. (66) 2 745-4090, Fax. (66) 2 398-0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. (0212) 279 2770, Fax. (0212) 282 6707

Ukraine: PHILIPS UKRAINE,
2A Akademika Koroleva str., Office 165, 252148 KIEV,
Tel. 380-44-4760297, Fax. 380-44-4766991

United Kingdom: Philips Semiconductors LTD.,
276 Bath Road, Hayes, MIDDLESEX UB3 5BX,
Tel. (0181) 730-5000, Fax. (0181) 754-8421

United States: 811 East Arques Avenue, SUNNYVALE,
CA 94088-3409, Tel. (800) 234-7381, Fax. (708) 296-8556

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. (381) 11 825 344, Fax. (359) 211 635 777

Internet: <http://www.semiconductors.philips.com/ps/>

For all other countries apply to: Philips Semiconductors,
Marketing & Sales Communications, Building BE-p,
P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands,
Fax. +31-40-2724825

SCDS48

© Philips Electronics N.V. 1996

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

537021/1100/02/pp24
Document order number:

Date of release: 1996 Mar 28
9397 750 00767