DATA SHEET

TDA8755
YUV 8-bit video low-power analog-to-digital interface

Product specification
Supersedes data of June 1994
File under Integrated Circuits, IC02

1995 Mar 09

Philips Semiconductors

PHILIPS

YUV 8-bit video low-power analog-to-digital interface

TDA8755

FEATURES

- 8-bit resolution
- Sampling rate up to 20 MHz
- TTL compatible digital inputs
- 3-state TTL outputs
- U, V two's complement outputs
- Y binary output
- Power dissipation of 550 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- High signal-to-noise ratio over a large analog input frequency range
- Track-and-hold included
- Clamp functions included
- UV multiplexed ADC
- 4 : 1 : 1 output data encoder
- Stable voltage regulator included.

APPLICATIONS

- High speed analog-to-digital conversion for video signal digitizing
- 100 Hz improved definition TV (IDTV).

GENERAL DESCRIPTION

The TDA8755 is a bipolar 8-bit video low-power analog-to-digital conversion (ADC) interface for YUV signals. The device converts the YUV analog input signal into 8-bit coded digital words in a 4 : 1 : 1 format at a sampling rate of 20 MHz. The U/V signals are converted in a multiplexed manner. All analog signal inputs are digitally clamped and a fast precharge is provided for start-up. All digital inputs and outputs are TTL compatible. Frame synchronization is supported in a multiplexed manner.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	46	55	mA
I_{CCD}	digital supply current		–	55	66	mA
I_{CCO}	output stages supply current		–	9	12	mA
INL	DC integral non-linearity	f_{clk} = 2 MHz	–	±0.4	±1	LSB
DNL	DC differential non-linearity	f_{clk} = 2 MHz	–	±0.3	±0.5	LSB
EB	effective bits		–	7.1	–	bits
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation		–	550	700	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8755T	32	SO32L	plastic	SOT287-1

BLOCK DIAGRAM

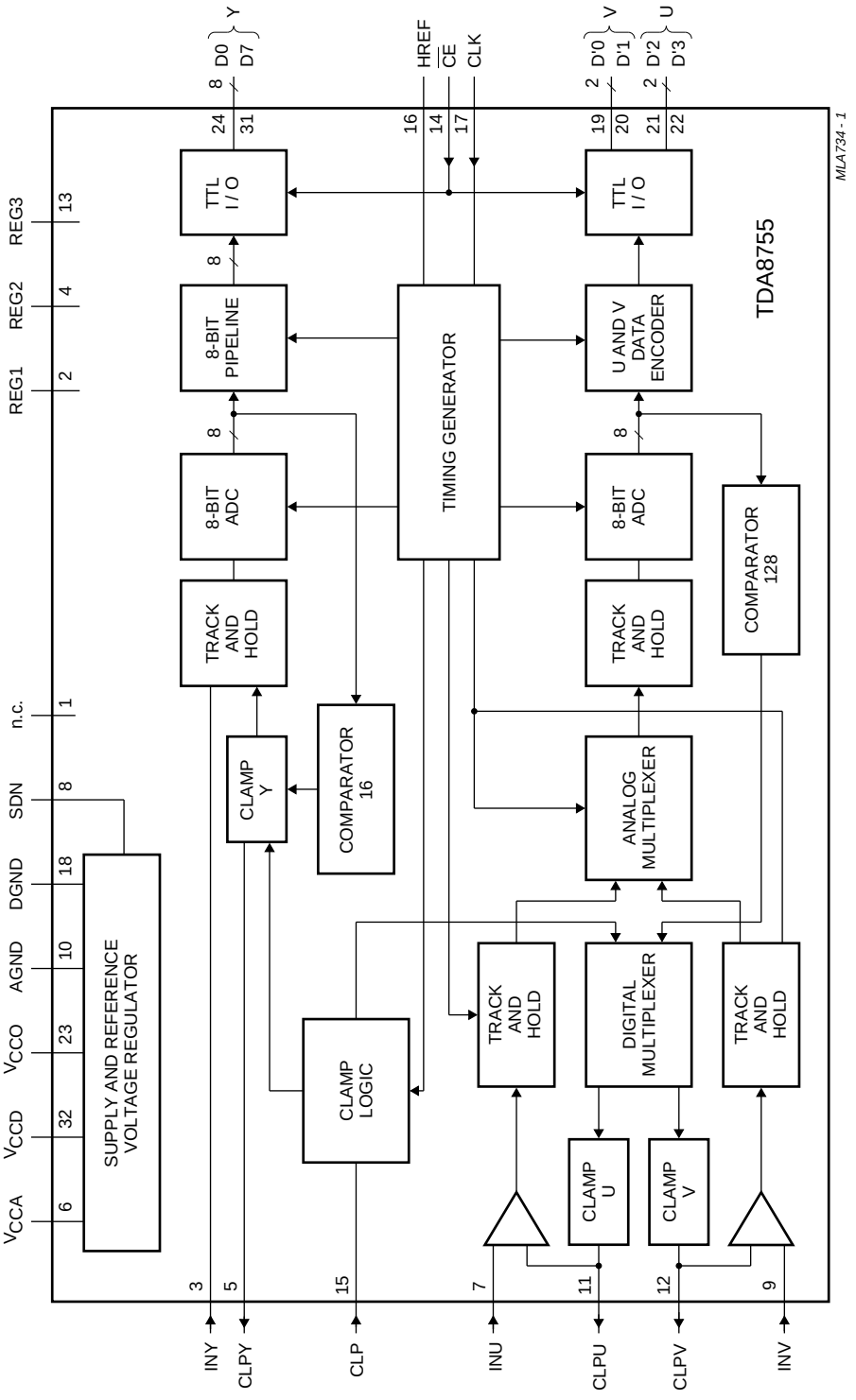


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
REG1	2	decoupling input (internal stabilization loop decoupling)
INY	3	Y analog voltage input
REG2	4	decoupling input (internal stabilization loop decoupling)
CLPY	5	Y clamp capacitor connection
V_{CCA}	6	analog positive supply voltage (+5 V)
INU	7	U analog voltage input
SDN	8	stabilizer decoupling node and analog reference voltage (+3.35 V)
INV	9	V analog voltage input
AGND	10	analog ground
CLPU	11	U clamp capacitor connection
CLPV	12	V clamp capacitor connection
REG3	13	decoupling input (internal stabilization loop decoupling)
$\overline{CE}$	14	chip enable input (TTL level input active LOW)
CLP	15	clamp control input
HREF	16	horizontal reference signal
CLK	17	clock input
DGND	18	digital ground
D'0	19	V data output; bit 0 (n–1)
D'1	20	V data output; bit 1 (n)
D'2	21	U data output; bit 0 (n–1)
D'3	22	U data output; bit 1 (n)
V_{CCO}	23	positive supply voltage for output stages (+5 V)
D0	24	Y data output; bit 0 (LSB)
D1	25	Y data output; bit 1
D2	26	Y data output; bit 2
D3	27	Y data output; bit 3
D4	28	Y data output; bit 4
D5	29	Y data output; bit 5
D6	30	Y data output; bit 6
D7	31	Y data output; bit 7 (MSB)
V_{CCD}	32	digital positive supply voltage (+5 V)

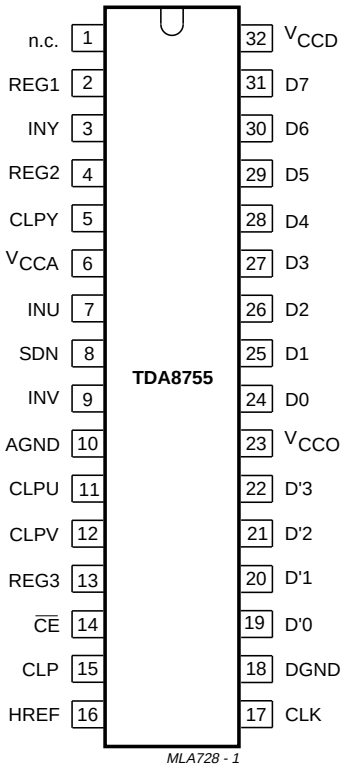


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		–0.3	+7.0	V
V_{CCD}	digital supply voltage		–0.3	+7.0	V
V_{CCO}	output stages supply voltage		–0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}		–1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}		–1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}		–1.0	+1.0	V
V_I	input voltage	referenced to AGND	–	+5.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
I_O	output current		–	+6	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

$V_{CCA} = V_6$ to V_{10} = 4.75 to 5.25 V; $V_{CCD} = V_{32}$ to V_{18} = 4.75 to 5.25 V; $V_{CCO} = V_{23}$ to V_{18} = 4.75 to 5.25 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = –0.25 to +0.25 V; V_{CCO} to V_{CCD} = –0.25 to +0.25 V; V_{CCA} to V_{CCO} = –0.25 to +0.25 V; T_{amb} = 0 to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	46	55	mA
I_{CCD}	digital supply current		–	55	66	mA
I_{CCO}	output stages supply current		–	9	12	mA
Inputs						
CLK (PIN 17)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	µA
Z_I	input impedance	f_{clk} = 20 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 20 MHz	–	4.5	–	pF
$\overline{CE}$, CLP AND HREF (PINS 14 TO 16)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	µA
CLPY (PIN 5)						
V_5	clamp voltage for 16 output code		–	3.725	–	V
I_5	clamp output current		–	±50	–	µA
CLPU AND CLPV (PINS 11 AND 12)						
$V_{11, 12}$	clamp voltage for 128 output code		–	3.30	–	V
$I_{11, 12}$	clamp output current		–	±50	–	µA
INY (PIN 3)						
$V_{I(p-p)}$	input voltage, full range (peak-to-peak value)	f_i = 4.43 MHz	0.93	1.0	1.07	V
Z_I	input impedance	f_i = 6 MHz	–	30	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INU AND INV (PINS 7 AND 9)						
$V_{I(p-p)}$	input voltage, full range (peak-to-peak value)	f_i = 1.5 MHz	0.93	1.03	1.13	V
Z_I	input impedance	f_i = 2 MHz	–	30	–	kΩ
C_I	input capacitance	f_i = 2 MHz	–	1	–	pF
INPUTS ISOLATION						
α_{ct}	crosstalk between Y, U and V		–	–55	–50	dB
Outputs						
SDN (PIN 8)						
V_{ref}	reference voltage		–	3.32	–	V
V_{REG}	line regulation	4.75 V ≤ V_{CCA} ≤ 5.25 V	–	4.0	–	mV
I_L	load current		–2	–	–	mA
DIGITAL OUTPUTS D0 TO D7 AND D'0 TO D'3 (PINS 24 TO 31 AND 19 TO 22)						
V_{OL}	LOW level output voltage	I_O = 0.4 mA	0	–	0.4	V
		I_O = 1.5 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
$f_{clk(min)}$	minimum clock frequency		–	–	2.0	MHz
t_{CPH}	clock pulse width HIGH		20	–	–	ns
t_{CPL}	clock pulse width LOW		20	–	–	ns
Analog signal processing (f_{clk} = 20 MHz; 50% clock duty factor)						
G_{diff}	differential gain	note 1; see Fig.8	–	2	–	%
φ_{diff}	differential phase	note 1; see Fig.8	–	3	–	deg
f_1	fundamental harmonics (full-scale)	note 2	–	–	0	dB
f_{all}	harmonics (full-scale), all components	note 2; see Fig.10	–	–54	–	dB
SVRR1	supply voltage ripple rejection 1	note 3	–	–40	–	dB
SVRR2	supply voltage ripple rejection 2	note 3	–	1.0	–	%/V
Transfer function (50% clock duty factor)						
INL	DC integral non-linearity	f_{clk} = 2 MHz	–	±0.4	±1.0	LSB
DNL	DC differential non-linearity	f_{clk} = 2 MHz	–	±0.3	±0.5	LSB
AILE	AC integral non-linearity	note 4	–	±1.0	±2.0	LSB
EB	effective bits	note 5; Fig.10	–	7.1	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{clk} = 20 MHz); note 6; see Figs 3 to 7						
t_{ds}	sampling delay time		–	1	–	ns
t_h	output hold time		7	–	–	ns
t_d	output delay time		–	33	42	ns
t_{dZH}	3-state output delay time	enable-to-HIGH	–	10	14	ns
t_{dZL}	3-state output delay time	enable-to-LOW	–	10	14	ns
t_{dHZ}	3-state output delay time	disable-to-HIGH	–	8	11	ns
t_{dLZ}	3-state output delay time	disable-to-LOW	–	4	6	ns
t_r	clock rise time		3	5	–	ns
t_f	clock fall time		3	5	–	ns
t_{su}	HREF set-up time		7	–	–	ns
t_h	HREF hold time		3	–	–	ns
t_r	data output rise time		–	12	–	ns
t_f	data output fall time		–	16	–	ns
t_{CLP}	minimum time for active clamp	note 7; see Fig.9	3	–	–	µs

Notes

1. Low frequency ramp signal ($V_{I(p-p)}$ = full-scale and 64 µs period) combined with a sinewave input voltage ($V_{I(p-p)}$ = 0.25 full-scale, f_i = maximum permitted frequency) at the input.
2. The input conditions are related as follows:
   a) Y channel: $V_{I(p-p)}$ = 1.0 V; f_i = 4.43 MHz
   b) U/V channel: $V_{I(p-p)}$ = 1.0 V; f_i = 1.5 MHz.
3. Supply voltage ripple rejection:
   a) SVRR1 is the variation of the input voltage producing output code 127 (code 15) for supply voltage variation of 0.5 V:

   $$SVRR1 = 20 \log \frac{\Delta V_{I(127)}}{\Delta V_{CCA}}$$

   b) SVRR2 is the relative variation of the full-scale range of analog input for a supply voltage variation of 0.5 V:

   $$SVVR2 = \frac{\Delta (V_{I(0)} - V_{I(255)})}{V_{I(0)} - V_{I(255)}} \times \frac{1}{\Delta V_{CCA}}$$

4. Full-scale sinewave (f_i = 4.43 MHz for Y and f_i = 1.5 MHz for U and V; f_{clk} = 20 MHz).
5. The number of effective bits is measured using a 20 MHz clock frequency. This value is given for a 4.43 MHz input frequency on the Y channel (1.5 MHz on the U and V channels). This value is obtained via a Fast Fourier Transform (FFT) treatment taking $4 \times T_{clk}$ (clock periods) acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency).

   Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
6. Output data acquisition is available after the maximum delay time of t_d.
7. U and V output data is not valid during t_{CLP}.

Table 1 Mode selection

$\overline{CE}$	D7 TO D0; D'3 TO D'0
1	high impedance
0	active; binary

Table 2 Output data coding

OUTPUT PORT	BIT	OUTPUT DATA			
Y	D7	$Y_0 7$	$Y_1 7$	$Y_2 7$	$Y_3 7$
	D6	$Y_0 6$	$Y_1 6$	$Y_2 6$	$Y_3 6$
	D5	$Y_0 5$	$Y_1 5$	$Y_2 5$	$Y_3 5$
	D4	$Y_0 4$	$Y_1 4$	$Y_2 4$	$Y_3 4$
	D3	$Y_0 3$	$Y_1 3$	$Y_2 3$	$Y_3 3$
	D2	$Y_0 2$	$Y_1 2$	$Y_2 2$	$Y_3 2$
	D1	$Y_0 1$	$Y_1 1$	$Y_2 1$	$Y_3 1$
	D0	$Y_0 0$	$Y_1 0$	$Y_2 0$	$Y_3 0$
U	D'3	$\overline{U}_0 7$	$U_0 5$	$U_0 3$	$U_0 1$
	D'2	$U_0 6$	$U_0 4$	$U_0 2$	$U_0 0$
V	D'1	$\overline{V}_0 7$	$V_0 5$	$V_0 3$	$V_0 1$
	D'0	$V_0 6$	$V_0 4$	$V_0 2$	$V_0 0$

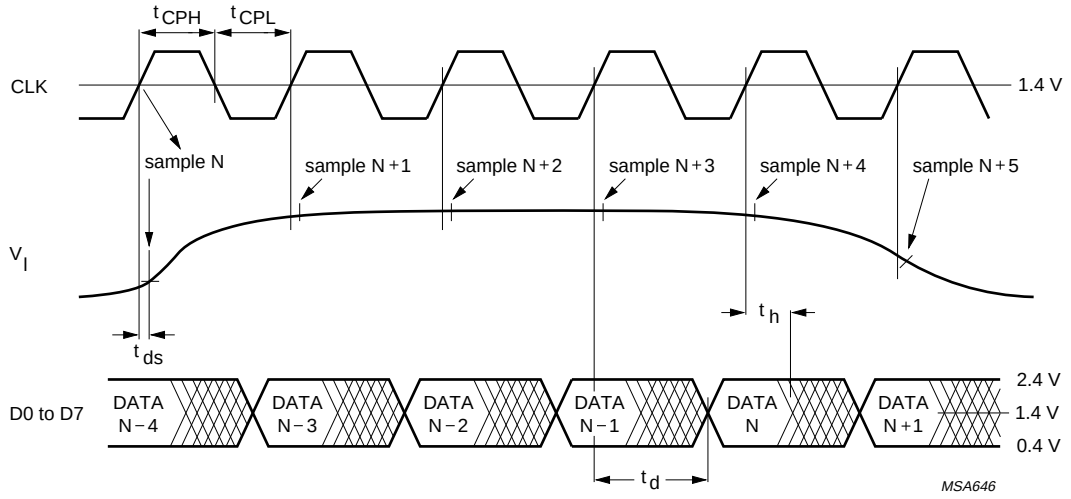
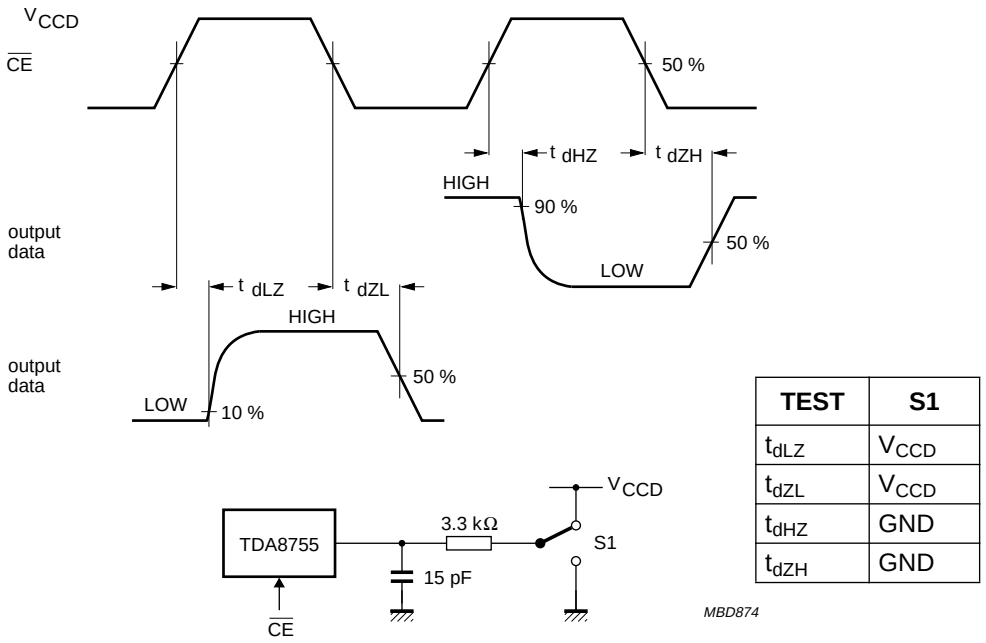


Fig.3 Timing diagram (INY signal).



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{\overline{CE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

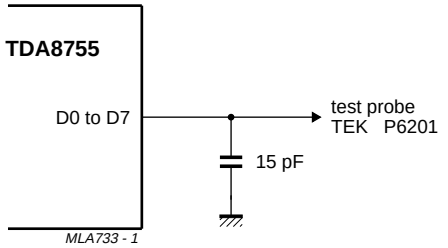
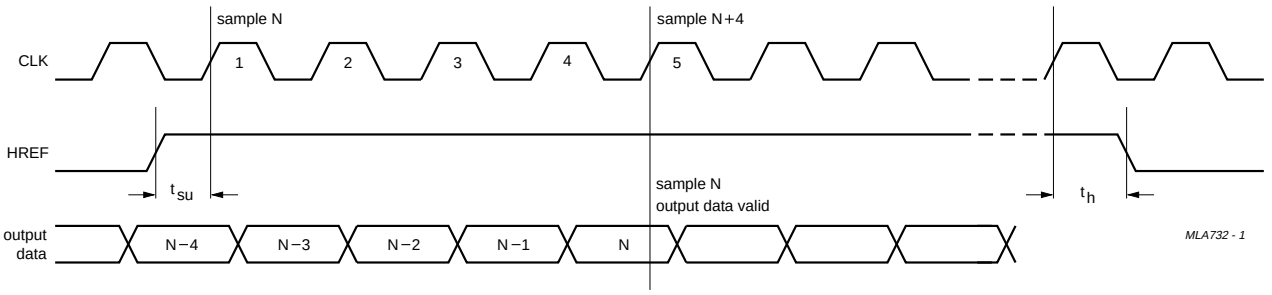
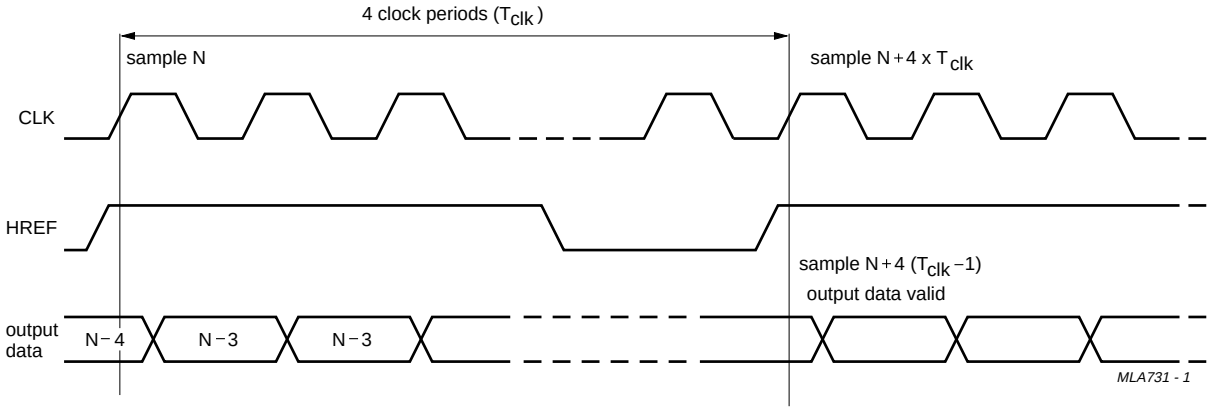


Fig.5 Load circuit for the 3-state output timing measurement.



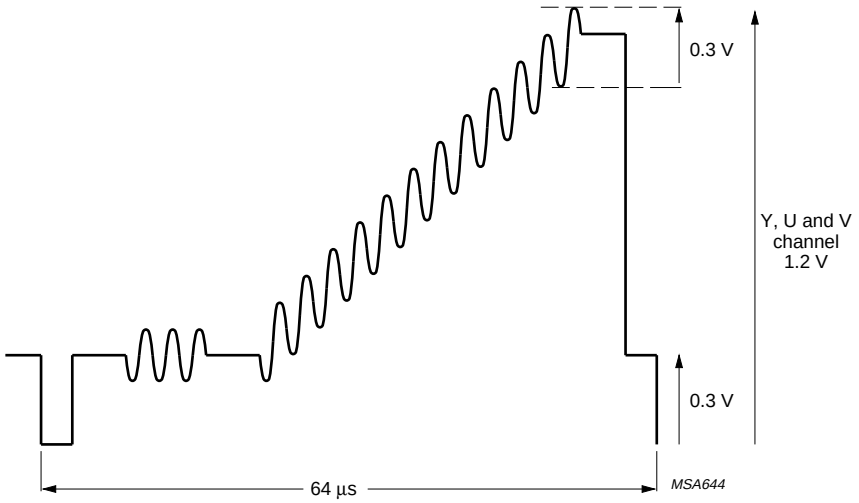
The output data is valid 4 clock periods after HREF goes HIGH.

Fig.6 Timing definition for set-up and hold times (HREF signal).



When the HREF period is a multiple of 4 clock periods, the output data is valid without any clock delay. The internal circuit always gives an internal delay of 4 clock periods as illustrated in Fig.6.

Fig.7 Timing diagram (HREF signal).



Y channel = 4.43 MHz sinewave.
U, V channel = 1.5 MHz sinewave.

Fig.8 Input test signal for differential gain and phase measurements.

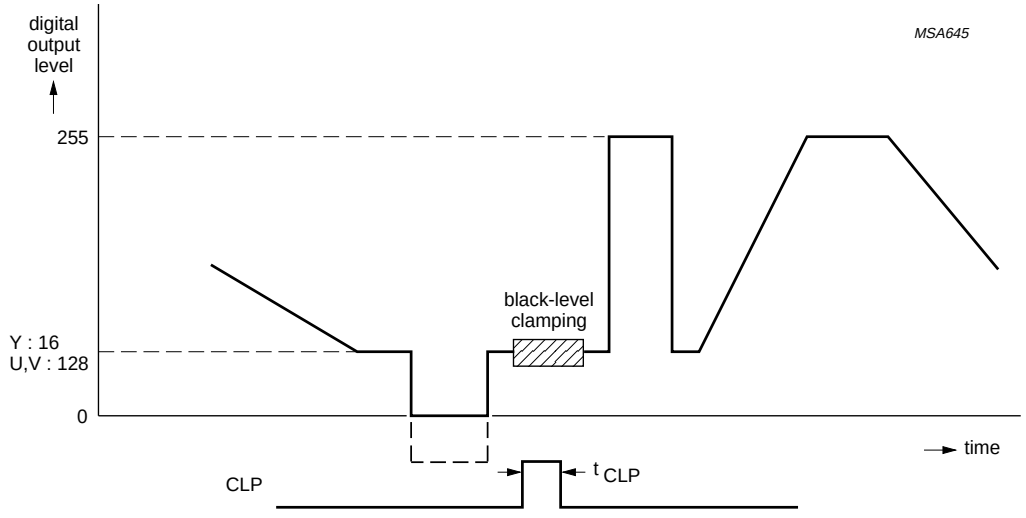
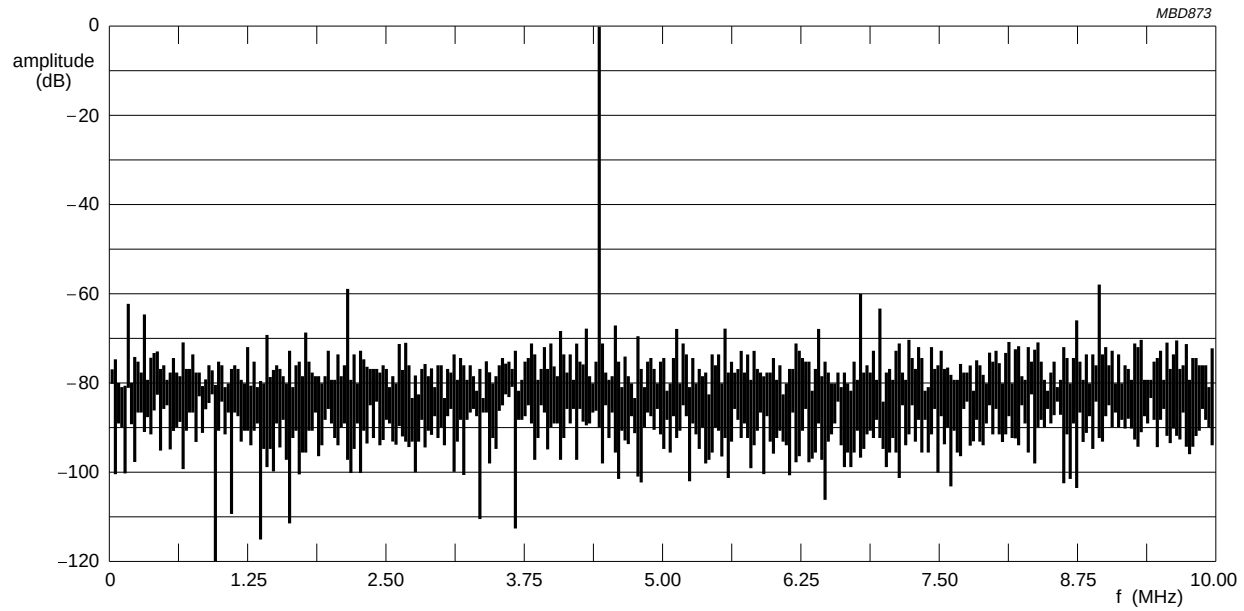


Fig.9 Clamping control timing.

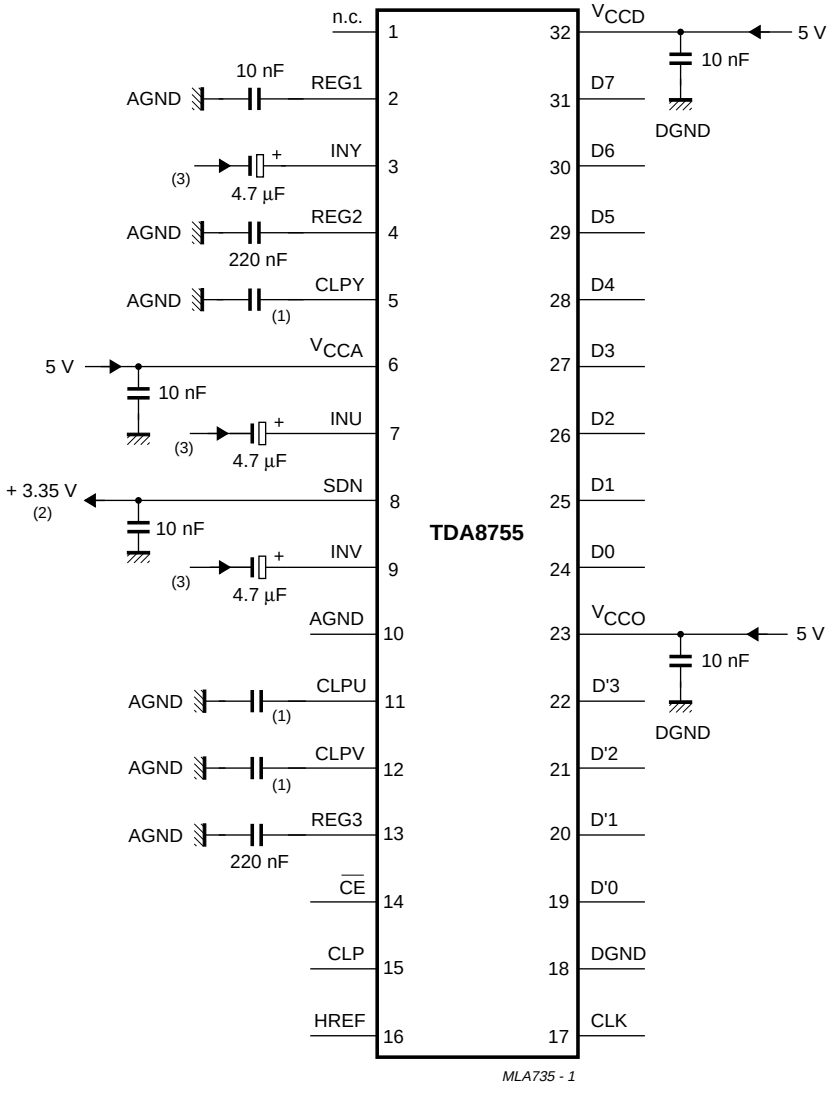


Effective bits: 7.30; THD = −53.35 dB.

Harmonic levels (dB): 2nd = −58.38; 3rd = −60.03; 4th = −57.30; 5th = −69.38; 6th = −67.09.

Fig.10 Fast Fourier Transform (f_{clk} = 20 MHz; f_i = 4.43 MHz).

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

(1) Clamp capacitors must be determined in accordance with the application; recommended values are CLPY = 18 nF, CLPU and CLPV = 33 nF.

(2) It is possible to use the reference output voltage pin SDN to drive other analog circuits under the limits indicated in Chapter “Characteristics”.

(3) Input signal pins have a high bandwidth. It is necessary to take special care on PCB layout to avoid any interaction from other signals (digital clocks for example).

Fig.11 Application diagram.

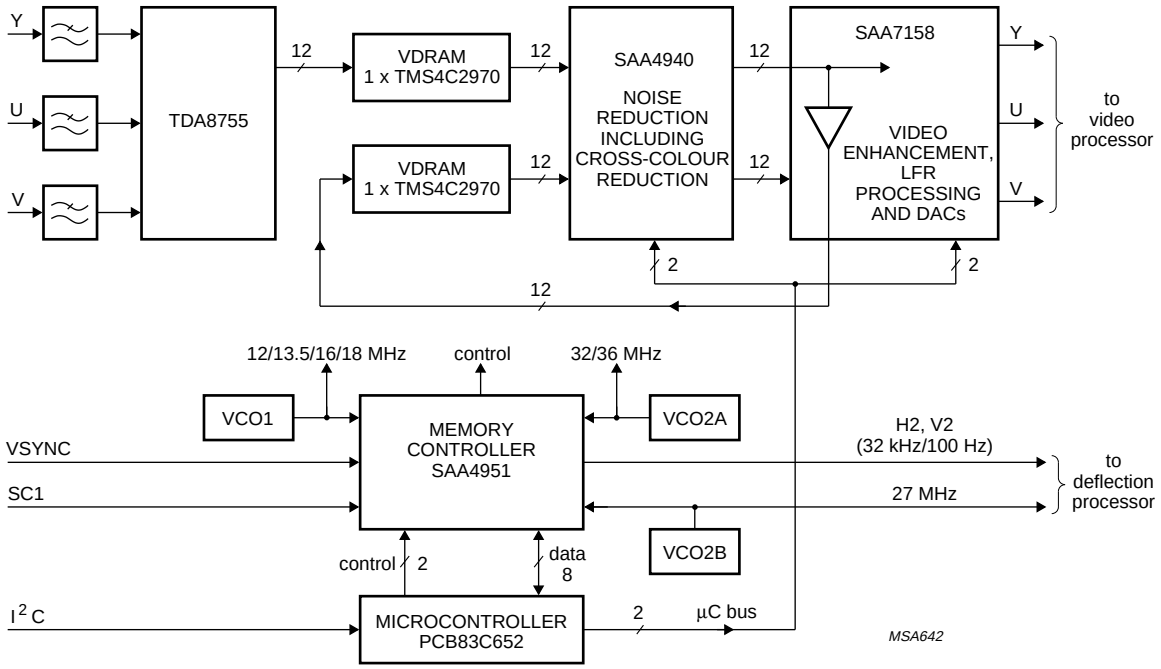


Fig.12 Block diagram of a full-options Improved Picture Quality (IPQ) module.

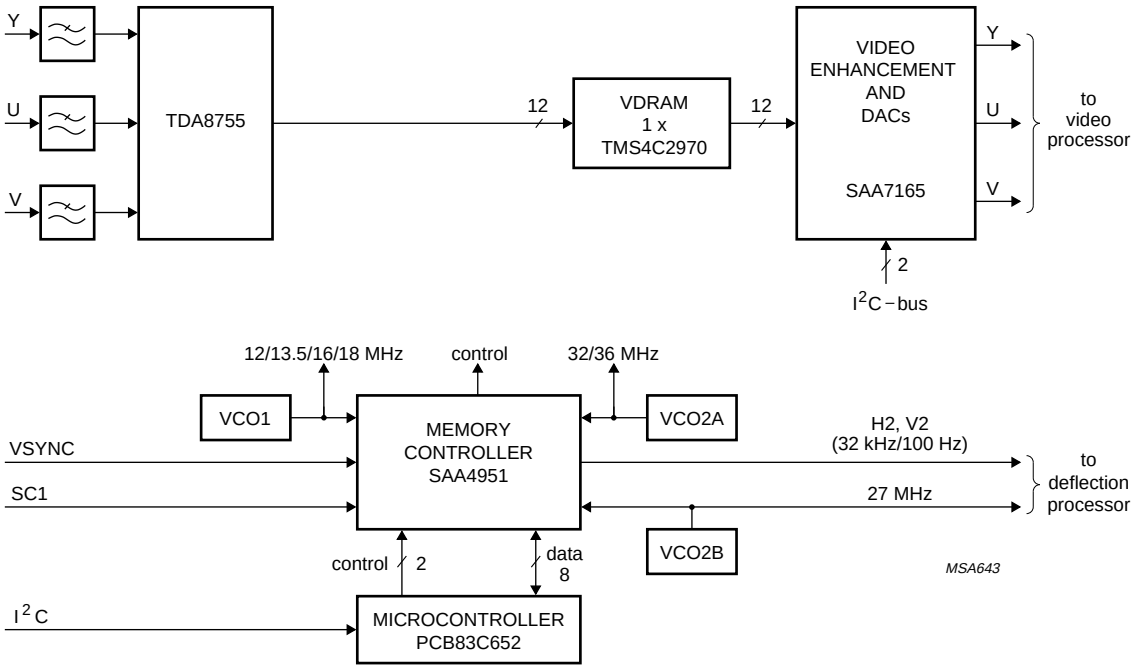
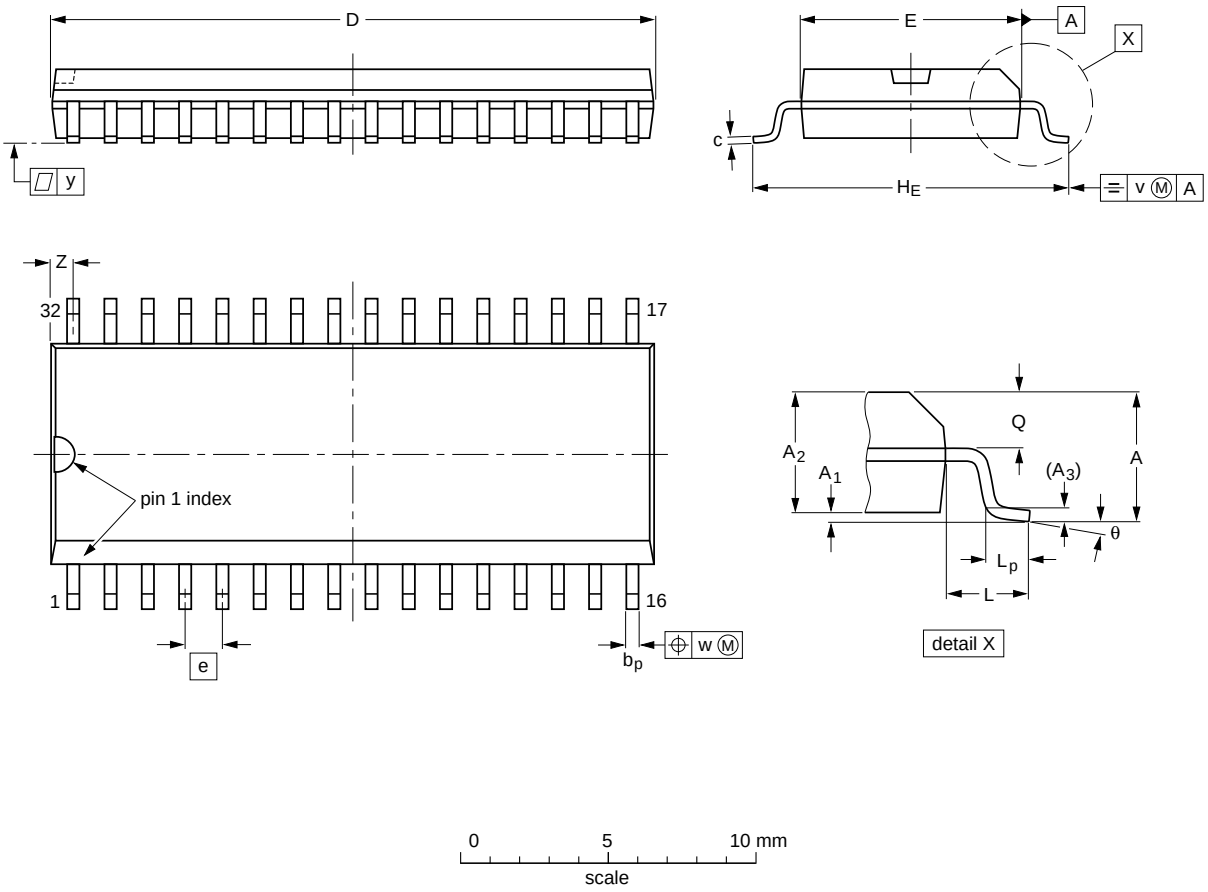


Fig.13 Block diagram of an economic Improved Picture Quality (IPQ) module.

PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~92-11-17~~ 95-01-25

SOLDERING

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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