DATA SHEET

TDA8050
QPSK transmitter

Preliminary specification
File under Integrated Circuits, IC02

1998 Jan 08

Philips
Semiconductors

PHILIPS

QPSK transmitter TDA8050

FEATURES

- Programmable gain
- PLL controlled carrier frequency
- 3 wire transmission bus
- 5 V supply voltage

APPLICATIONS

- QPSK modulation

GENERAL DESCRIPTION

The QPSK transmitter IC is a monolithic bipolar IC dedicated for quadrature modulation of the I and Q signals. It includes two double balanced mixers, a symmetrical V.C.O with 0-90 degrees signal generation for modulation, a phase locked loop for IF frequency control, a conversion mixer, a phase locked loop for RF frequency control, a gain controlled output amplifier, a three wire bus and an output buffer.

The first PLL consists of a fixed main divider, a crystal oscillator and its programmable reference divider, a phase/frequency detector combined with a fixed charge pump.

The second PLL consists of a divide by four preamplifier, a 12-bit programmable divider, a crystal oscillator and its programmable reference divider, a phase/frequency detector combined with a "clever" charge pump which drives the tuning amplifier, including 9 V output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{cc}	functional supply range	4.75	5.00	5.25	V
T_{amb}	operating ambient temperature	0		70	^{o}C
f_{rf}	output centered frequency	5		40	MHz
V_o	maximum output level		55		dBmV
f_{xtal}	crystal frequency	1		4	MHz
$f_{ref(mod)}$	reference frequency for modulator synthesizer		250		kHz
f_{step}	frequency step size for converter synthesizer	50		500	kHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8050T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

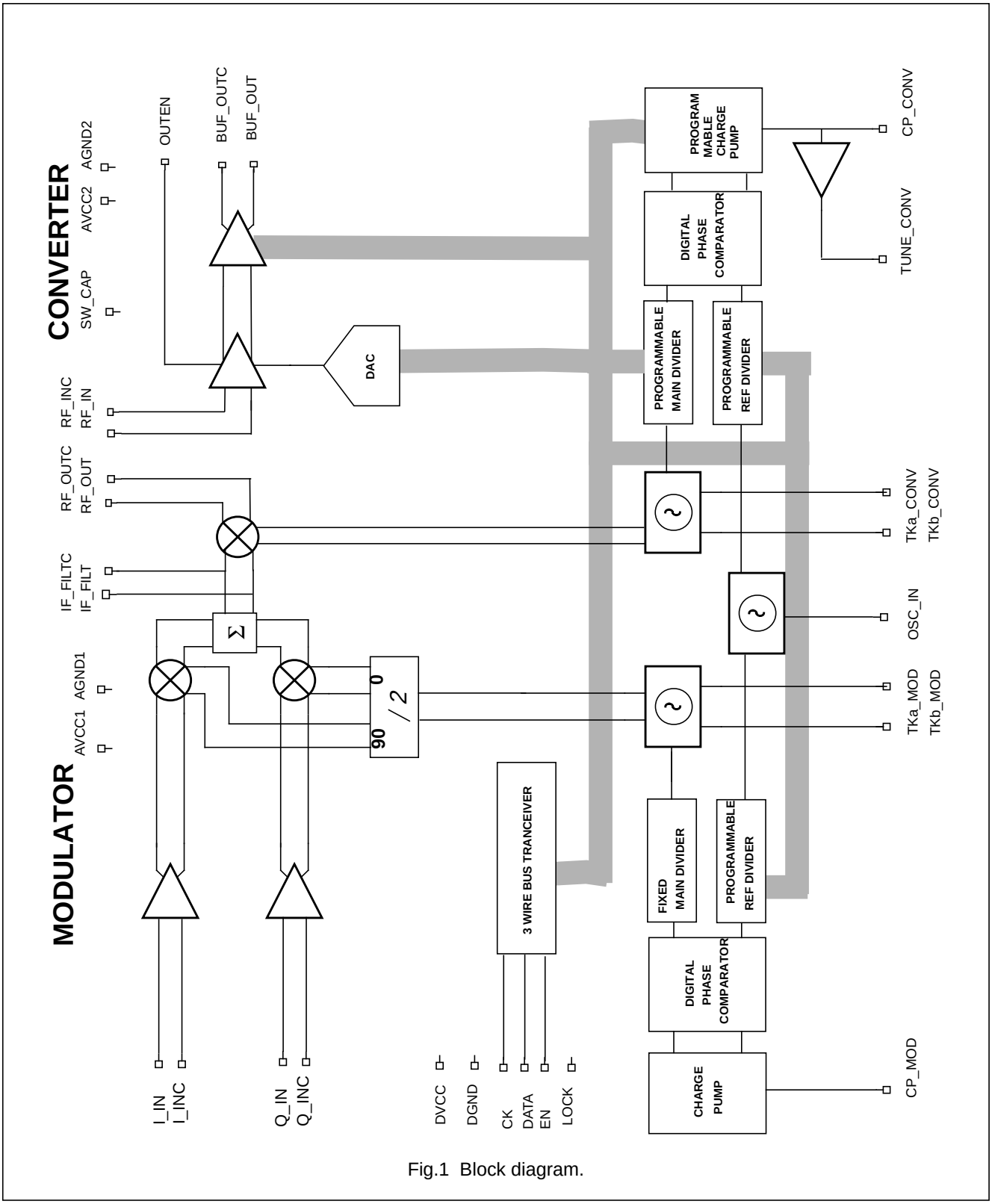


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTEN	1	output Enable
BUF_OUT	2	output amplifier balanced output
BUF_OUTC	3	output amplifier balanced output
AGND2	4	converter analog ground
I_IN	5	I balanced input
I_INC	6	I balanced input
Q_IN	7	Q balanced input
Q_INC	8	Q balanced input
AGND1	9	modulator analog ground
TKa_MOD	10	modulator VCO tank circuit input 2
TKb_MOD	11	modulator VCO tank circuit input 1
CP_MOD	12	modulator charge pump output for PLL loop filter
DVCC	13	digital supply
CK	14	3 wire bus serial Control Clock
DATA	15	3 wire bus serial Control Data
EN	16	3 wire bus serial Control Enable
OSC_IN	17	crystal oscillator input
DGND	18	digital ground
CP_CONV	19	converter charge pump output for PLL loop filter
TUNE_CONV	20	tuning voltage output for converter VCO
TKb_CONV	21	converter VCO tank circuit input 1
TKa_CONV	22	converter VCO tank circuit input 2
LOCK	23	lock detect signal
IF_FILT	24	IF balanced output to filter
IF_FILTC	25	IF balanced output to filter
AVCC1	26	modulator analog supply
RF_OUTC	27	RF balanced output to filter
RF_OUT	28	RF balanced output to filter
AVCC2	29	converter analog supply
RF_IN	30	RF balanced input to programmable amplifier
RF_INC	31	RF balanced input to programmable amplifier
SW_CAP	32	switch capacitor

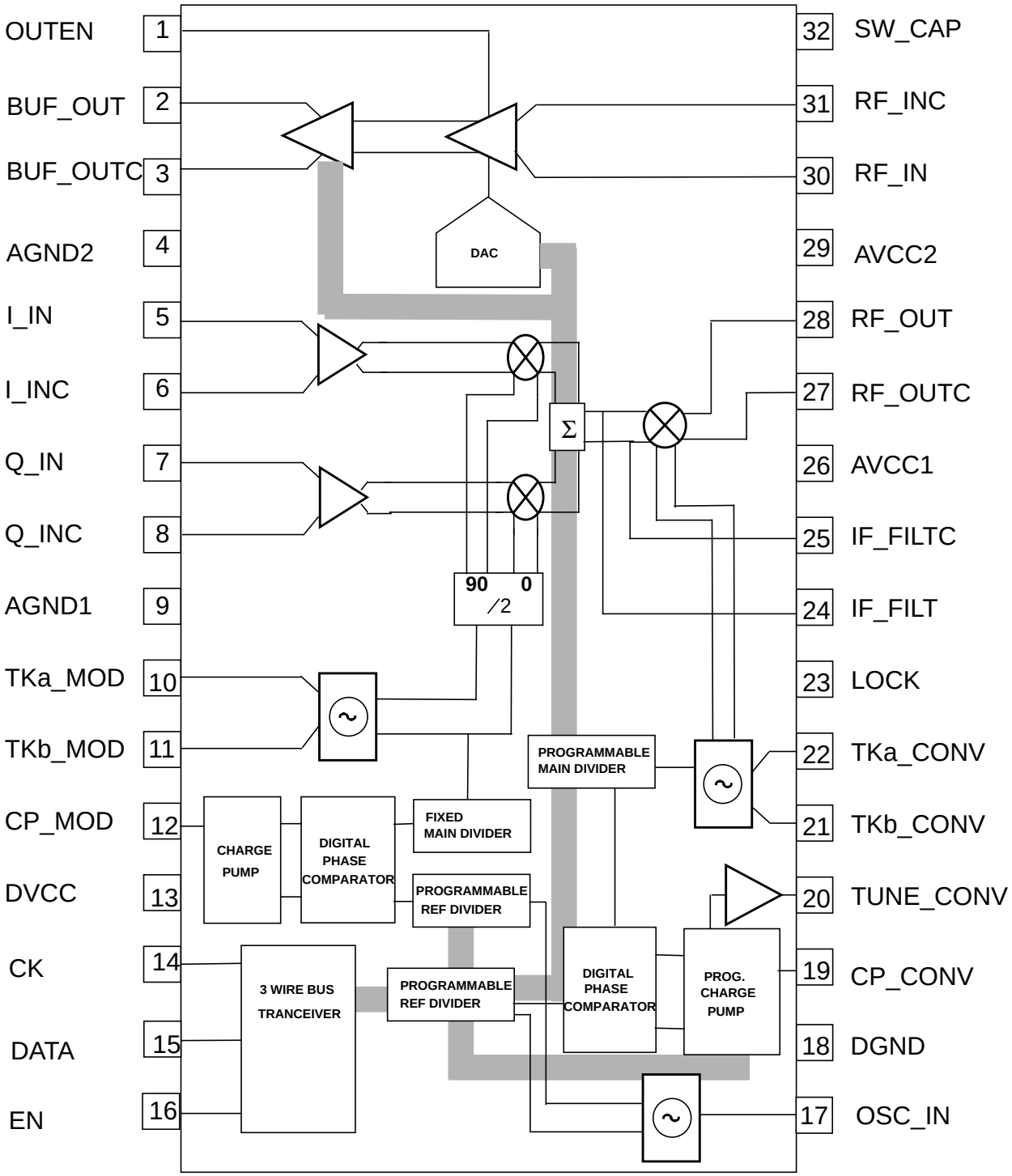


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The I and Q signals are presented under the form of balanced analog signal at a level of 400 mVpp. These signals are mixed by two double balanced mixers with the signal generated by a first local oscillator to provide the modulated signal.

This signal is then filtered by an IF filter and converted by a balanced mixer with the signal generated by a second local oscillator to provide the QPSK signal.

This signal is then amplified by a gain controlled amplifier to a level suitable for its transmission. The gain of the amplifier is controlled by bus. The gain controlled amplifier can be disabled when not transmitting in order to provide signal attenuation.

The amplified signal is applied to an on chip amplifier. This amplifier has balanced outputs (open collector) which are linked to two off chip resistors (values 150 Ω), linked to +9 V. The balanced outputs are designed to drive a transformer 2:1 (Siemens V944) loaded with 75 Ω which gives an output level of 55 dBmV. The output frequency range of the transmitter is 5-40 MHz.

The frequency of the first local oscillator is fixed thanks to the Phase Locked Loop implemented in the circuit. The VCO needs an external LC tank circuit with two varicap diodes. The oscillator operates at twice the frequency (ie 280 MHz).

The frequency of the second local oscillator is programmable thanks to the Phase Locked Loop implemented in the circuit. The VCO needs an external LC tank circuit with two varicap diodes. The oscillator operates in the 145 up to 180 MHz bandwidth.

The data sent to the PLL is loaded in bursts framed by the signal EN. Programming clock edges (rising clock edges), together with their appropriate data bits, are ignored until EN becomes active (low). The internal latches are updated with the latest programming data when EN returns inactive (high). Only the last 14 bits are retained within the programming register. No check is made on the number of clock pulses received during the time that programming is enabled. **EN going high while CLOCK is still low generates a wrong active clock edge causing a shift of the data bits**. At power up, EN should be high. The lock detector output LOCK is high when both PLLs are in lock.

The main divider ratio and the reference divider ratios are provided via the serial bus. A control register controls the DAC, the output amplifier and the charge pump currents.(Table 1, 2 , 3).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{cc}	supply voltage		–0.3	6.0	V
T_{amb}	operating ambient temperature		0	70	°C
T_{sg}	IC storage temperature		–40	+150	°C
T_j	maximum junction temperature		–	+150	°C
t_{sc}	short circuit time (every pin to Vcc or GND)		–	10	s
V_{MAX}	voltage on all pins except BUF_OUT, BUF_OUTC, TUNE_CONV		–0.3	V_{CC}	V
$V_{o(TUNE)}$	output tuning voltage		–0.3	30	V
$V_{O(BUF)}$	output buffer voltage on pin BUF_OUT & BUF_OUTC			10	V
P_{tot}	maximum power dissipation			800	mW

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	63	K/W

HANDLING

HBM: The IC pins withstand 2 KV except pins 27 and 28 (1750 V).
MM: The IC pins withstand 100 V.

CHARACTERISTICS

Measured in application circuit with the following conditions :
V_{cc} = 5 V, T_{amb} = 25°C; unless otherwise specified.
All AC units are rms values, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{CC(mod)}$	modulator analog supply voltage		4.75	5	5.25	V
$I_{CC(mod)}$	modulator analog supply current			41		mA
$V_{CC(conv)}$	converter analog supply voltage		4.75	5	5.25	V
$I_{CC(conv)}$	converter analog supply current			48		mA
$I_{CC(buf)}$	buffer output supply current			44		mA
V_{CCD}	digital supply voltage		4.75	5	5.25	V
I_{CCD}	digital supply current			22		mA
$V_{CC(TUNE)}$	tuning supply voltage				9	V
Quadrature modulator						
I and Q inputs						
$V_{i(DC)}$	input DC level	over the complete range of temperature		$0.5*V_{CC}$		V
V_i	signal input level (balanced)	Indicative		400	500	mVpp
$f_{i(max)}$	I and Q maximum input frequency	Indicative		10		MHz
Z_i	differential input impedance			4.4		kΩ
BW	amplifier 1 dB bandwidth	Indicative		10		MHz
Modulator						
f_O	output centered frequency				140	MHz
ΔA	amplitude imbalance	Fig.3			± 1	dB
$\Delta\Phi$	phase imbalance				± 2	deg
LO_{sup}	LO suppression	Fig.3		–28		dBc
Z_o	differential output impedance			1.8		kΩ
Modulator Voltage Controlled Oscillator						
$F_{OSC(mod)}$	oscillation frequency				280	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Converter output						
V_O	output level	f = 30 MHz V_i = 100mV$_{dif}$ at I and Q inputs	37.5	40	42.5	dBmV
ΔV_O	output flatness	f = 5 to 40 MHz V_i = 100 mV$_{dif}$ at I and Q inputs			2	dB
f_O	output centered frequency		5		40	MHz
Z_o	differential output impedance			150		Ω
IM3	3rd order intermodulation distorsion	Fig.4			–35	dBc
H2	2nd order harmonic of 5 to 40 MHz signal	f = 10 to 80 MHz V_i = 100 mV$_{dif}$ at I and Q inputs			–45	dBc
H3	3rd order harmonic of 5 to 40 MHz signal	f = 15 to 120 MHz V_i = 100 mV$_{dif}$ at I and Q inputs			–45	dBc
S_O	mixer spurious outputs of 5 to 40 MHz signal	f = 5 to 40 MHz V_i = 100 mV$_{dif}$ at I and Q inputs			–50	dBc
Converter voltage controlled oscillator						
$f_{osc(conv\_min)}$	minimum oscillation frequency				145	MHz
$f_{osc(conv\_max)}$	maximum oscillation frequency		180			MHz
Programmable gain and output buffer note1						
Z_i	differential input impedance			5.6		kΩ
ΔG	output level step size				2	dB
Δbuf_O	output level adjust range	V_i = 30 dBmV sine wave 40 MHz at pin RF_IN, RF_INC DAC = 0 to 31	32			dB
V_o	output level			55		dBmV
ΔV_o	output flatness	f = 5 to 40 MHz V_i = 30 dBmV sine wave DAC = 28			2	dB
$V_{IL(en-low)}$	output controlled enable Low	output buffer on			0.8	V
$V_{IH(en-high)}$	output controlled enable High	output buffer off	2.4			V
ISO	disable isolation	V_i = 100 mV$_{dif}$ V_o = 55 dBmV DAC = 28 f=40 MHz OE = 0,5	–35			dBc
$G_{V(max)}$	maximum gain	Fig.5		22		dB
$V_{o(1dB)}$	1 dB compression point	Fig.5	60			dBmV

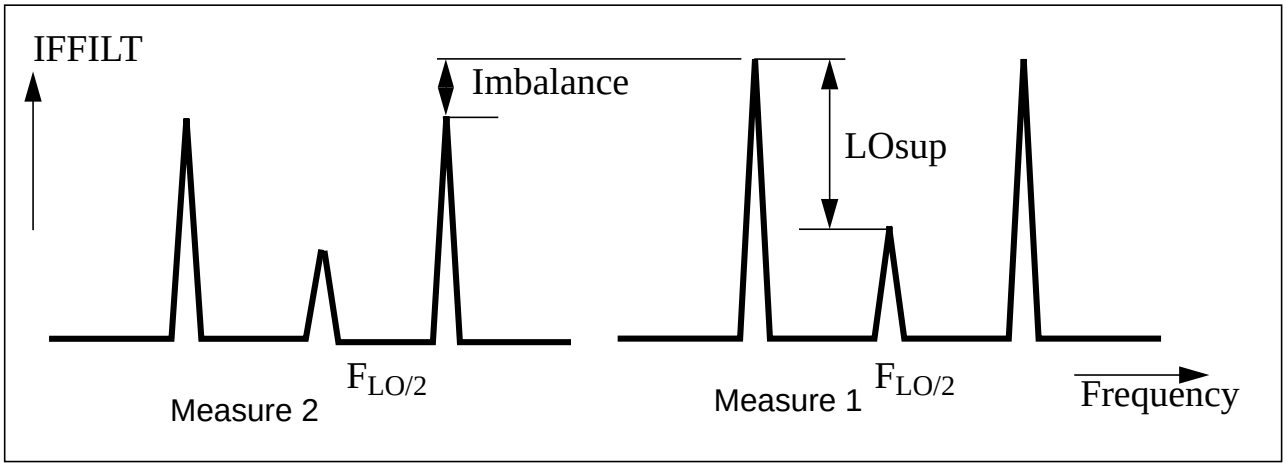
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
H2	2nd order harmonic of 5 to 40 MHz signal	f = 10 to 40 MHz f = 54 to 120 MHz Fig.6			–45 –35	dBc
H3	3rd order harmonic of 5 to 40 MHz signal	f = 15 to 40 MHz f = 54 to 120 MHz Fig.6			–45 –35	dBc
Overall note 1						
Φ_{osc}	phase noise	at 10 kHz at100 kHz Note 2		–70 –90		dBc/Hz
S_o	spurious signals of 5 to 40 MHz signal	f = 5 to 40 MHz Vin = 10 mV_{dif} at I and Q inputs Vout = 30 to 55 dBmV			–50	dBc
ISO_{tot}	total isolation at I/Q midrange	Fig.7			–65	dBc
C/N	carrier to noise ratio at final output at 2 MHz from carrier	Vin = 100 mV_{dif} Vout = 35 to 55 dBmV f = 26.5 MHz		113		dBc/Hz
Crystal oscillator						
f_{xtal}	crystal frequency	Note 3	1		4	MHz
Z_i	input impedance	Fxtal = 4 MHz	600	1200		Ω
$V_{i(DC)}$	DC input level			2.9		V
Modulator Synthesizer						
$f_{ref(mod)}$	reference frequency			250		kHz
RDR1	reference divider ratio		4		16	
ND1	fix main divider ratio			1120		
$I_{(cp)}$	charge-pump current	fixed		0.30		mA
Converter Synthesizer						
f_{step}	step size		50		500	kHz
RD2	fix reference divider ratio			2		
RDR2	reference divider ratio	table 4	4		160	
ND2	fix main divider ratio			4		
NDR2	programmable main divider ratio	table 4	290		3600	
Three wire bus						
V_L	input Low level				0.8	V
V_H	iInput High level		2.4			V
Lock detect pin						
$V_{O(lock)}$	output voltage (LOCK)			5		V
$V_{O(unlock)}$	output voltage (UNLOCK)			0.02		V
Serial control clock						
f_{ck}	clock frequency			330		kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{su}	input data to CK set-up time	Fig.3		2		µs
t_h	input data to CK hold time	Fig.3		1		µs
t_{start}	delay to rising clock edge	Fig.3		3		µs
t_{end}	delay from last clock edge	Fig.3		3		µs

Notes

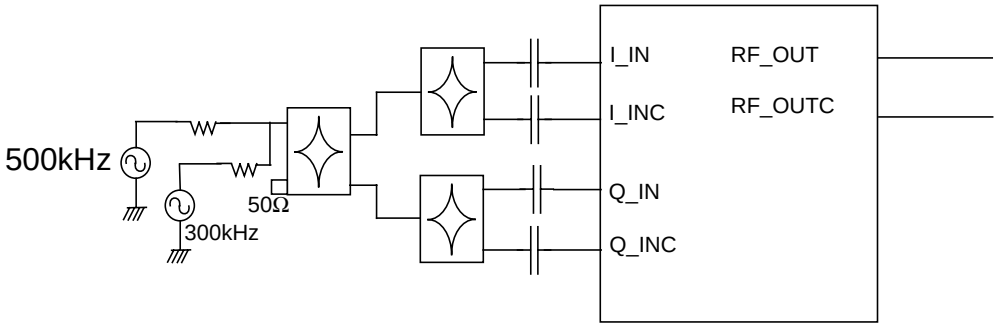
1. All the specification points regarding the output section and the overall circuit are measured after the transformer 2:1 (siemens V944) loaded with 75 Ω.
2. Overall phase noise
   Converter: $I_{(cp)}$ = 0.36 mA
   f_{ref} = 12.5 kHz
   I&9 = 100 mV_{dif}
   V_O= 55 dBmV
   DAC = 28
   f = 26.5 MHz
3. Crystal oscillator
   the crystal oscillator uses a 4 MHz, 2 MHz or 1 MHz crystal in series with a capacitor. The crystal is parallel resonant with load capacitance of 18 to 20 pF. The connection to V_{CC} is prefered but it might also be to GND.

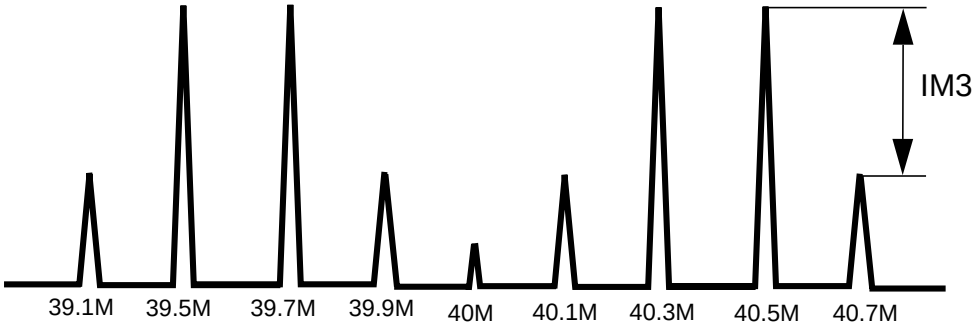
NOTES TO THE CHARACTERISTICS



The amplitude imbalance and the LO suppression are measured in the spectrum of the signal measured at the output IF_FILT and are defined in the following conditions :
measure 1: I input frequency = 500 kHz. I input level = 400 mVpp sine wave. Unused input as 0 volt differential.
measure 2: Q input frequency = 500 kHz. Q input level = 400 mVpp sine wave. Unused input as 0 volt differential.

Fig.3 Imbalance and LO suppression





3rd order intermodulation distorsion

Two tones of 260 mVpp at each input input I&Q:

$$Vavg = \frac{400}{2} \times 10^{\frac{-4}{20}} = 128mVrms$$

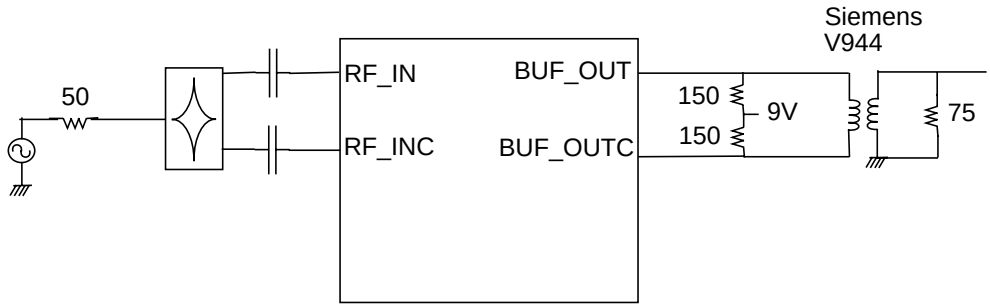
2 sine wave with a total rms values of 128 mVrms give:

$$\sqrt{2 \times x^2} = 128$$

$$x = \frac{128}{\sqrt{2}} = 90mVrms = 260mVpp$$

and f1 = 300 kHz, f2 = 500 kHz and f_{RF} = 40 MHz.

Fig.4 IM3



DAC = 31
f = 26.5 MHz
Vin variable to have a variable output voltage.

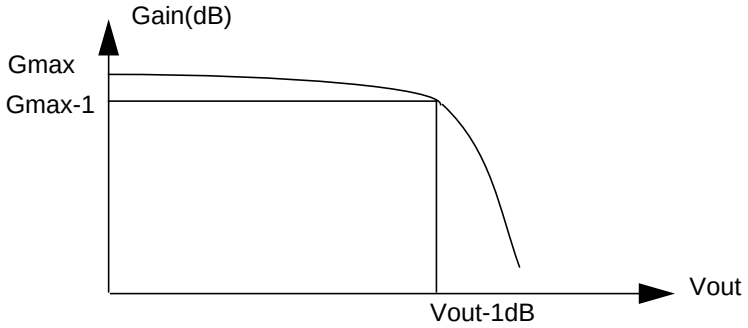
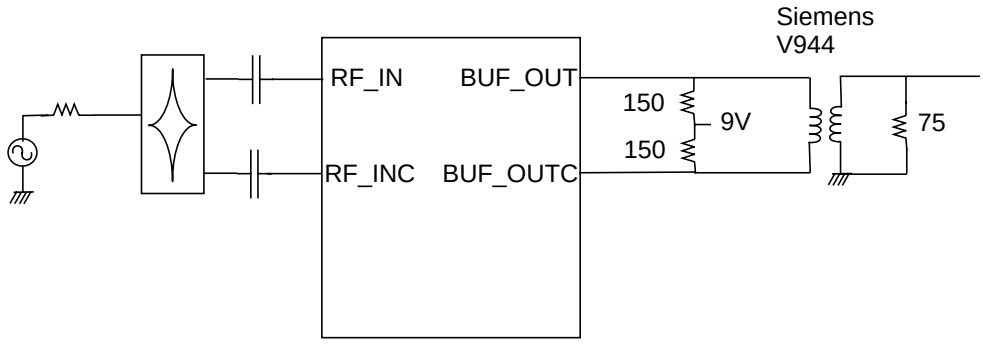
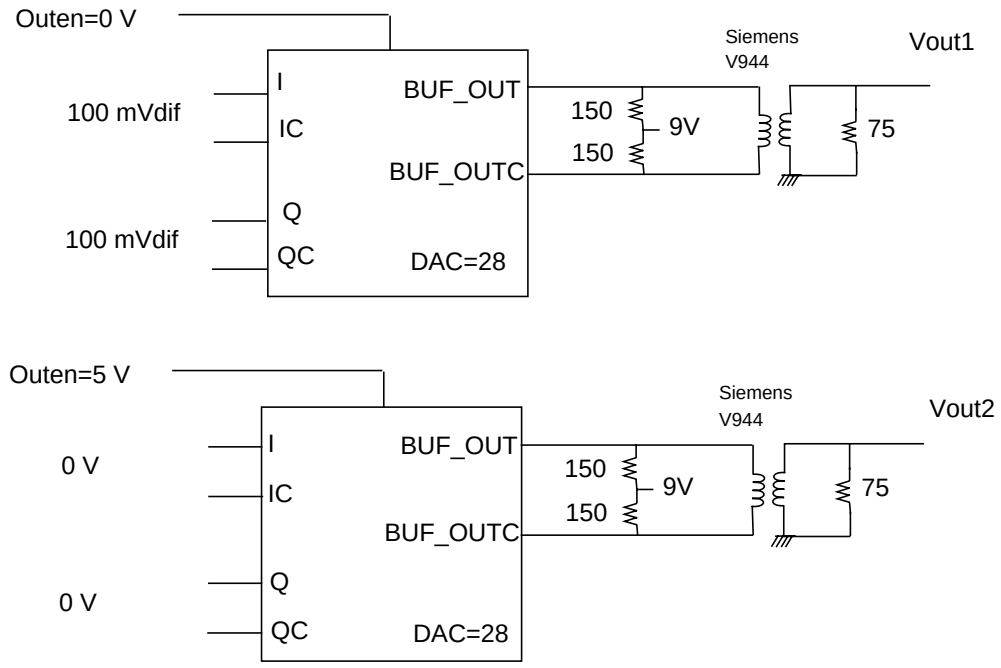


Fig.5 Maximum gain and compression point



DAC = 28
f = 5 to 40 MHz
Vin = 200 mV sine wave
Vout = 55 dBmVrms

Fig.6 Harmonics of output section H2 and H3



ISO_{tot} = Vout1(dB) -Vout2(dB)

Fig.7 Isotot

APPLICATION INFORMATION

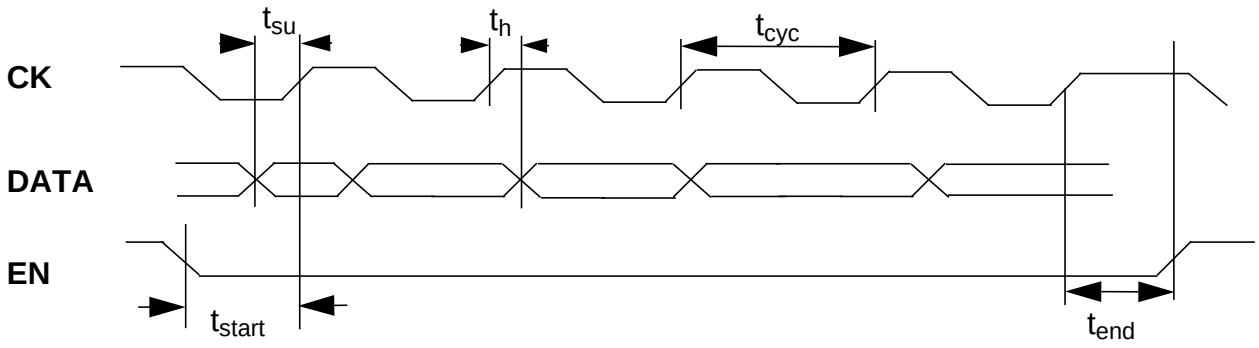


Fig.8 3 wire bus timing.

Table 1

DATA FORMAT

DATA												ADDRESS	
d11 first in	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	ad1	ad0 last in
MODULATOR REFERENCE DIVIDER RATIO				CONVERTER REFERENCE DIVIDER RATIO									
x	x	mp1	mp0	r7	r6	r5	r4	r3	r2	r1	r0	0	1
CONTROL REGISTER													
x	x	x	oen	cr2	cr1	cr0	dac4	dac3	dac2	dac1	dac0	1	0
MAIN DIVIDER RATIO													
p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0	1	1

Notes

1. X = don’t care
2. When OEN (output enable) is at ‘0’, output is disabled, at ‘1’ output is enabled.
3. When DAC4..0 is ‘0’, minimum gain is programmed at ‘1’ maximum gain is programmed.
4. MP1,. MPO : Modulator reference divider ratio (see table 2
5. CR2,CRO: Converter synthesizer charge pump current(see table3

Table 2

Modulator reference divider ratio

MP1	MP0	PROGRAMMED RATIO
1	1	4
1	0	8
0	1	16

Table 3

Converter synthesizer charge pump current

CR2	CR1	CR0	LOCK_CONV	ICP(MA)
0	0	0	0	1.2
0	0	0	1	0.36
0	0	1	0	0.36
0	0	1	1	0.1
0	1	0	x	0.1
0	1	1	x	0.36
1	0	0	x	1.2

Table 4

CONVERTER SYNTHESIZER table fcomp = fosc/RD

fosc\fcomp	**12.5 kHz**	**25 kHz**	**50 kHz**	**125 kHz**
1 MHz	80	40	20	8
4 MHz	320	160	80	32

CONVERTER SYNTHESIZER table ND = 4 f_lo = ND*NDR*fcomp = NDR*step

F_LO\step	50 kHz	100 kHz	200 kHz	500 kHz
145 MHz	2900	1450	725	290
180 MHz	3600	1800	900	360

Where lock_conv is an internal signal and lock_conv is zero (resp. one) when the converter PLL is out-of-lock (resp in-lock)

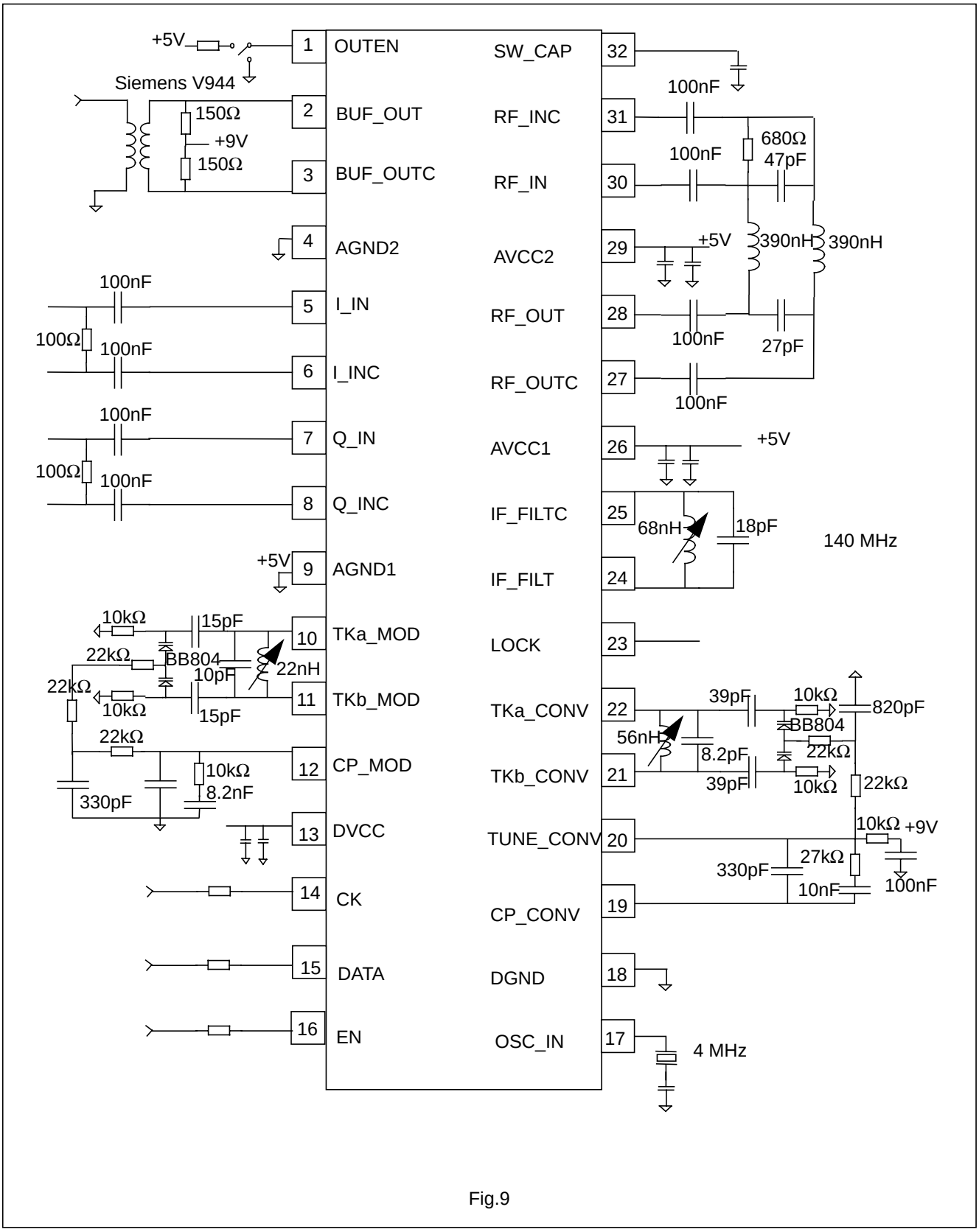
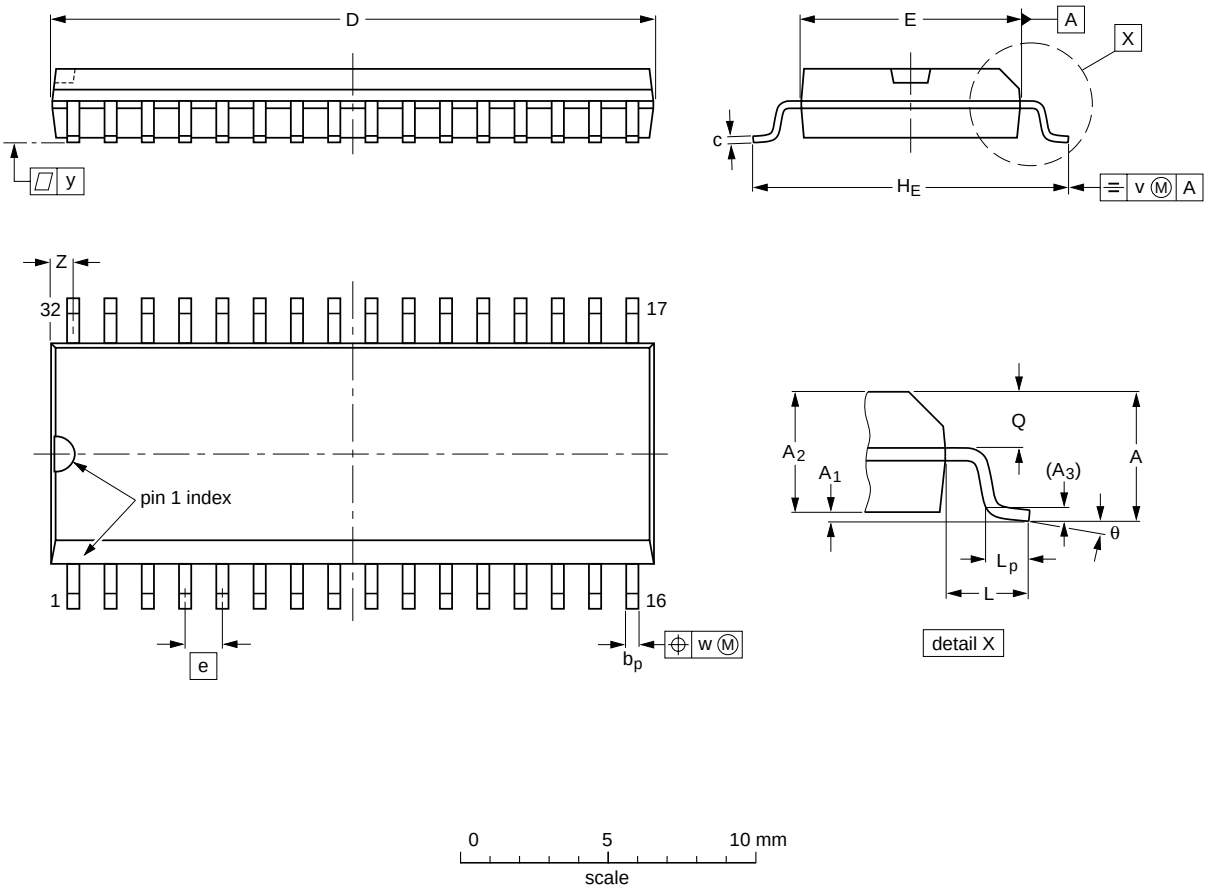

+5V
1
OUTEN
SW_CAP
32
Siemens V944
100nF
2
BUF_OUT
RF_INC
31
150Ω
+9V
150Ω
680Ω
47pF
100nF
3
BUF_OUTC
RF_IN
30
4
AGND2
AVCC2
29
+5V
390nH
390nH
100nF
5
I_IN
RF_OUT
28
100Ω
100nF
100nF
27pF
6
I_INC
RF_OUTC
27
100nF
100nF
7
Q_IN
AVCC1
26
+5V
100Ω
100nF
8
Q_INC
IF_FILTC
25
68nH
18pF
140 MHz
+5V
9
AGND1
IF_FILT
24
10kΩ
15pF
10
TKa_MOD
LOCK
23
22kΩ
BB804
22nH
10pF
22kΩ
11
TKb_MOD
TKa_CONV
22
39pF
10kΩ
820pF
10kΩ
15pF
56nH
BB804
22kΩ
22kΩ
8.2pF
39pF
10kΩ
22kΩ
12
CP_MOD
TKb_CONV
21
10kΩ
8.2nF
330pF
10kΩ +9V
13
DVCC
TUNE_CONV
20
27kΩ
330pF
10nF
100nF
14
CK
CP_CONV
19
15
DATA
DGND
18
16
EN
OSC_IN
17
4 MHz

Fig.9

PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Printed in The Netherlands 547047/1200/01/pp20 Date of release: 1998 Jan 08 Document order number: 9397 750 03145

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