



# TDA7443D

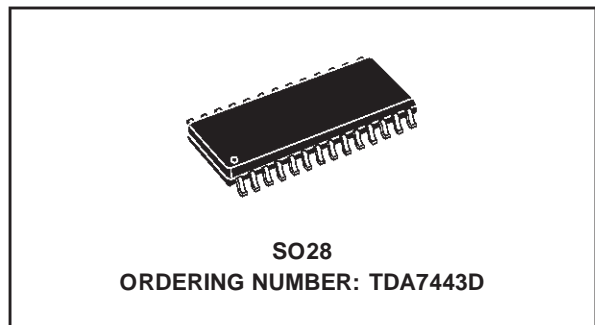
## TONE CONTROL AND SURROUND DIGITALLY CONTROLLED AUDIO PROCESSOR WITH AGC

PRODUCT PREVIEW

- INPUT MULTIPLEXER
  - 5 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- AGC
- TREBLE AND BASS CONTROL IN 2.0dB STEPS
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
  - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
  - INDEPENDENT MUTE FUNCTION
- TWO SURROUND MODES AVAILABLE
  - MUSIC
  - PSEUDO STEREO
- ALL FUNCTIONS ARE PROGRAMMABLE VIA SERIAL BUS

### DESCRIPTION

The TDA7443D is a volume tone (bass and treble)



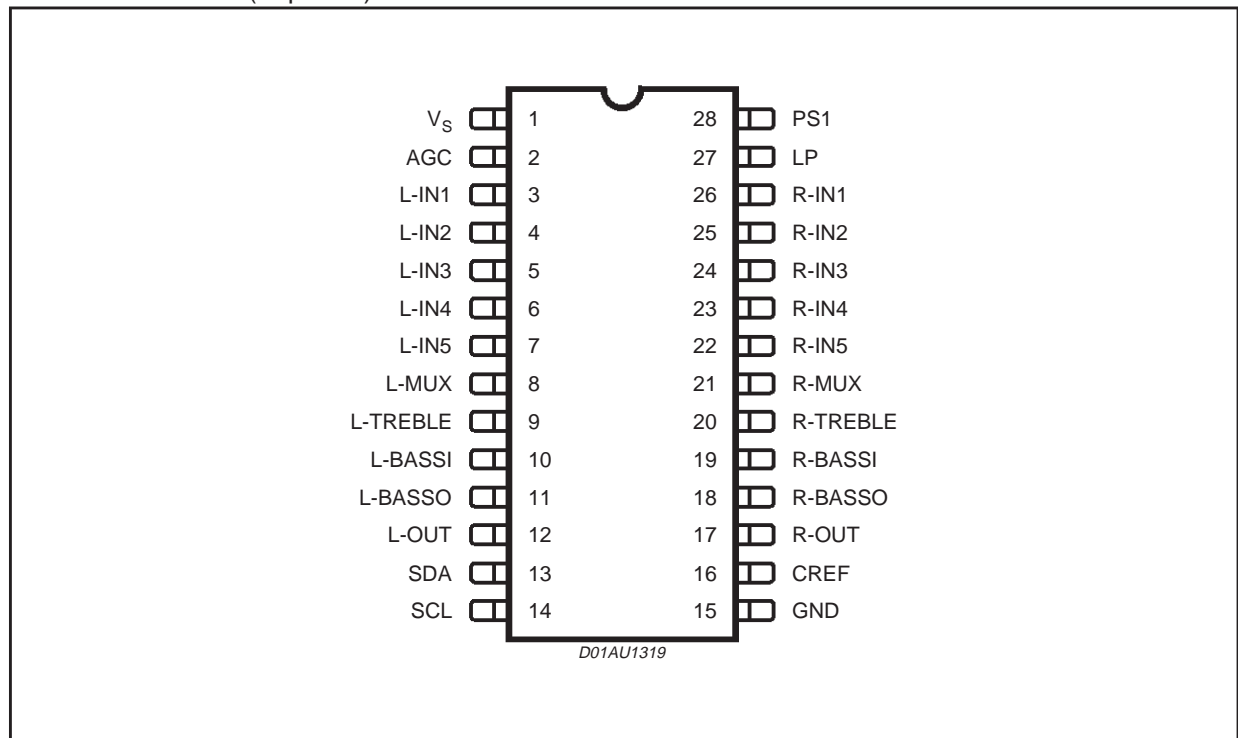
balance (Left/Right) processor for quality audio applications in Hi-Fi systems.

Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

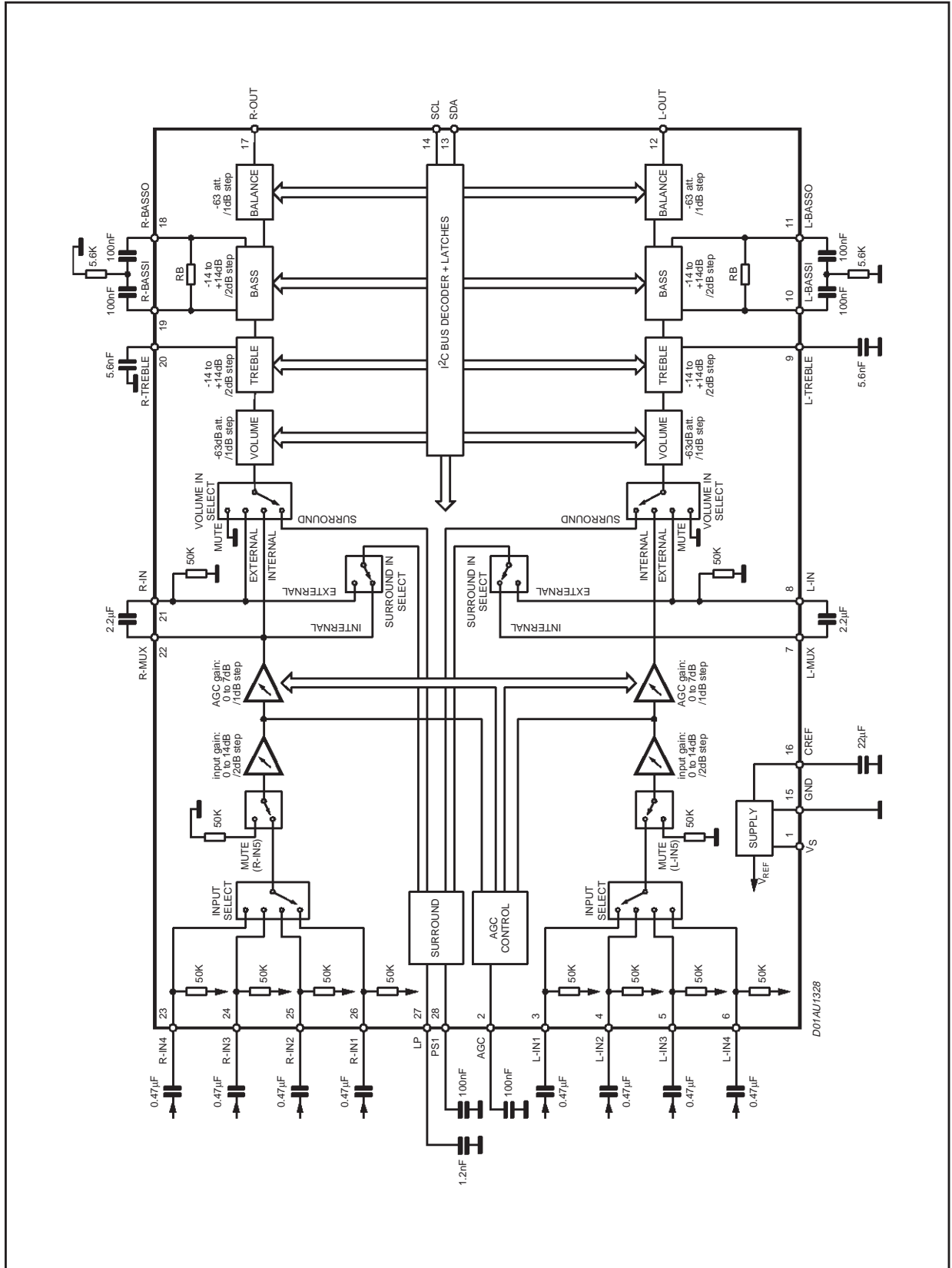
The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

### PIN CONNECTION (Top view)



BLOCK DIAGRAM & TEST CIRCUIT



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>s</sub>	Operating Supply Voltage	10.5	V
T <sub>amb</sub>	Operating Ambient Temperature	-10 to 85	°C
T <sub>stg</sub>	Storage Temperature Range	-55 to 150	°C

**THERMAL DATA**

Symbol	Parameter	Value	Unit
R <sub>th j-pin</sub>	Thermal Resistance Junction-pins	85	°C/W

**QUICK REFERENCE DATA**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>S</sub>	Supply Voltage	5	9	10	V
V <sub>CL</sub>	Max. input signal handling	2			V <sub>rms</sub>
THD	Total Harmonic Distortion V=1V <sub>rms</sub> f=1kHz		0.01	0.1	%
S/N	Signal to Noise Ratio V <sub>OUT</sub> =1V <sub>rms</sub> (mode=OFF)		100		dB
S <sub>C</sub>	Channel Separation f=1kHz		90		dB
	Input Gain (2dB step)	0		14	dB
	AGC Gain (1dB step)	0		7	dB
	Volume Control (1dB step)	-63		0	dB
	Treble Control (2dB step)	-14		+14	dB
	Bass Control (2dB step)	-14		+14	dB
	Balance Control (1dB step)	-63		0	dB
	Mute Attenuation		90		dB

## TDA7443D

### ELECTRICAL CHARACTERISTICS

(Refer to the test circuit  $T_{amb}=25^{\circ}\text{C}$ ,  $V_s=9\text{V}$ ,  $f=1\text{kHz}$ , all controls flat, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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#### SUPPLY

$V_S$	Supply Voltage		5	9	10	V
$I_S$	Supply Current			tbd		mA
SVR	Ripple Rejection		60	80		dB

#### INPUT STAGE

$R_{IN}$	Input Resistance		35	50	65	$k\Omega$
$V_{CL}$	Clipping Level	THD = 0.3%	2	2.5		$V_{rms}$
$S_{IN}$	Input Separation		80	100		dB
$G_{in\ min}$	Minimum Input Gain		-1	0	1	dB
$G_{in\ max}$	Maximum Input Gain		13	14	15	dB
$G_{in\ step}$	Step Resolution		1.5	2	2.5	dB

#### AGC

$G_{AGCmin}$	Minimum AGC Gain		-1	0	1	dB
$G_{AGCmax}$	Maximum AGC Gain		6	7	8	dB
$G_{AGCstep}$	Step Resolution		0.5	1	1.5	dB

#### SURROUND

$R_{IN}$	Input Resistance		35	50	65	$k\Omega$
$R_{PS0}$	Phase Shifter:D1=0,D0=0		8.3	11.8	15.2	$k\Omega$
$R_{PS1}$	Phase Shifter:D1=0,D0=1		10	14.1	18.3	$k\Omega$
$R_{PS2}$	Phase Shifter:D1=1,D0=0		12.6	17.9	23.3	$k\Omega$
$R_{PS3}$	Phase Shifter:D1=1,D0=1		26.4	37.3	48.85	$k\Omega$
$C_{RANGE}$	Effect Control Range		-21		-6	dB
$S_{step}$	Effect Control Step Resolution		0.5	1	1.5	dB

#### VOLUME CONTROL

$A_{VOLmin}$	Minimum Attenuation		-1	0	1	dB
$A_{VOLmax}$	Maximum Attenuation		61	63	65	dB
$A_{VOLstep}$	Step Resolution		0.5	1	1.5	dB
$E_A$	Attenuation set error	$A_V = 0$ to $-24$ dB	-1	0	1	dB
		$A_V = -24$ to $-63$ dB	-2	0	2	dB
$V_{DC}$	DC Steps	Adjacent att. steps	-3	0	3	mV

#### BASS CONTROL

$G_B$	Control Range	Max. Boost/Cut	$\pm 12$	$\pm 14$	$\pm 16$	dB
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**ELECTRICAL CHARACTERISTICS** (continued)(Refer to the test circuit  $T_{amb}=25^{\circ}\text{C}$ ,  $V_s=9\text{V}$ ,  $f=1\text{kHz}$ , all controls flat, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$B_{\text{step}}$	Step Resolution		1	2	3	dB
$R_B$	Internal Feedback Resistance		33	44	55	$\text{k}\Omega$

**TREBLE CONTROL**

$G_T$	Control Range	Max. Boost/Cut	$\pm 13$	$\pm 14$	$\pm 15$	dB
$T_{\text{step}}$	Step Resolution		1	2	3	dB
$R_T$	Internal Feedback Resistance			25		$\text{k}\Omega$

**BALANCE CONTROL**

$A_{\text{BALmin}}$	Minimum Attenuation		-1	0	1	dB
$A_{\text{BALmax}}$	Maximum Attenuation		61	63	65	dB
$A_{\text{BALstep}}$	Step Resolution			1		dB
$E_A$	Attenuation set error	$A_V = 0$ to $-24$ dB	-1	0	1	dB
		$A_V = -24$ to $-63$ dB	-2	0	2	dB
$V_{\text{DC}}$	DC Steps	Adjacent att. steps	-3	0	3	mV

**AUDIO OUTPUTS**

$V_{\text{OCL}}$	Clipping Level	THD = 0.3%	2	2.5		$V_{\text{rms}}$
$R_L$	Output Load Resistance		2			$\text{k}\Omega$
$V_{\text{OUT}}$	DC Voltage Level			4.5		V
$N_{\text{O(OFF)}}$	Output Noise (OFF)	BW=20Hz to 20kHz; All gains 0dB; Output muted flat		5	15	$\mu\text{V}$
				10		$\mu\text{V}$
$N_{\text{O(MUS)}}$	Output Noise (Music)	BW=20Hz to 20kHz; Mode=Music		30		$\mu\text{V}$
$N_{\text{O(PS)}}$	Output Noise(Pseudo Stereo)	BW=20Hz to 20kHz; Mode=Pseudo Stereo		30		$\mu\text{V}$
$A_{\text{MUTE}}$	Output Mute Condition			90		dB
S/N	Signal to Noise Ratio	All gains 0dB; $V_O = 1V_{\text{rms}}$		100		dB
$S_C$	Channel Separation Left/Right			90		dB
d	Distortion	$A_V = 0$ ; $V_I = 1V_{\text{rms}}$		0.01	0.1	%

**BUS INPUT**

$V_{\text{IL}}$	Input Low Voltage				1	V
$V_{\text{IH}}$	Input High Voltage		2.5			V
$I_{\text{IN}}$	Input Current	$V_{\text{IN}} = 0.4\text{V}$	-5		5	$\mu\text{A}$
$V_O$	Output Voltage (ACK)	$I_O = 1.6\text{mA}$		0.4	0.8	V

**I<sup>2</sup>C BUS INTERFACE**

Data transmission from microprocessor to the TDA7443D and vice versa takes place through the 2 wires I<sup>2</sup>C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

**Data Validity**

As shown in fig. 1, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

**Start and Stop Conditions**

As shown in fig. 2 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

**Byte Format**

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

**Acknowledge**

The master (μP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 3). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

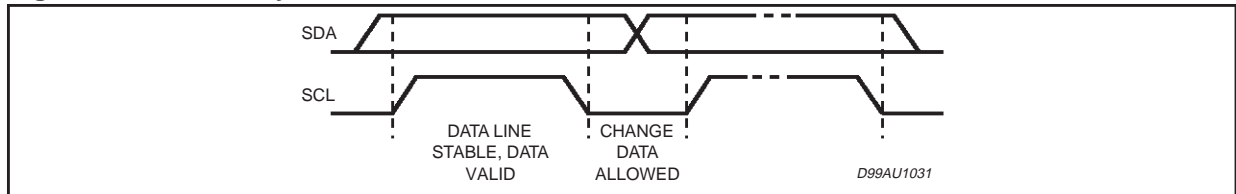
The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

**Transmission without Acknowledge**

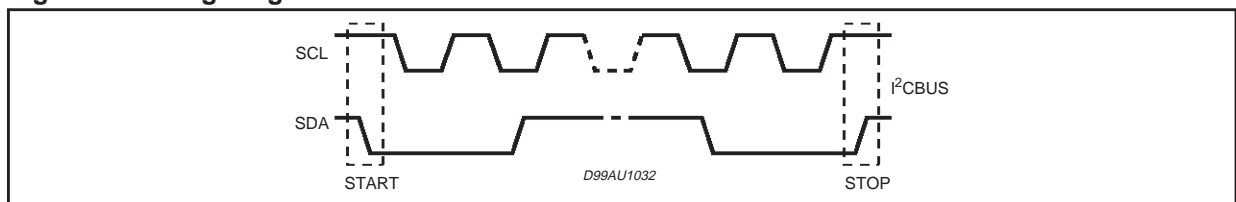
Avoiding to detect the acknowledge of the audio processor, the μP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

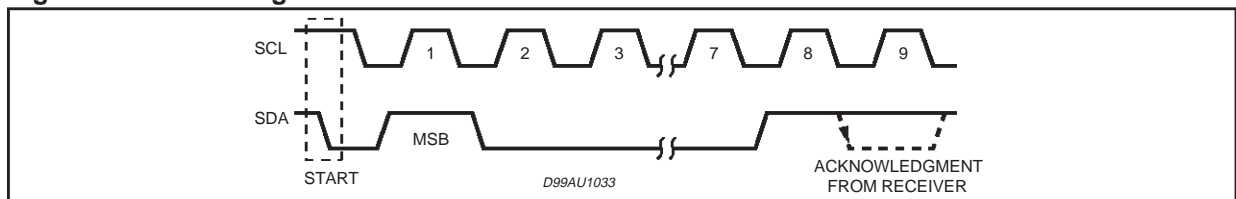
**Figure 1. Data Validity on the I<sup>2</sup>C BUS**



**Figure 2. Timing Diagram of I<sup>2</sup>C BUS**



**Figure 3. Acknowledge on the I<sup>2</sup>C BUS**

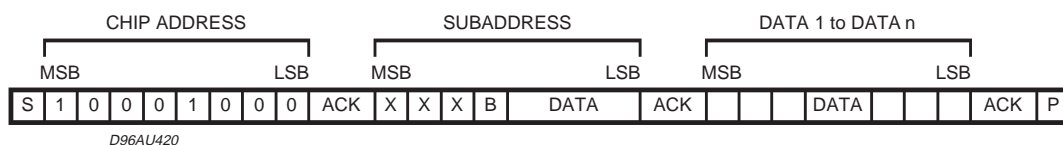


## SOFTWARE SPECIFICATION

### Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7440D address
- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)

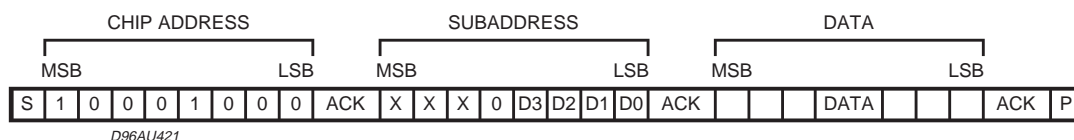


ACK = Acknowledge;    S = Start;    P = Stop;    A = Address;    B = Auto Increment

## EXAMPLES

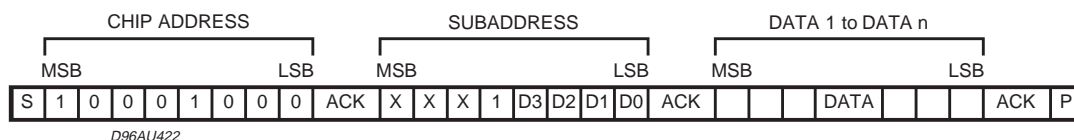
### No Incremental Bus

The TDA7443D receives a start condition, the correct chip address, a subaddress with the B = 0 (no incremental bus), N-data (all these data concern the subaddress selected), a stop condition.



### Incremental Bus

The TDA7443D receives a start conditions, the correct chip address, a subaddress with the B = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "XXX1000" to "XXX1111" of DATA are ignored. The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receives the stop condition.



## TDA7443D

### POWER ON RESET CONDITION

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	0

### DATA BYTES

Address=(HEX) 10001000

FUNCTION SELECTION: First byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	INPUT
X	X	X	B	0	0	0	1	AGC
X	X	X	B	0	0	1	0	SURROUND
X	X	X	B	0	0	1	1	VOLUME
X	X	X	B	0	1	0	0	tone
X	X	X	B	0	1	0	1	BALANCE "L"
X	X	X	B	0	1	1	0	BALANCE "R"

B=1: INCREMENTAL BUS; ACTIVE

B=0: NO INCREMENTAL BUS

X= INDIFFERENT 0/1

### INPUT

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
								<b>INPUT SELECT</b>
					0	0	0	IN1
					0	0	1	IN2
					0	1	0	IN3
					0	1	1	IN4
					1	X	X	IN5
								<b>MUTE</b>
				0				Output Mute OFF
				1				Output Mute ON
								<b>SURROUND IN SELECT</b>
			0					Surround ONI
			1					Mute
								<b>INPUT GAIN</b>
0	0	0						0dB
0	0	1						2dB
0	1	0						4dB
0	1	1						6dB
1	0	0						8dB
1	0	1						10dB
1	1	0						12dB
1	1	1						14dB



## AGC

MSB								LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0		
									<b>AGC MODE</b>
							0	OFF	
							1	ON	
									<b>DETECTOR</b>
						0		OFF	
						1		ON	
									<b>RELEASE CURRENT</b>
					0			OFF	
					1			ON	
									<b>ATTACK TIME</b>
			0	0				ATTACK1	
			0	1				ATTACK2	
			1	0				ATTACK3	
			1	1				ATTACK4	
									<b>TARGET LEVEL</b>
	0	0						TARGET1	
	0	1						TARGET2	
	1	0						TARGET3	
	1	1						TARGET4	
									<b>ZEROCROSS</b>
0								OFF	
1								ON	

## SURROUND

MSB							LSB		SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0		
								<b>SURROUND MODE</b>	
						0		PSEUDO STEREO	
						1		MUSIC	
								<b>EFFECT CONTROL</b>	
		0	0	0	0			-6 dB	
		0	0	0	1			-7 dB	
		0	0	1	0			-8 dB	
		0	0	1	1			-9 dB	
		0	1	0	0			-10 dB	
		0	1	0	1			-11 dB	
		0	1	1	0			-12 dB	
		0	1	1	1			-13 dB	
		1	0	0	0			-14 dB	
		1	0	0	1			-15 dB	
		1	0	1	0			-16 dB	
		1	0	1	1			-17 dB	
		1	1	0	0			-18 dB	
		1	1	0	1			-19 dB	
		1	1	1	0			-20 dB	
		1	1	1	1			-21 dB	
								<b>PHASE SHIFT RESISTOR</b>	
0	0							12 kohm	
0	1							14 kohm	
1	0							18 kohm	
1	1							37 kohm	

## VOLUME

MSB								LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0		
								<b>VOLUME IN SELECT</b>	
						0	0	Surround	
						0	1	Non Surround	
						1	X	Mute	
								<b>1dB STEPS</b>	
			0	0	0			0dB	
			0	0	1			-1dB	
			0	1	0			-2dB	
			0	1	1			-3dB	
			1	0	0			-4dB	
			1	0	1			-5dB	
			1	1	0			-6dB	
			1	1	1			-7dB	
								<b>8dB STEPS</b>	
0	0	0						0dB	
0	0	1						-8dB	
0	1	0						-16dB	
0	1	1						-24dB	
1	0	0						-32dB	
1	0	1						-40dB	
1	1	0						-48dB	
1	1	1						-56dB	

VOLUME=0 to -63dB

TREBLE & BASS

MSB								LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0		
								<b>TREBLE</b>	
				0	0	0	0	-14 dB	
				0	0	0	1	-12 dB	
				0	0	1	0	-10 dB	
				0	0	1	1	-8 dB	
				0	1	0	0	-6 dB	
				0	1	0	1	-4 dB	
				0	1	1	0	-2 dB	
				0	1	1	1	0 dB	
				1	0	0	0	14 dB	
				1	0	0	1	12 dB	
				1	0	1	0	10 dB	
				1	0	1	1	8 dB	
				1	1	0	0	6 dB	
				1	1	0	1	4 dB	
				1	1	1	0	2 dB	
				1	1	1	1	0 dB	
								<b>BASS</b>	
0	0	0	0					-14 dB	
0	0	0	1					-12 dB	
0	0	1	0					-10 dB	
0	0	1	1					-8 dB	
0	1	0	0					-6 dB	
0	1	0	1					-4 dB	
0	1	1	0					-2 dB	
0	1	1	1					0 dB	
1	0	0	0					14 dB	
1	0	0	1					12 dB	
1	0	1	0					10 dB	
1	0	1	1					8 dB	
1	1	0	0					6 dB	
1	1	0	1					4 dB	
1	1	1	0					2 dB	
1	1	1	1					0 dB	

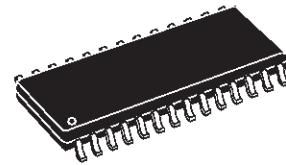
**BALANCE**

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
								<b>1dB STEPS</b>
			0	0	0			0dB
			0	0	1			-1dB
			0	1	0			-2dB
			0	1	1			-3dB
			1	0	0			-4dB
			1	0	1			-5dB
			1	1	0			-6dB
			1	1	1			-7dB
								<b>8dB STEPS</b>
0	0	0						0dB
0	0	1						-8dB
0	1	0						-16dB
0	1	1						-24dB
1	0	0						-32dB
1	0	1						-40dB
1	1	0						-48dB
1	1	1						-56dB

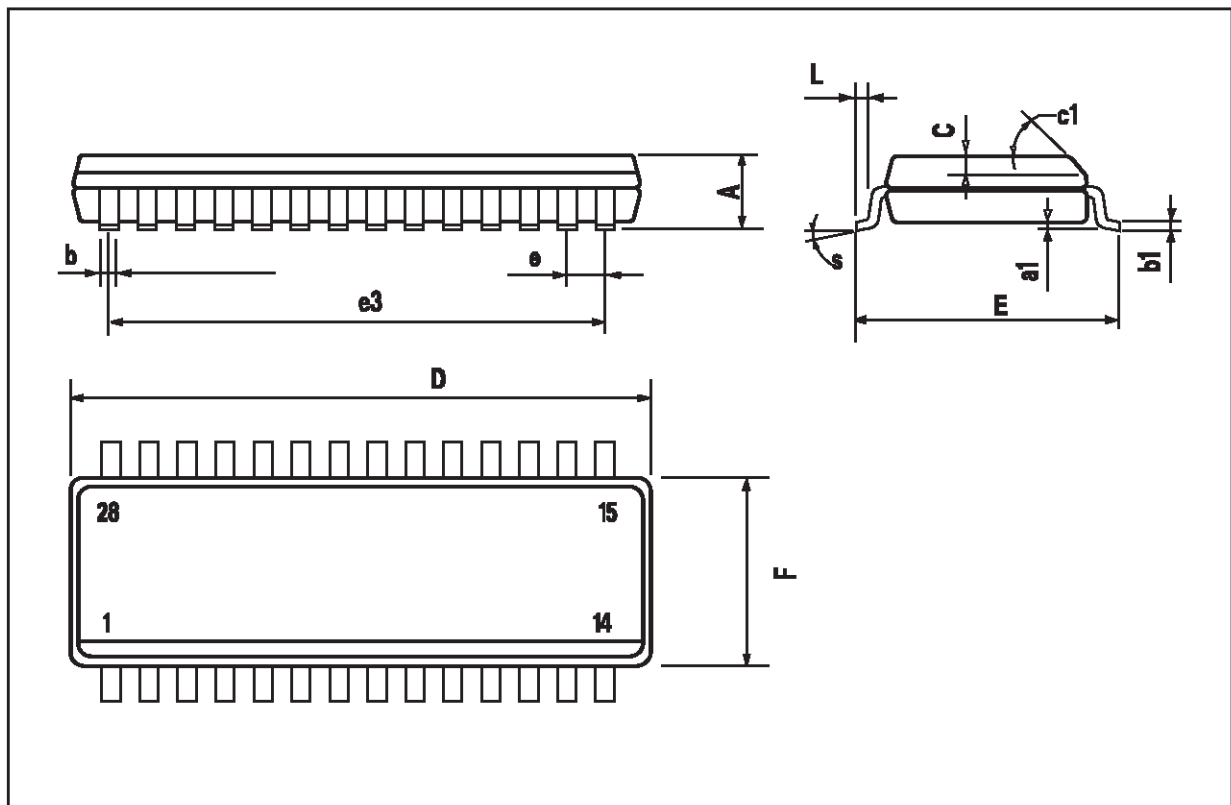
VOLUME=0 to -63dB

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

**OUTLINE AND MECHANICAL DATA**



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