TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WB125FK

Dual Bus Switch

The TC7WB125FK is a low on-resistance, high-speed CMOS 2-bit bus switch. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable (\overline{OE}) is at low level, the switch is on; when at high level, the switch is off.

All inputs are equipped with protector circuits to protect the device from static discharge.

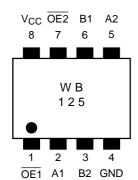
Features

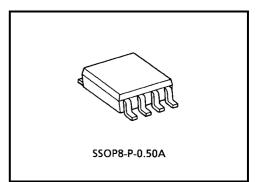
- Operating voltage: $V_{CC} = 4.5 \sim 5.5 V$
- High speed operation: $t_{pd} = 0.25 \text{ ns} (max)$
- Ultra-low on resistance: $R_{ON} = 5 \Omega$ (typ.)
- Electro-static discharge (ESD) performance: ±200 V or more (JEITA)

±2000 V or more (MIL)

- TTL level input (control input)
- Package: US8

Pin Assignment (top view)





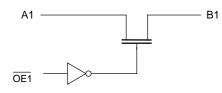
Weight: 0.01 g (typ.)

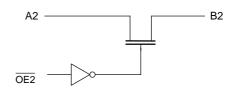
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Truth Table

Inputs	Function
OE	Tunction
L	A port = B port
Н	Disconnect

System Diagram





Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	-0.5~7.0	V
Control pin input voltage	V _{IN}	-0.5~7.0	V
Switch terminal I/O voltage	VS	-0.5~7.0	V
Clump diode current	I _{IK}	-50	mA
Switch I/O current	IS	128	mA
Power dissipation	PD	200	mW
DC V _{CC} /GND current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65~150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	4.5~5.5	V
Control pin input voltage	V _{IN}	0~5.5	V
Switch I/O voltage	VS	0~5.5	V
Operating temperature	T _{opr}	-40~85	°C
Control pin input rise/fall time	dt/dv	0~10	ns/V

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condi	Test Condition		Min	Typ. (Note1)	Max	Unit
		Symbol			V _{CC} (V)	IVIITI			
Control pin input	"H" level	VIH	_		4.5~5.5	2.0	_	_	V
voltage	"L" level	VIL	_		4.5~5.5		_	0.8	v
Input leakage cur	rent	I _{IN}	V _{IN} = 0~5.5 V		4.5~5.5	_	_	±1.0	μA
Power off leakage	e current	IOFF	A, B, $\overline{OE} = 0 \sim 5.5 \text{ V}$		0	_	_	±1.0	μA
Off-state leakage (switch		I _{SZ}	A, B = 0~5.5 V, $\overline{OE} = V_{CC}$		4.5~5.5		_	±1.0	μA
			V _{IS} = 0 V	$I_{IS} = 64 \text{ mA}$	4.5	_	5	7	
ON resistance	(Note2)	R _{ON}	VIS = 0 V	I _{IS} = 30 mA	4.5	_	5	7	Ω
			$V_{IS} = 2.4 \text{ V}, \ I_{IS} = 15 \text{ m}.$	4	4.5		10	15	
Quiescent supply current		Icc	$V_{IN} = V_{CC} \text{ or } GND$ $I_{OUT} = 0$		5.5			10	μA
		ΔI_{CC}	V _{IN} = 3.4 V (one input)		5.5		_	2.5	mA

Note1: The typical values are at $V_{CC} = 5 \text{ V}$, Ta = 25°C.

AC Characteristics (Ta = -40~85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time	t _{pLH}	Figure 1, Figure 2 (Note3)	4.5		0.25	200
(bus to bus)	t _{pHL}	Figure 1, Figure 2 (Note3)	4.5		0.25	ns
Output enable time	t _{pZL}	Figure 1, Figure 3	4.5		4.0	ns
	t _{pZH}		ч.0		ч.0	113
Output disable time	t _{pLZ}	Figure 1, Figure 3	4.5		5.0	ns
	t _{pHZ}		ч.0		0.0	113

Note3: The propagation delay time is calculated by the RC (on-resistance and load capacitance) time constant.

Capacitive Characteristics (Ta = 25°C)

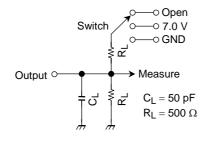
Characteristics	Symbol	Test Condition		V _{CC} (V)	Тур.	Unit
Control pin input capacitance	C _{IN}		(Note4)	5.0	3	pF
Switch terminal capacitance	C _{I/O}	$\overline{OE} = V_{CC}$	(Note4)	5.0	10	pF

Note4: This item is guaranteed by design.

Note2: Apply the specified current to the switch, then measure the voltages on pins A and B. The on-resistance is the lower of the two.

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AC Test Circuit



Parameter	Switch		
t _{pLH} , t _{pHL}	Open		
t _{pLZ} , t _{pZL}	7.0 V		
t _{pHZ} , t _{pZH}	Open		



AC Waveform

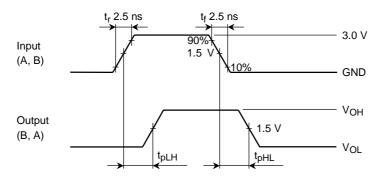
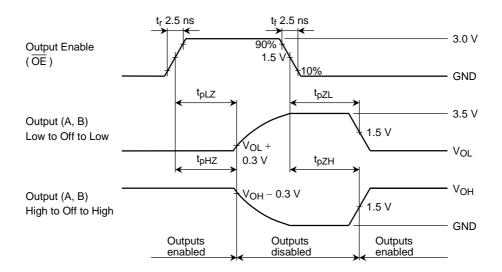
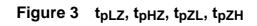


Figure 2 t_{pLH}, t_{pHL}

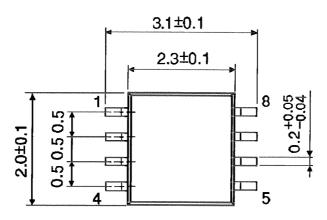


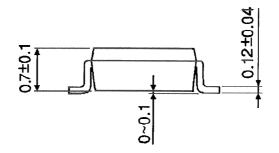


Package Dimensions

SSOP8-P-0.50A

Unit : mm





Weight: 0.01 g (typ.)

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Handbook" etc..

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