TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7MB3251FK

#### 1-of-8 FET Multiplexer/Demultiplexer

The TC7MB3251FK is high-speed CMOS 1-8

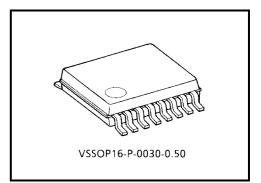
multiplexer/demultiplexer. The low on resistance of the switch allows connections to be made with minimal propagation delay time.

This device is 1 to 8 multiplexer/demultiplexer controlled by the combination of select inputs (S0, S1, S2) and output enable ( $\overline{OE}$ ). The A inputs is connected to the corresponded B1~B8 outputs determined by the combination both the select inputs (S0, S1, S2) and output enable ( $\overline{OE}$ ). When the output enable ( $\overline{OE}$ ) input is held "H" level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

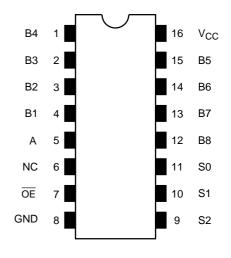
#### Features

- Operating voltage: V<sub>CC</sub> = 4.5~5.5 V
- High speed:  $t_{pd} = 0.25 \text{ ns} (max)$
- Low on resistance:  $R_{ON} = 5 \Omega$  (typ.)
- ESD performance: Machine model > ±200 V Human body model > ±2000 V
- Compatible with TTL outputs (control inputs)
- Package: VSSOP (US16)
- Pin compatible with the 74xx251 type. Functionally equivalent to (FST/CBT) 3251.



Weight: 0.02 g (typ.)

#### Pin Assignment (top view)

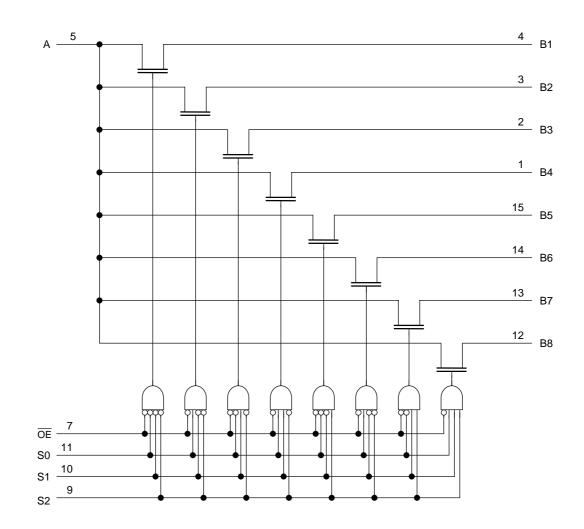


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# **Truth Table**

	Inp	Function		
ŌĒ	S2	S1	S0	Tunction
L	L	L	L	A port = B1 port
L	L	L	Н	A port = B2 port
L	L	Н	L	A port = B3 port
L	L	Н	Н	A port = B4 port
L	н	L	L	A port = B5 port
L	н	L	Н	A port = B6 port
L	н	Н	L	A port = B7 port
L	н	н	Н	A port = B8 port
н	Х	Х	Х	Disconnect

# System Diagram



#### **Maximum Ratings**

Characteristics	Symbol	Rating	Unit
Power supply range	V <sub>CC</sub>	-0.5~7.0	V
DC input voltage	V <sub>IN</sub>	-0.5~7.0	V
DC switch voltage	VS	-0.5~7.0	V
Input diode current	I <sub>IK</sub>	-50	mA
Continuous channel current	IS	128	mA
Power dissipation	PD	180	mW
DC V <sub>CC</sub> /GND current	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA
Storage temperature	T <sub>stg</sub>	-65~150	°C

## **Recommended Operating Conditions**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	4.5~5.5	V
Input voltage ( $\overline{OE}$ , S)	V <sub>IN</sub>	0~5.5	V
Switch voltage	VS	0~5.5	V
Operating temperature	T <sub>opr</sub>	-40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

# **Electrical Characteristics**

## DC Characteristics ( $Ta = -40 \sim 85^{\circ}C$ )

Characteristics		Symbol	Symbol Test Condition			Min	Typ. (Note1)	Max	Unit
		Cymzei			V <sub>CC</sub> (V)				Offic
Input voltage	"H" level	VIH	—		4.5~5.5	2.0	—	_	V
mput voltage	"L" level	VIL	_		4.5~5.5	_	_	0.8	v
Input leakage current ( OE , S)		I <sub>IN</sub>	V <sub>IN</sub> = 0~5.5 V 4.5~		4.5~5.5	_	—	±1.0	μA
Power off leakage current		I <sub>OFF</sub>	A, B, $\overline{OE}$ = 0~5.5 V		0	_	_	±1.0	μA
Off-state leakage current		I <sub>SZ</sub>	A, B = 0~5.5 V, $\overline{OE}$ =	45.5	4.5~5.5			±1.0	μA
(switch off)		ISZ	$A, B = 0 \sim 3.3 \text{ V},  OE = VCC$		4.5~5.5			±1.0	μΛ
ON resistance (Note2)			V <sub>IS</sub> = 0 V	I <sub>IS</sub> = 64 mA	4.5		5	7	
		R <sub>ON</sub>	VIS – U V	I <sub>IS</sub> = 30 mA	4.5	_	5	7	Ω
			$V_{IS} = 2.4 \text{ V}, \ I_{IS} = 15 \text{ m}.$	2.4 V, I <sub>IS</sub> = 15 mA		_	10	15	
Increase in I <sub>CC</sub> per input		ICC	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$		5.5	_	_	10	μA
		$\Delta I_{CC}$	V <sub>IN</sub> = 3.4 V (one input)		5.5		_	2.5	mA

Note 1: Typical values are at  $V_{CC} = 5 V$ , Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40~85°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay time	t <sub>pLH</sub>					
(bus to bus)	t <sub>pHL</sub>	Figure 1, Figure 2 (Note3)	4.5	_	0.25	ns
Propagation delay time	t <sub>pLH</sub>		4.5		6.0	20
(S to bus)	t <sub>pHL</sub>	Figure 1, Figure 2	4.5		6.0	ns
Output enable time	t <sub>pZL</sub>	Figure 1, Figure 3	4.5		5.6	20
( OE to bus)	t <sub>pZH</sub>		4.5	_	5.6	ns
Output enable time	t <sub>pZL</sub>	Figure 1, Figure 3	4.5		5.6	ns
(S to bus)	t <sub>pZH</sub>		4.5		5.0	115
Output disable time	t <sub>pLZ</sub>	Figure 1, Figure 3	4.5		6.4	20
( OE to bus)	t <sub>pHZ</sub>		4.0		0.4	ns
Output disable time	t <sub>pLZ</sub>	Figure 1, Figure 3	4.5		6.4	ns
(S to bus)	t <sub>pHZ</sub>		4.5		0.4	115

Note 3: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

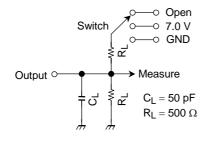
#### **Capacitive Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Control pin input capacitance ( $\overline{\text{OE}}$ , S)	C <sub>IN</sub>	(Note4)	5.0	3	pF
Switch terminal capacitance (B1~8)	C <sub>I/O</sub>	$\overline{OE} = V_{CC}$ (Note4)	5.0	10	pF
Switch terminal capacitance (A)	C <sub>I/O</sub>	$\overline{OE} = V_{CC}$ (Note4)	5.0	59	pF

Note 4: This parameter is guaranteed by design.

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# **AC Test Circuit**



Parameter	Switch		
t <sub>pLH</sub> , t <sub>pHL</sub>	Open		
t <sub>pLZ</sub> , t <sub>pZL</sub>	7.0 V		
t <sub>pHZ</sub> , t <sub>pZH</sub>	Open		



#### **AC Waveform**

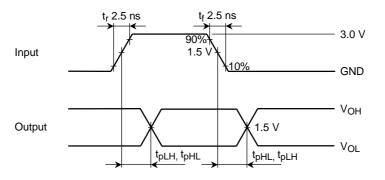
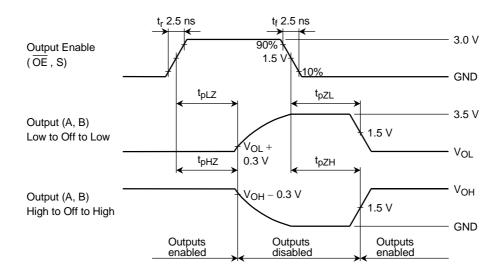
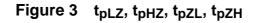


Figure 2  $t_{pLH}, t_{pHL}$ 

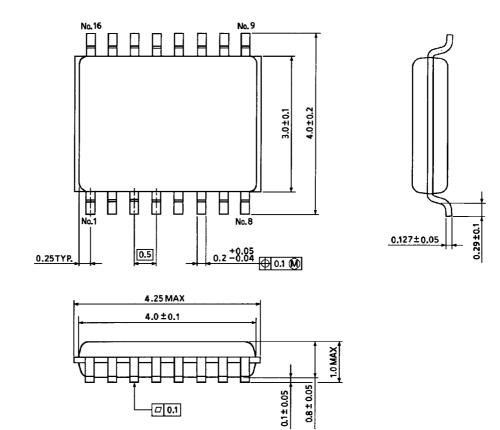




# Package Dimensions

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)

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Handbook" etc..

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