TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74LVX02F,TC74LVX02FN,TC74LVX02FT

#### Quad 2-Input NOR Gate

The TC74LVX02F/ FN/ FT is a high-speed CMOS 2-input NOR gate fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

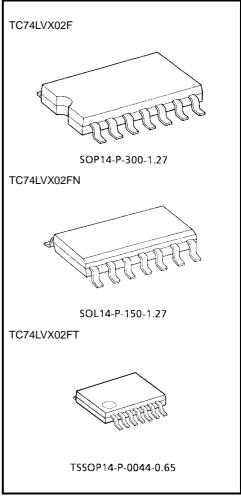
The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

#### **Features**

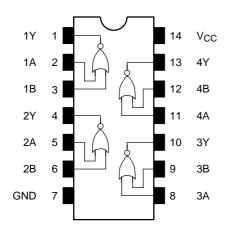
- High-speed:  $t_{pd} = 4.5 \text{ ns (typ.) (V}_{CC} = 3.3 \text{ V})$
- Low-power dissipation:  $I_{CC} = 2 \mu A \text{ (max) (Ta} = 25 ^{\circ}\text{C)}$
- Input voltage level:  $V_{IL} = 0.8 \text{ V (max)} (V_{CC} = 3 \text{ V})$   $V_{IH} = 2.0 \text{ V (min)} (V_{CC} = 3 \text{ V})$
- · Power-down protection provided on all inputs
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Low noise: VOLP = 0.5 V (max)
- Pin and function compatible with 74HC02

Note: xxxFN (JEDEC SOP) is not available in Japan.

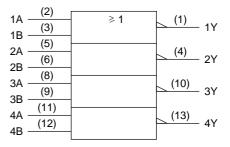


Weight SOP14-P-300-1.27: 0.18 g (typ.) SOL14-P-150-1.27: 0.12 g (typ.) TSSOP14-P-0044-0.65: 0.06 g (typ.)

### Pin Assignment (top view)



### **IEC Logic Symbol**



### **Truth Table**

Inp	Outputs		
Α	В	Υ	
L	L	Н	
L	Н	L	
Н	L	L	
Н	Н	L	

### **Maximum Ratings**

Characteristics	Symbol	Rating	Unit
Supply voltage range	Vcc	-0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
DC output voltage	V <sub>OUT</sub>	$-0.5$ to $V_{CC} + 0.5$	V
Input diode current	I <sub>IK</sub>	-20	mA
Output diode current	lok	±20	mA
DC output current	lout	±25	mA
DC V <sub>CC</sub> /ground current	Icc	±50	mA
Power dissipation	P <sub>D</sub>	180	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

### **Recommended Operating Conditions**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2.0 to 3.6	V
Input voltage	V <sub>IN</sub>	0 to 5.5	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V



#### **Electrical Characteristics**

#### **DC Characteristics**

Characteristics S		Symbol Test Condition		Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
					V <sub>CC</sub> (V) Min Typ. Ma		Max	Min	Max		
				2.0	1.5	_	_	1.5	_		
H-leve	H-level	$V_{IH}$		_	3.0	2.0	_	_	2.0	_	
Input voltage					3.6	2.4	_	_	2.4	_	V
Input voltage					2.0	_	_	0.5	_	0.5	V
L-lev	L-level	$V_{IL}$		_	3.0	_	_	0.8	_	0.8	
					3.6	_	_	0.8	_	0.8	
			H VIN = VIL	$I_{OH} = -50 \mu A$	2.0	1.9	2.0	_	1.9	_	
	H-level	V <sub>OH</sub>		$I_{OH} = -50 \mu A$	3.0	2.9	3.0	_	2.9	_	
				$I_{OH} = -4 \text{ mA}$	3.0	2.58	_	_	2.48	_	V
Output voltage		L-level V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$I_{OL} = 50 \mu A$	2.0	_	0	0.1	_	0.1	V
L-	L-level			$I_{OL} = 50 \mu A$	3.0	_	0	0.1	_	0.1	
				I <sub>OL</sub> = 4 mA	3.0	_	_	0.36	_	0.44	
Input leakage curi	rent	I <sub>IN</sub> V <sub>IN</sub> = 5.5 V or GND		3.6	_	_	±0.1	_	±1.0	μΑ	
Quiescent supply	current	Irrent $I_{CC}$ $V_{IN} = V_{CC}$ or GND		3.6		_	2.0	_	20.0	μΑ	

### AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Тур.	Max	Min	Max	
Propagation delay time	t <sub>pLH</sub>	-	2.7	15		5.9	10.7	1.0	13.5	
				50	_	8.4	14.2	1.0	17.0	ns
	t <sub>pHL</sub>		3.3 ± 0.3	15	_	4.5	6.6	1.0	8.0	115
				50	_	7.0	10.1	1.0	11.5	
Output to output skew	t <sub>osLH</sub>	(Note 1)	2.7	50	_	_	1.5	_	1.5	ns
	t <sub>osHL</sub>		$3.3 \pm 0.3$	50	_	_	1.5	_	1.5	115
Input capacitance	C <sub>IN</sub>			(Note 2)	_	4	10		10	pF
Power dissipation capacitance	C <sub>PD</sub>			(Note 3)	_	15	_	_	_	pF

Note 1: Parameter guaranteed by design.  $(t_{OSLH} = |t_{DLHm} - t_{DLHn}|, \, t_{OSHL} = |t_{DHLm} - t_{DHLn}|)$ 

Note 2: Parameter guaranteed by design.

Note 3: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

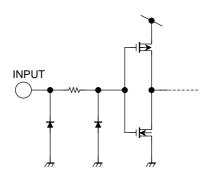
Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$ 

# Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, $C_L = 50$ pF)

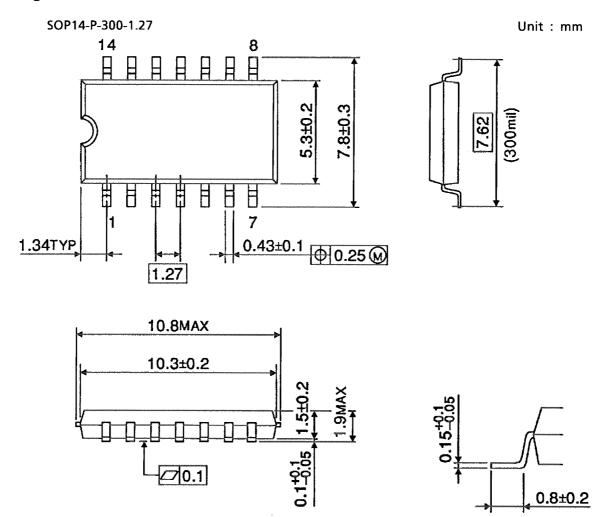
Characteristics		Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Limit	Unit
Quiet output maximum dynamic	V <sub>OL</sub>	V <sub>OLP</sub>	_	3.3	0.3	0.5	٧
Quiet output minimum dynamic	V <sub>OL</sub>	V <sub>OLV</sub>	_	3.3	-0.3	-0.5	٧
Minimum high level dynamic input voltage	V <sub>IH</sub>	$V_{IHD}$	_	3.3	_	2.0	V
Maximum low level dynamic input voltage	V <sub>IL</sub>	V <sub>ILD</sub>	_	3.3	_	0.8	V

# **Input Equivalent Circuit**



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# **Package Dimensions**

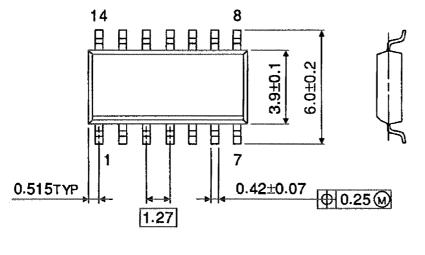


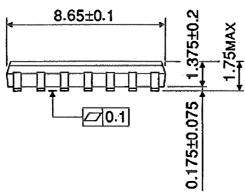
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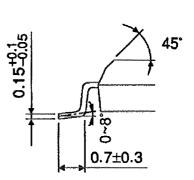
Weight: 0.18 g (typ.)

### **Package Dimensions**









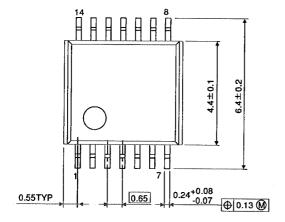
Weight: 0.12 g (typ.)

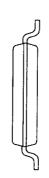
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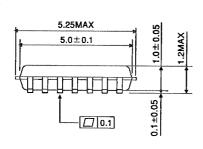
Unit: mm

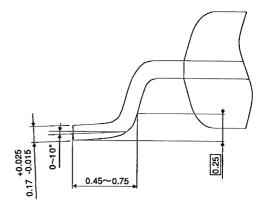
### **Package Dimensions**

TSSOP14-P-0044-0.65









Weight: 0.06 g (typ.)

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