TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

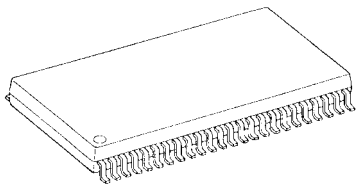
TC74LCX164245FT

16-Bit Dual Supply Bus Transceiver

The TC74LCX164245FT is a dual supply, advanced high-speed CMOS 16-bit dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 5-V bus and a 3.3-V or 2.5-V bus in mixed 5-V/3.3-V or 2.5-V supply systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input. The enable input ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated. The B-port interfaces with the 5-V bus, the A-port with the 3.3-V or 2.5-V bus.



TSSOP48-P-0061-0.50

Weight: 0.25 g (typ.)

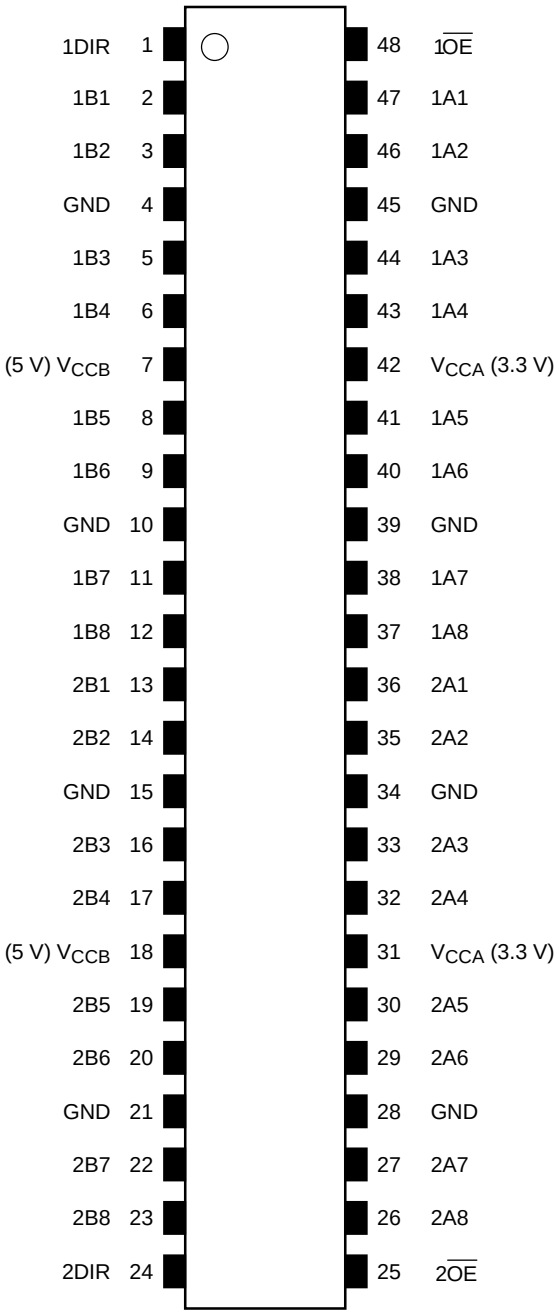
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

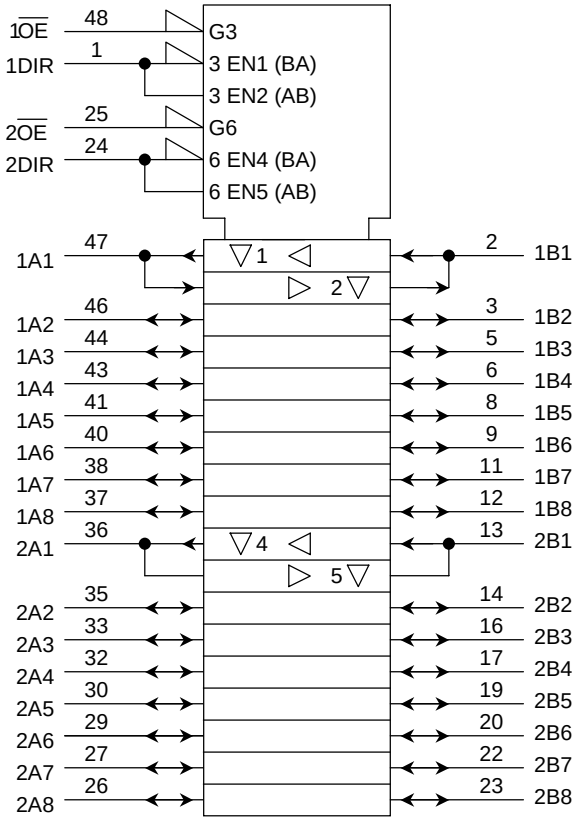
- Bidirectional interface between 5-V and 3.3-V or 2.5-V buses
- High-speed: t_{pd} = 5.8 ns (max)
  (V_{CCB} = 5.0 ± 0.5 V/V_{CCA} = 3.3 ± 0.3 V, Ta = −40 to 85°C)
- Low power dissipation: I_{CC} = 80 μA (max) (Ta = −40 to 85°C)
- Symmetrical ouput impedance: I_{OUTA} = ±24 mA (min)
  I_{OUTB} = ±24 mA (min)
  (V_{CCA} = 3.0 V/V_{CCB} = 4.5 V)
- Power-down protection provided on all inputs and outputs
- Allows A port and V_{CCA} to float simultaneously when $\overline{OE}$ is “H”.
- Latch-up performance: ±500 mA
- Package: TSSOP (thin shrink small outline package)

Note 1: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

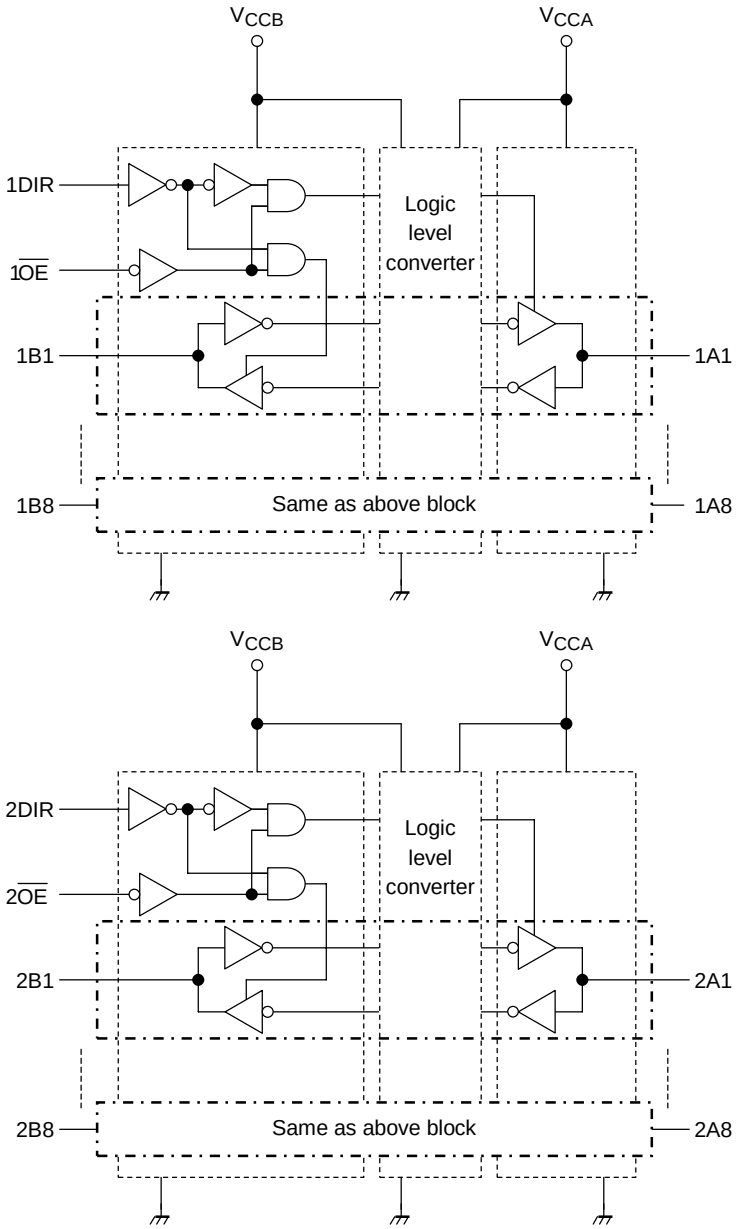
Inputs		Function		Outputs
$1\overline{OE}$	1DIR	Bus 1A1-1A8	Bus 1B1-1B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

Inputs		Function		Outputs
$2\overline{OE}$	2DIR	Bus 2A1-2A8	Bus 2B1-2B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

X: Don’t care

Z: High impedance

Block Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V_{CCB}	−0.5 to 7.0	V
	V_{CCA}	−0.5 to V_{CCB} + 0.5	
DC input voltage (DIR, $\overline{OE}$)	V_{IN}	−0.5 to 7.0	V
DC bus I/O voltage	$V_{I/OB}$	−0.5 to 7.0 (Note 3)	V
		−0.5 to V_{CCB} + 0.5 (Note 4)	
	$V_{I/OA}$	−0.5 to 7.0 (Note 3)	
		−0.5 to V_{CCA} + 0.5 (Note 4)	
Input diode current	I_{IK}	−50	mA
Output diode current	$I_{I/OK}$	±50 (Note 5)	mA
DC output current	I_{OUTB}	±50	mA
	I_{OUTA}	±50	
DC V_{CC}/ground current per supply pin	I_{CCB}	±100	mA
	I_{CCA}	±100	
Power dissipation	P_D	400	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 2: $V_{CCB} > V_{CCA}$
Don't supply a voltage to V_{CCA} terminal when V_{CCB} is in the off-state.

Note 3: OFF state

Note 4: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 5: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Range

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CCB}	4.5 to 5.5	V
	V_{CCA}	2.3 to 3.6	
Input voltage (DIR, $\overline{OE}$)	V_{IN}	0 to 5.5	V
Bus I/O voltage	$V_{I/OB}$	0 to 5.5 (Note 6)	V
		0 to V_{CCB} (Note 7)	
	$V_{I/OA}$	0 to 5.5 (Note 6)	
		0 to V_{CCA} (Note 7)	
Output current	I_{OUTB}	±24 (Note 8)	mA
		±24 (Note 9)	
	I_{OUTA}	±8 (Note 10)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 11)	ns/V

Note 6: OFF state

Note 7: High or low state

Note 8: V_{CCB} = 4.5 to 5.5 V

Note 9: V_{CCA} = 3.0 to 3.6 V

Note 10: V_{CCA} = 2.3 to 2.7 V

Note 11: V_{INB} = 0.8 to 2.0 V, V_{CCB} = 5.0 V
V_{INA} = 0.8 to 2.0 V, V_{CCA} = 3.0 V

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Ta = −40 to 85°C		Unit
						Min	Max	
H-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		5.0 ± 0.5	2.3 to 3.6	2.0	—	V
	V_{IHA}	An		5.0 ± 0.5	2.5 ± 0.2	1.7	—	
				5.0 ± 0.5	3.3 ± 0.3	2.0	—	
L-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		5.0 ± 0.5	2.3 to 3.6	—	0.8	V
	V_{ILA}	An		5.0 ± 0.5	2.5 ± 0.2	—	0.7	
				5.0 ± 0.5	3.3 ± 0.3	—	0.8	
H-level output voltage	V_{OHB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OHB} = −100 μA	5.0 ± 0.5	2.3 to 3.6	V_{CCB} − 0.2	—	V
			I_{OHB} = −24 mA	4.5	2.3 to 3.6	3.7	—	
	V_{OHA}		I_{OHA} = −100 μA	5.0 ± 0.5	2.3 to 3.6	V_{CCA} − 0.2	—	
			I_{OHA} = −24 mA	5.0 ± 0.5	3.0	2.2	—	
			I_{OHA} = − 8 mA	5.0 ± 0.5	2.3	1.8	—	
L-level output voltage	V_{OLB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OLB} = 100 μA	5.0 ± 0.5	2.3 to 3.6	—	0.2	V
			I_{OLB} = 24 mA	4.5	2.3 to 3.6	—	0.44	
	V_{OLA}		I_{OLA} = 100 μA	5.0 ± 0.5	2.3 to 3.6	—	0.2	
			I_{OLA} = 24 mA	5.0 ± 0.5	3.0	—	0.55	
			I_{OLA} = 8 mA	5.0 ± 0.5	2.3	—	0.6	
3-state output OFF state current	I_{OZB}	V_{IN} = V_{IHB} or V_{ILB} $V_{I/OB}$ = 0 to 5.5 V		5.0 ± 0.5	2.3 to 3.6	—	±5.0	μA
	I_{OZA}	V_{IN} = V_{IHB} or V_{ILB} $V_{I/OA}$ = 0 to 5.5 V		5.0 ± 0.5	2.3 to 3.6	—	±5.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 5.5 V		5.5	3.6	—	±5.0	μA
Power-off leakage current	I_{OFF}	V_{INA}/V_{INB} = 5.5 V		0	0	—	10	μA
Quiescent supply current	I_{CCB1}	$V_{I/OA}$ = Open, V_{CCA} = Open V_{INB} = V_{CCB} or GND $\overline{OE}$ = V_{CCB}, DIR = GND		5.5	Open	—	80	μA
	I_{CCB2}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		5.5	3.6	—	80	
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		5.5	3.6	—	50	
	I_{CCTB}	V_{INB} = 3.4 V per input		5.5	2.3 to 3.6	—	2.0	mA
	I_{CCTA}	V_{INA} = V_{CCA} − 0.6 V per input		5.0 ± 0.5	3.6	—	500	μA

AC Characteristics (input: $t_r = t_f = 2.5$ ns, $R_L = 500\ \Omega$)

$V_{CCA} = 3.3 \pm 0.3$ V

Characteristics	Symbol	Test Condition	CL (pF)	V_{CCB} (V)	Ta = −40 to 85°C		Unit
					Min	Max	
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Input: Bn Output: An (DIR = "L")	50	5.0 ± 0.5	1.0	5.8	ns
3-state output enable time ($\overline{OE}$ → An)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	9.0	
3-state output disable time ($\overline{OE}$ → An)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	9.0	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Input: An Output: Bn (DIR = "H")	50	5.0 ± 0.5	1.0	5.8	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	8.9	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	9.0	
Output to output skew	t_{osLH} t_{osHL}	(Note 12)	50	5.0 ± 0.5	—	1.0	ns

Note 12: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCA} = 2.5 \pm 0.2$ V

Characteristics	Symbol	Test Condition	CL (pF)	V_{CCB} (V)	Ta = −40 to 85°C		Unit
					Min	Max	
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Input: Bn Output: An (DIR = "L")	30	5.0 ± 0.5	1.0	8.4	ns
3-state output enable time ($\overline{OE}$ → An)	t_{pZL} t_{pZH}		30	5.0 ± 0.5	1.0	11.0	
3-state output disable time ($\overline{OE}$ → An)	t_{pLZ} t_{pHZ}		30	5.0 ± 0.5	1.0	10.0	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Input: An Output: Bn (DIR = "H")	50	5.0 ± 0.5	1.0	9.0	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	10.5	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	10.3	
Output to output skew	t_{osLH} t_{osHL}	(Note 12)	30 or 50	5.0 ± 0.5	—	1.0	ns

Note 12: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Capacitive Characteristics (Ta = 25°C)

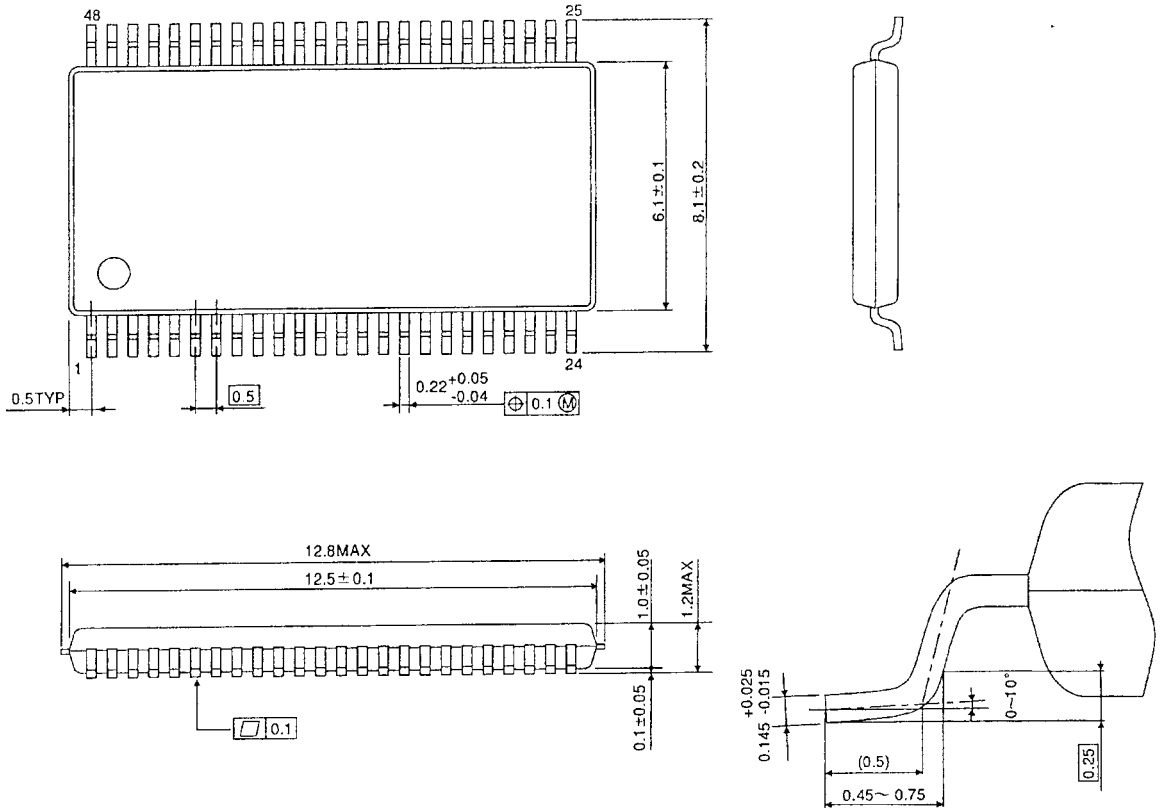
V_{CCB} = 5.0 V

Characteristics	Symbol	Test Circuit	Test Condition	V_{CCA} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	DIR, $\overline{OE}$	2.5, 3.3	7	pF
Output capacitance	$C_{I/O}$	—	An, Bn	2.5, 3.3	8	pF
Power dissipation capacitance (Note 13)	C_{PDA}	—	A ⇒ B (DIR = "H")	2.5, 3.3	2	pF
			B ⇒ A (DIR = "L")	2.5, 3.3	26	
	C_{PDB}	—	A ⇒ B (DIR = "H")	2.5, 3.3	36	
			B ⇒ A (DIR = "L")	2.5, 3.3	4	

Note 13: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16$ (per bit)

Package Dimensions

TSSOP48-P-0061-0.50 Unit : mm



Weight: 0.25 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.