TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX16646AFT

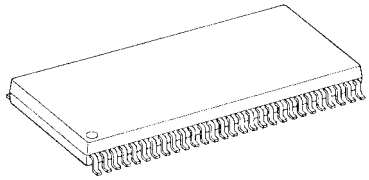
Low-Voltage 16-Bit Bus Transceiver/Register with 5-V Tolerant Inputs and Outputs

The TC74LCX16646AFT is a high-performance CMOS 16-bit bus transceiver/register. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

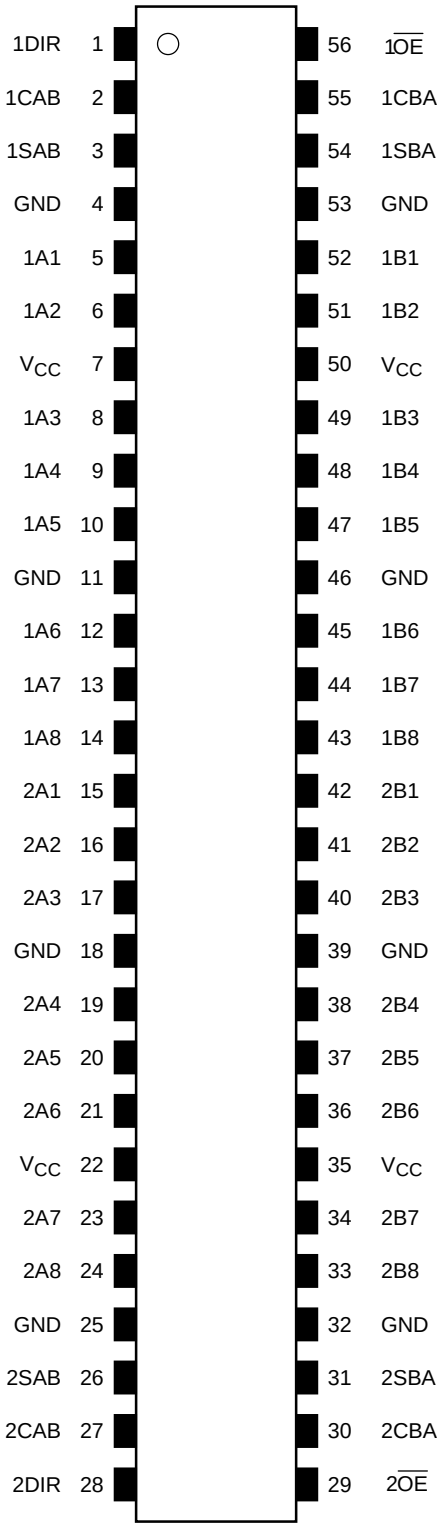
Weight: 0.25 g (typ.)

Features

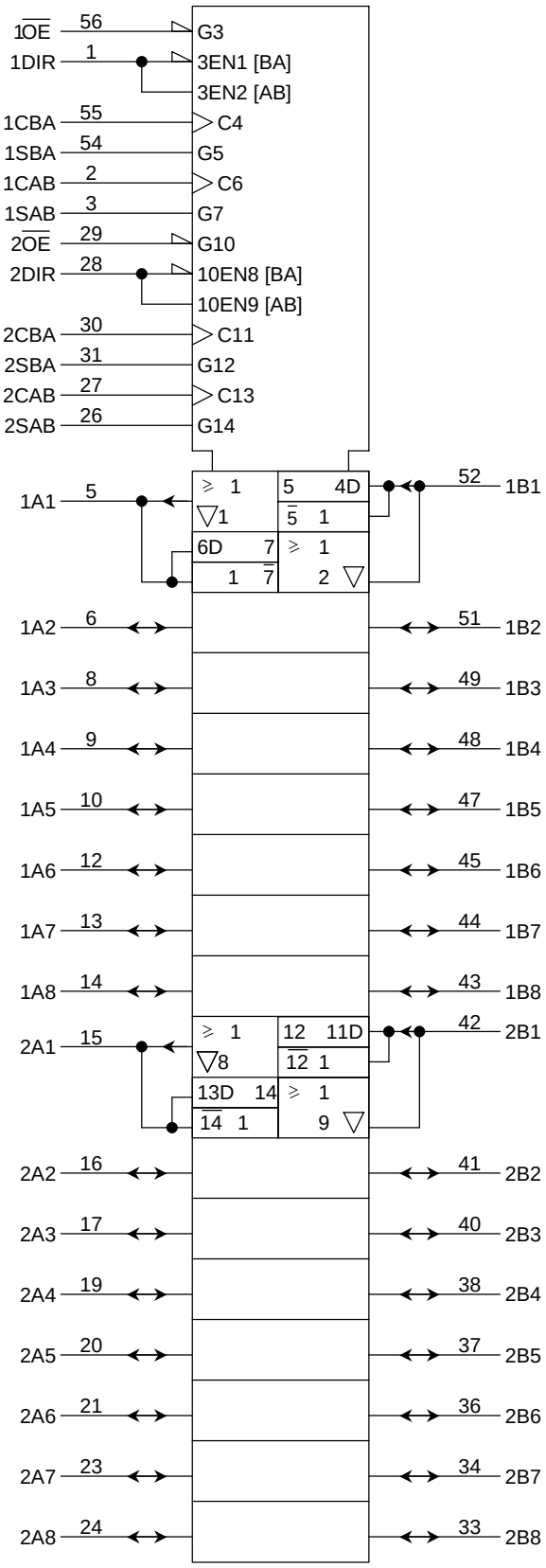
- Low-voltage operation: V_{CC} = 2.0 to 3.6 V
- High-speed operation: t_{pd} = 6.0 ns (max) (V_{CC} = 3.0 to 3.6 V)
- Ouput current: $|I_{OH}|/I_{OL}$ = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance: ±500 mA
- Package: TSSOP (thin shrink small outline package)
- Bidirectional interface between 5.0 V and 3.3 V signals
- Power-down protection provided on all inputs and outputs

Note 1: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input levels fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Control Inputs						Bus		Function
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A	B	
H	X	X*	X*	X	X	Input	Input	The output functions of A and B busses are disabled.
						Z	Z	
		↑	↑	X	X	X	X	Both A and B busses are used as inputs to the internal flip-flops. Data on the bus will be stored on the rising edge of the clock.
L	H	X*	X*	L	X	Input	Output	The data on the A bus are displayed on the B bus.
						L	L	
						H	H	
		↑	X*	L	X	L	L	The data on the A bus are displayed on the B bus, and are stored into the A storage flip-flops on the rising edge of CAB.
						H	H	
		X*	X*	H	X	X	Qn	The data in the A storage flop-flops are displayed on the B bus.
		↑	X*	H	X	L	L	The data on the A bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B bus.
						H	H	
L	L	X*	X*	X	L	Output	Input	The data on the B bus are displayed on the A bus.
						L	L	
						H	H	
		X*	↑	X	L	L	L	The data on the B bus are displayed on the A bus, and are stored into the B storage flip-flops on the rising edge of CBA.
						H	H	
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A bus.
		X*	↑	X	H	L	L	The data on the B bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A bus.
						H	H	

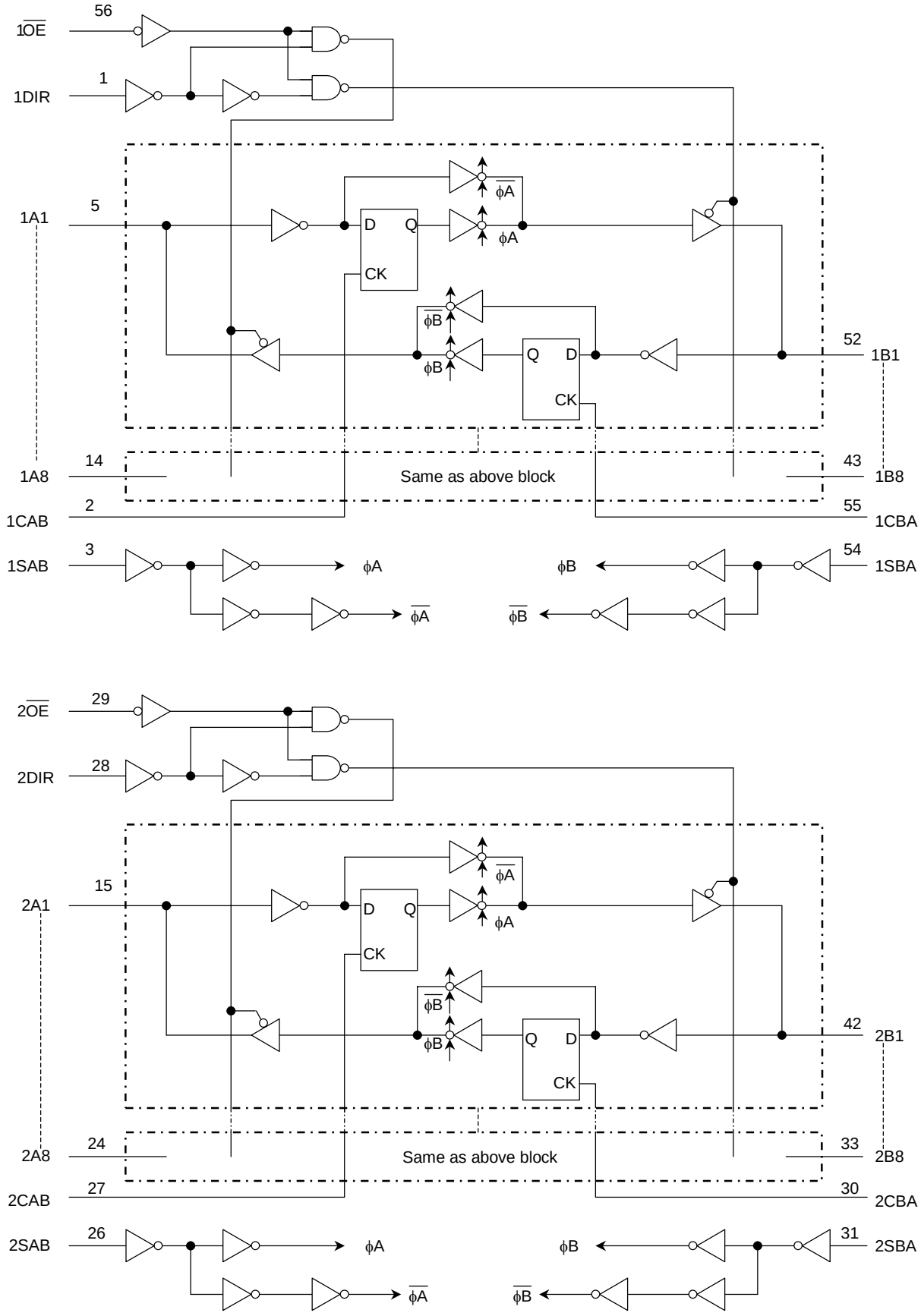
X: Don't care

Z: High impedance

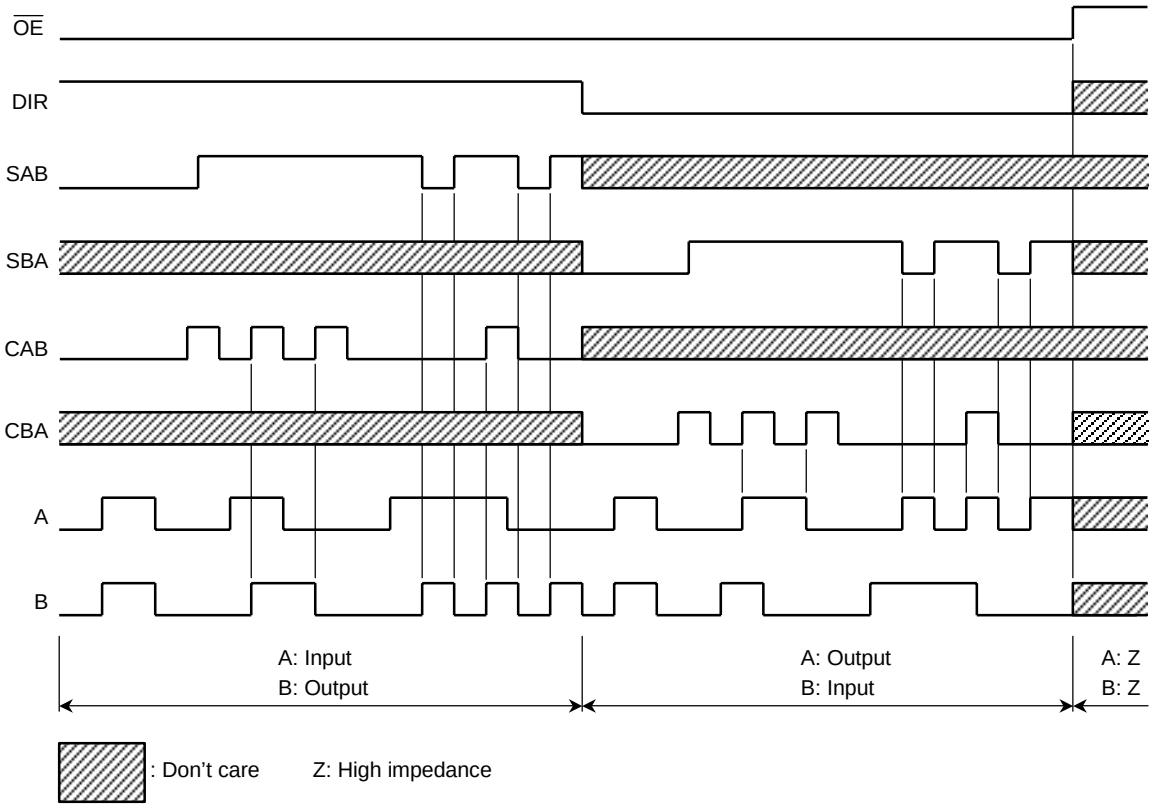
Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

*: The clocks are not internally with either $\overline{OE}$ or DIR.
Therefore, data on the A and/or B busses may be clocked into the storage flip-flops at any time.

System Diagram



Timing Chart



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 7.0	V
DC input voltage (DIR, $\overline{OE}$, CAB, CBA, SAB, SBA)	V_{IN}	−0.5 to 7.0	V
DC bus I/O voltage	$V_{I/O}$	−0.5 to 7.0 (Note 2)	V
		−0.5 to V_{CC} + 0.5 (Note 3)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 4)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	400	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 2: Output in OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0 to 3.6	V
		1.5 to 3.6 (Note 5)	
Input voltage (DIR, $\overline{OE}$, CAB, CBA, SAB, SBA)	V_{IN}	0 to 5.5	V
Bus I/O voltage	$V_{I/O}$	0 to 5.5 (Note 6)	V
		0 to V_{CC} (Note 7)	
Output current	I_{OH}/I_{OL}	±24 (Note 8)	mA
		±12 (Note 9)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 10)	ns/V

Note 5: Data retention only

Note 6: Output in OFF state

Note 7: High or low state

Note 8: V_{CC} = 3.0 to 3.6 V

Note 9: V_{CC} = 2.7 to 3.0 V

Note 10: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = −40 to 85°C)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V_{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7 to 3.6	V_{CC} − 0.2	—	V
				I_{OH} = −12 mA	2.7	2.2	—	
				I_{OH} = −18 mA	3.0	2.4	—	
				I_{OH} = −24 mA	3.0	2.2	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 16 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I_{IN}	V_{IN} = 0 to 5.5 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 5.5 V		2.7 to 3.6	—	±5.0	μA
Power-off leakage current		I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.7 to 3.6	—	20.0	μA
			V_{IN}/V_{OUT} = 3.6 to 5.5 V		2.7 to 3.6	—	±20.0	
Increase in Icc per input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7 to 3.6	—	500	

AC Characteristics (Ta = –40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Maximum clock frequency	f_{max}	Figure 1, Figure 2	2.7	—	—	MHz
			3.3 ± 0.3	170	—	
Propagation delay time (An, Bn-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	2.7	—	6.6	ns
			3.3 ± 0.3	1.5	6.0	
Propagation delay time (CAB, CBA-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 5	2.7	—	8.3	ns
			3.3 ± 0.3	1.5	7.5	
Propagation delay time (SAB, SBA-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	2.7	—	8.3	ns
			3.3 ± 0.3	1.5	7.5	
Output enable time ($\overline{OE}$, DIR-An, Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3, Figure 4	2.7	—	8.3	ns
			3.3 ± 0.3	1.5	7.5	
Output disable time ($\overline{OE}$, DIR-An, Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3, Figure 4	2.7	—	8.3	ns
			3.3 ± 0.3	1.5	7.5	
Minimum pulse width	t_W (H) t_W (L)	Figure 1, Figure 5	2.7	4.0	—	ns
			3.3 ± 0.3	3.0	—	
Minimum setup time	t_s	Figure 1, Figure 5	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum hold time	t_h	Figure 1, Figure 5	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 11)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

Note 11: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics
(Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500$ Ω)

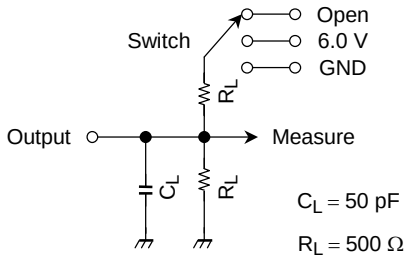
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
Quiet output minimum dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	DIR, $\overline{OE}$, CAB, CBA, SAB, SBA	3.3	7	pF
Bus input capacitance	$C_{I/O}$	An, Bn	3.3	8	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note 12)	3.3	25	pF

Note 12: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16$ (per bit)

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V
t_{pHZ}, t_{pZH}	GND
t_w, t_s, t_h, f_{max}	Open

Figure 1

AC Waveform

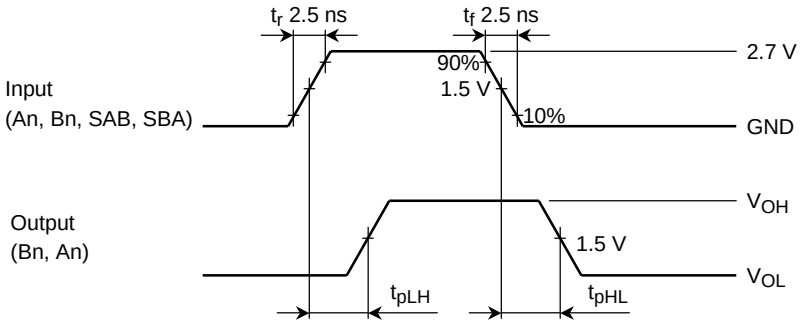


Figure 2 t_{pLH}, t_{pHL}

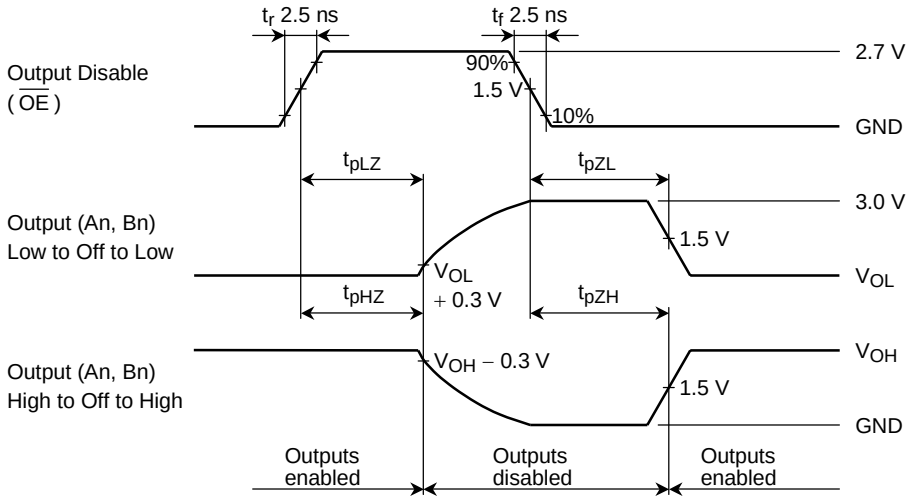


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

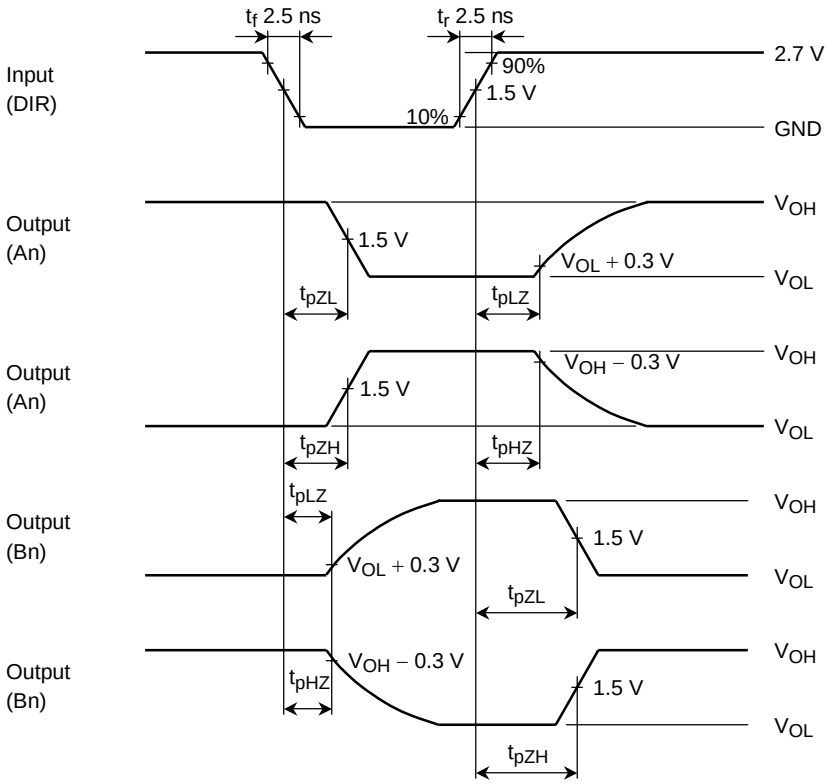


Figure 4 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

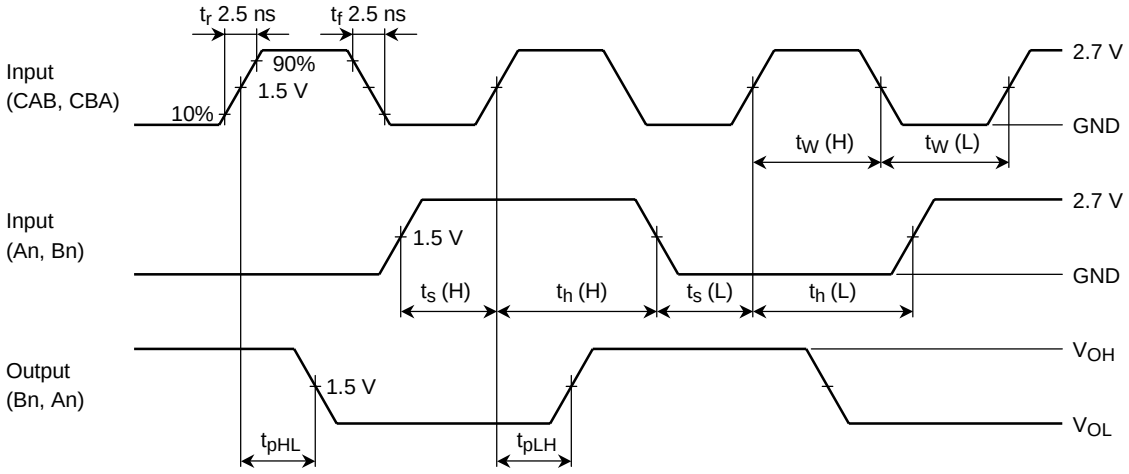
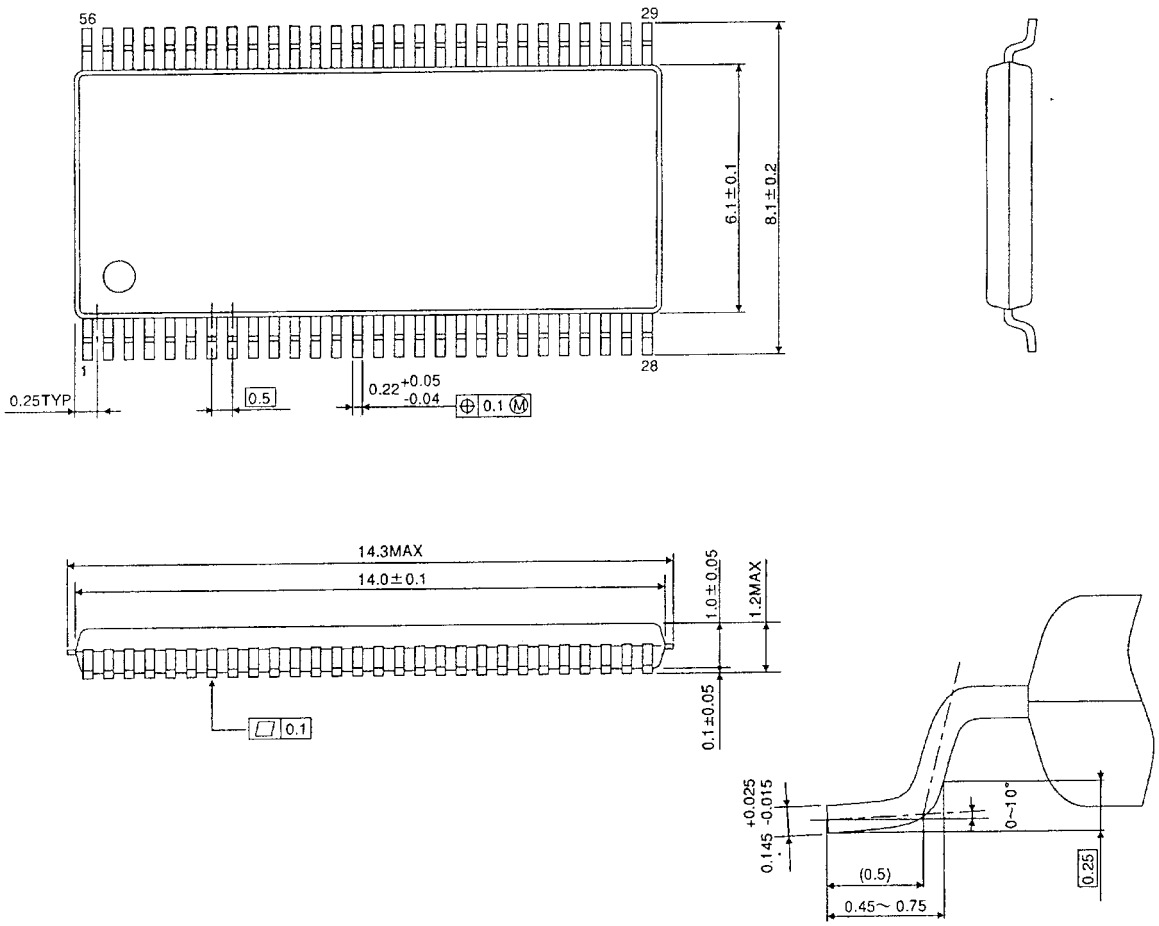


Figure 5 t_{pLH}, t_{pHL}, t_W, t_S, t_h

Package Dimensions

TSSOP56-P-0061-0.50 Unit : mm



Weight: 0.25 g (typ.)

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