TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX16245AFT

Low-Voltage 16-Bit Bus Transceiver with 5-V Tolerant Inputs and Outputs

The TC74LCX16245AFT is a high-performance CMOS 16-bit bus transceiver. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

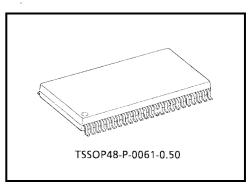
The device is designed for low-voltage $(3.3 \text{ V}) \text{ V}_{CC}$ applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This 16-bit bus transceiver is controlled by direction control (DIR) inputs and output enable (\overline{OE}) inputs which are common to each byte. It can be used as two 8-bit transceiver or one 16-bit transceiver. The direction of data transmission is determined by the level of the DIR inputs. The \overline{OE} inputs can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

Features

- Low-voltage operation: V_{CC} = 2.0 to 3.6 V
- High-speed operation: $t_{pd} = 5.2 \text{ ns} (max) (V_{CC} = 3.0 \text{ to } 3.6 \text{ V})$
- Ouput current: $|I_{OH}|/I_{OL} = 24 \text{ mA} (\text{min}) (V_{CC} = 3.0 \text{ V})$
- Latch-up performance: ±500 mA
- Package: TSSOP (thin shrink small outline package)
- Bidirectional interface between 5.0 V and 3.3 V signals
- Power-down protection provided on all inputs and outputs
 - Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result. All floating (high impedance) bus pins must have their input level fixed by means of pull-up or pull-down resistors.

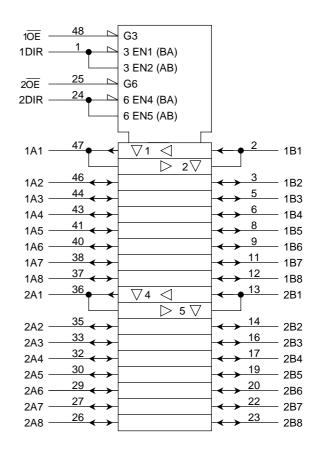




Pin Assignment (top view)

			1	
1DIR	1	\bigcirc	48	10E
1B1	2		47	1A1
1B2	3		46	1A2
GND	4		45	GND
1B3	5		44	1A3
1B4	6		43	1A4
V _{CC}	7		42	V _{CC}
1B5	8		41	1A5
1B6	9		40	1A6
GND	10		39	GND
1B7	11		38	1A7
1B8	12		37	1A8
2B1	13		36	2A1
2B2	14		35	2A2
GND	15		34	GND
2B3	16		33	2A3
2B4	17		32	2A4
V _{CC}	18		31	V _{CC}
2B5	19		30	2A5
2B6	20		29	2A6
GND	21		28	GND
2B7	22		27	2A7
2B8	23		26	2A8
2DIR	24		25	20E
			I	

IEC Logic Symbol



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Truth Table

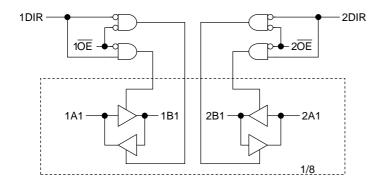
Inputs		Function		
10E	1DIR	Bus 1A1-1A8	Bus 1B1-1B8	Outputs
L	L	Output	Input	A = B
L	н	Input	Output	B = A
Н	Х	Z		Z

Inputs		Function		
20E	2DIR	Bus 2A1-2A8	Bus 2B1-2B8	Outputs
L	L	Output	Input	A = B
L	Н	Input	Output	B = A
Н	Х	Z		Z

X: Don't care

Z: High impedance

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	-0.5 to 7.0	V
DC input voltage (DIR, OE)	V _{IN}	-0.5 to 7.0	V
		-0.5 to 7.0 (Note 1)	
DC bus I/O voltage	V _{I/O}	-0.5 to V _{CC} + 0.5	V
		(Note 2)	
Input diode current	IIK	-50	mA
Output diode current	IOK	±50 (Note 3)	mA
DC output current	IOUT	±50	mA
Power dissipation	PD	400	mW
DC V _{CC} /ground current per supply pin	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Output in OFF state

Note 2: High or low state. IOUT absolute maximum rating must be observed.

Note 3: $V_{OUT} < GND, V_{OUT} > V_{CC}$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V _{CC}	2.0 to 3.6		
Tower supply voltage	v CC	1.5 to 3.6 (Note 4)	V	
Input voltage (DIR, OE)	V _{IN}	0 to 5.5	V	
Bus I/O voltage	V _{I/O}	0 to 5.5 (Note 5)	V	
Bus i/O voltage	v I/O	0 to V _{CC} (Note 6)	v	
Output current	I _{OH} /I _{OI}	±24 (Note 7)	mA	
Output current	'OH/'OL	±12 (Note 8)	IIIA	
Operating temperature	T _{opr}	-40 to 85	°C	
Input rise and fall time	dt/dv	0 to 10 (Note 9)	ns/V	

Note 4: Data retention only

Note 5: Output in OFF state

Note 6: High or low state

Note 7: $V_{CC} = 3.0$ to 3.6 V

Note 8: $V_{CC} = 2.7$ to 3.0 V

Note 9: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC Characteristics (Ta = -40 to 85° C)

Characte	ristics	Symbol	Test (Condition	V _{CC} (V)	Min	Max	Unit
lanut velte en	H-level	VIH			2.7 to 3.6	2.0		V
Input voltage	L-level	VIL			2.7 to 3.6		0.8	V
				I _{OH} = -100 μA	2.7 to 3.6	V _{CC} - 0.2	_	
	H-level	VOH	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -12 mA	2.7	2.2		
		-		I _{OH} = -18 mA	3.0	2.4	_	
Output voltage				I _{OH} = -24 mA	3.0	2.2	_	V
		(o))/	V _{OL} V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7 to 3.6	_	0.2	
	L-level			I _{OL} = 12 mA	2.7	_	0.4	
	L-level	VOL		I _{OL} = 16 mA	3.0	_	0.4	
				I _{OL} = 24 mA	3.0	_	0.55	
Input leakage curre	nt	I _{IN}	$V_{IN} = 0$ to 5.5 V		2.7 to 3.6	_	±5.0	μA
3-state output OFF	state current	I _{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = 0 \text{ to } 5.5 \text{ V}$		2.7 to 3.6		±5.0	μA
Power-off leakage	current	IOFF	$V_{IN}/V_{OUT} = 5.5 V$		0		10.0	μA
	urroot		$V_{IN} = V_{CC}$ or GND		2.7 to 3.6		20.0	
Quiescent supply c	uneni	ICC	$V_{IN}/V_{OUT} = 3.6 \text{ to } 5.5$	5 V	2.7 to 3.6		±20.0	μA
Increase in Icc per	input	ΔI_{CC}	$V_{IH} = V_{CC} - 0.6 V$		2.7 to 3.6	_	500	

AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time	t _{pLH}	Figure 1, Figure 2	2.7	_	6.2	ns
r topagation delay time	t _{pHL}		$\textbf{3.3}\pm\textbf{0.3}$	1.5	5.2	115
3-state output enable time	t _{pZL}	Figure 1, Figure 3	2.7	_	7.5	ns
	t _{pZH}		$\textbf{3.3}\pm\textbf{0.3}$	1.5	6.5	115
3-state output disable time	t _{pLZ}	Figure 1, Figure 3	2.7	_	7.0	ns
	t _{pHZ}		$\textbf{3.3}\pm\textbf{0.3}$	1.5	6.0	115
	t _{osLH}	(Note 10)	2.7	_	_	ns
Output to output skew	t _{osHL}		$\textbf{3.3}\pm\textbf{0.3}$	_	1.0	115

Note 10: Parameter guaranteed by design.

 $(t_{OSLH} = |t_{pLHm} - t_{pLHn}|, t_{OSHL} = |t_{pHLm} - t_{pHLn}|)$

Dynamic Switching Characteristics (Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Input capacitance	C _{IN}	_	3.3	7	pF
Bus input capacitance	C _{I/O}		3.3	8	pF
Power dissipation capacitance	C _{PD}	$f_{IN} = 10 \text{ MHz}$ (Note	1) 3.3	25	pF

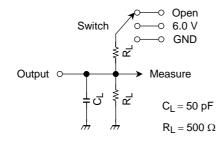
Note 11: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$

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AC Test Circuit



Parameter	Switch
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0 V
t _{pHZ} , t _{pZH}	GND



AC Waveform

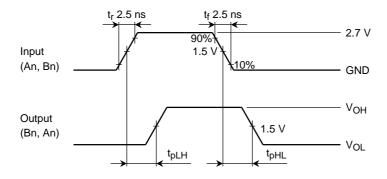


Figure 2 t_{pLH}, t_{pHL}

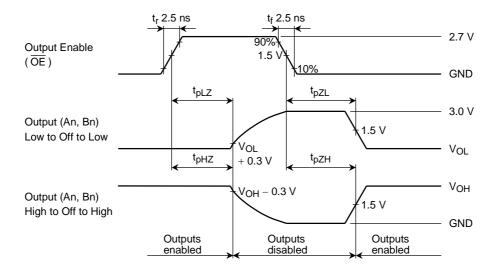
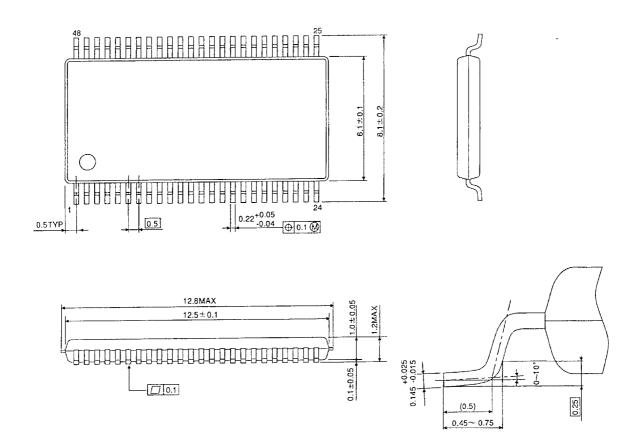


Figure 3 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

Package Dimensions

TSSOP48-P-0061-0.50

Unit : mm



Weight: 0.25 g (typ.)

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