

**TC74AC10P, TC74AC10F, TC74AC10FN**

**TRIPLE 3-INPUT NAND GATE**

The TC74AC10 is an advanced high speed CMOS 3-INPUT NAND GATE fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

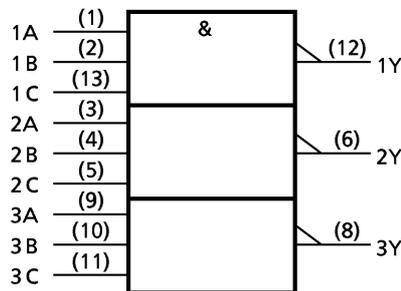
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

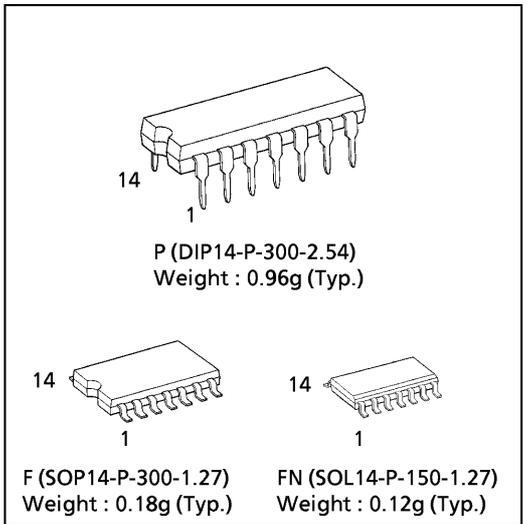
**FEATURES :**

- High Speed..... $t_{pd} = 5.0ns$ (typ.) at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at  $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 24mA$ (Min.)  
 Capability of driving  $50\Omega$  transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (opr) = 2V \sim 5.5V$
- Pin and Function Compatible with 74F10

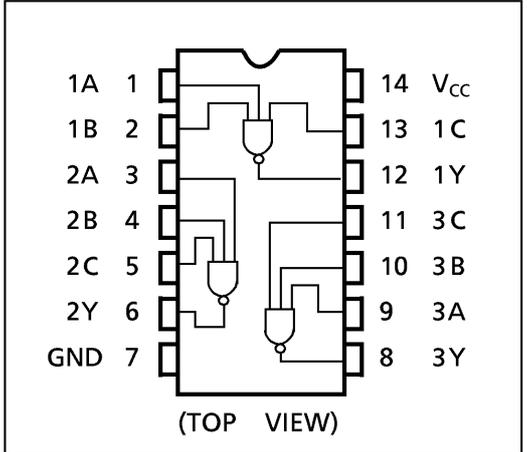
**IEC LOGIC SYMBOL**



(Note) The JEDEC SOP (FN) is not available in Japan.



**PIN ASSIGNMENT**



**TRUTH TABLE**

A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

X : Don't Care

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V <sub>CC</sub>	-0.5~7.0	V
DC Input Voltage	V <sub>IN</sub>	-0.5~V <sub>CC</sub> +0.5	V
DC Output Voltage	V <sub>OUT</sub>	-0.5~V <sub>CC</sub> +0.5	V
Input Diode Current	I <sub>IK</sub>	± 20	mA
Output Diode Current	I <sub>OK</sub>	± 50	mA
DC Output Current	I <sub>OUT</sub>	± 50	mA
DC V <sub>CC</sub> /Ground Current	I <sub>CC</sub>	± 100	mA
Power Dissipation	P <sub>D</sub>	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T <sub>stg</sub>	-65~150	°C

\*500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V <sub>CC</sub>	2.0~5.5	V
Input Voltage	V <sub>IN</sub>	0~V <sub>CC</sub>	V
Output Voltage	V <sub>OUT</sub>	0~V <sub>CC</sub>	V
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Input Rise and Fall Time	dt / dV	0~ 100 (V <sub>CC</sub> = 3.3 ± 0.3V) 0~ 20 (V <sub>CC</sub> = 5 ± 0.5V)	ns / V

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V <sub>IH</sub>		2.0	1.50	—	—	1.50	—	V	
			3.0	2.10	—	—	2.10	—		
			5.5	3.85	—	—	3.85	—		
Low - Level Input Voltage	V <sub>IL</sub>		2.0	—	—	0.50	—	0.50	V	
			3.0	—	—	0.90	—	0.90		
			5.5	—	—	1.65	—	1.65		
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	2.0	1.9	2.0	—	1.9	V	
				3.0	2.9	3.0	—	2.9		—
			I <sub>OH</sub> = -4mA I <sub>OH</sub> = -24mA I <sub>OH</sub> = -75mA*	4.5	4.4	4.5	—	4.4		—
				5.5	—	—	—	—		—
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub>	I <sub>OL</sub> = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 12mA I <sub>OL</sub> = 24mA I <sub>OL</sub> = 75mA*	4.5	—	—	0.36	—	0.44	
				5.5	—	—	—	—	1.65	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0		

\* : This spec indicates the capability of driving 50Ω transmission lines.  
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$  ,  $R_L = 500\ \Omega$  , Input  $t_r = t_f = 3\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time	$t_{pLH}$ $t_{pHL}$		3.3 ± 0.3	—	7.6	13.0	1.0	15.0	ns
			5.0 ± 0.5	—	6.1	8.6	1.0	9.9	
Input Capacitance	C <sub>IN</sub>		—	5	10	—	10	pF	
Power Dissipation Capacitance	C <sub>PD</sub> (1)		—	70	—	—	—		

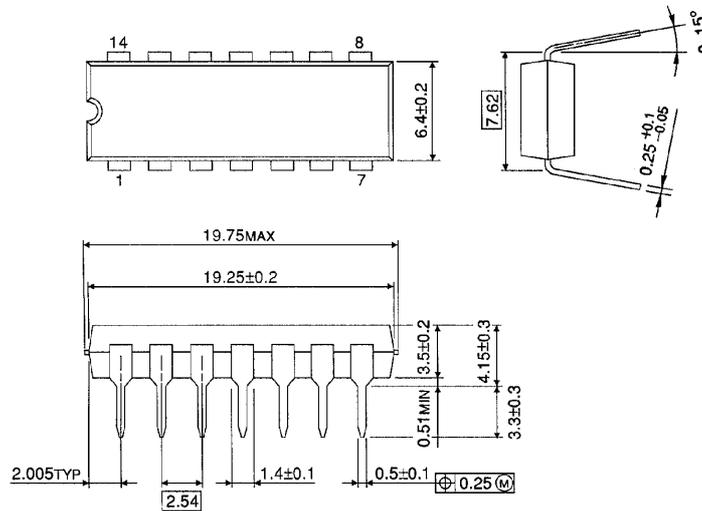
Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(\text{opr.})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 3 \text{ (per Gate)}$$

**DIP 14PIN PACKAGE DIMENSIONS (DIP14-P-300-2.54)**

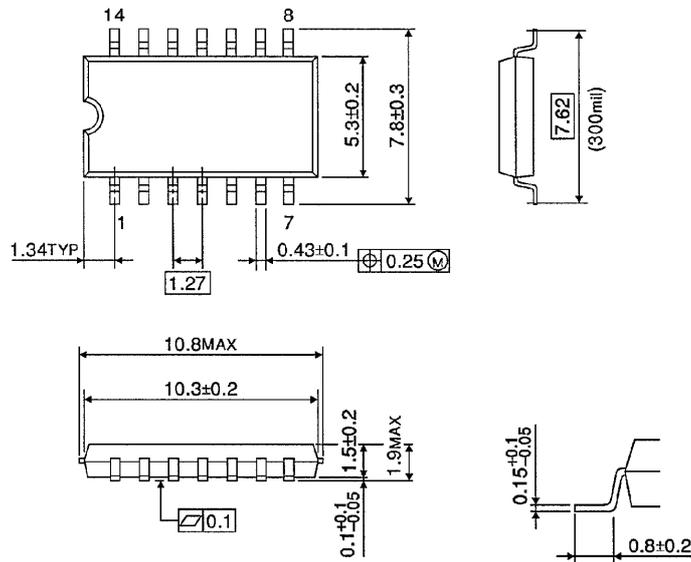
Unit in mm



Weight : 0.96g (Typ.)

**SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)**

Unit in mm

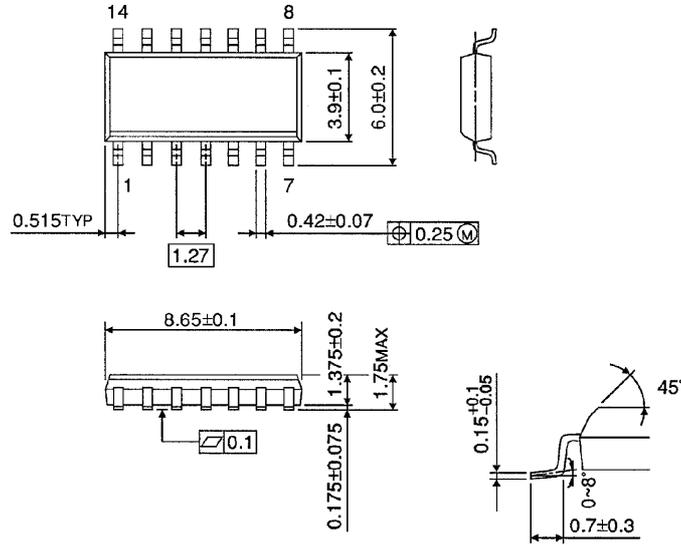


Weight : 0.18g (Typ.)

**SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOL14-P-150 -1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

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