TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74AC109P, TC74AC109F, TC74AC109FN

DUAL J – $\overline{K}$ FLIP FLOP WITH PRESET AND CLEAR

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74AC109 is an advanced high speed CMOS DUAL J-$\overline{K}$ FLIP FLOP fabricated with silicon gate and double - layer metal wiring C^2MOS technology.

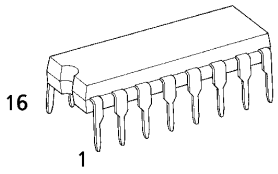
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and $\overline{K}$ input this device changes state on positive going transition of the clock pulse. $\overline{CLEAR}$ and $\overline{PRESET}$ are independent of the clock and accomplished by a low logic level on the corresponding input.

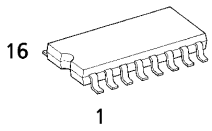
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

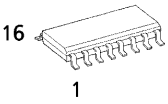
- High Speed ····· f_{MAX} = 200MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.)at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr) = 2V ~ 5.5V
- Pin and Function Compatible with 74F109



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

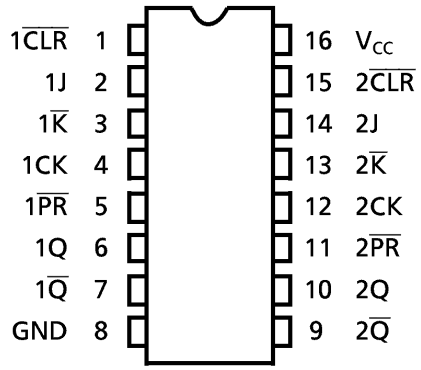


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



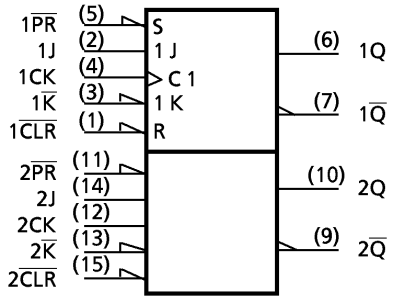
(TOP VIEW)

TRUTH TABLE

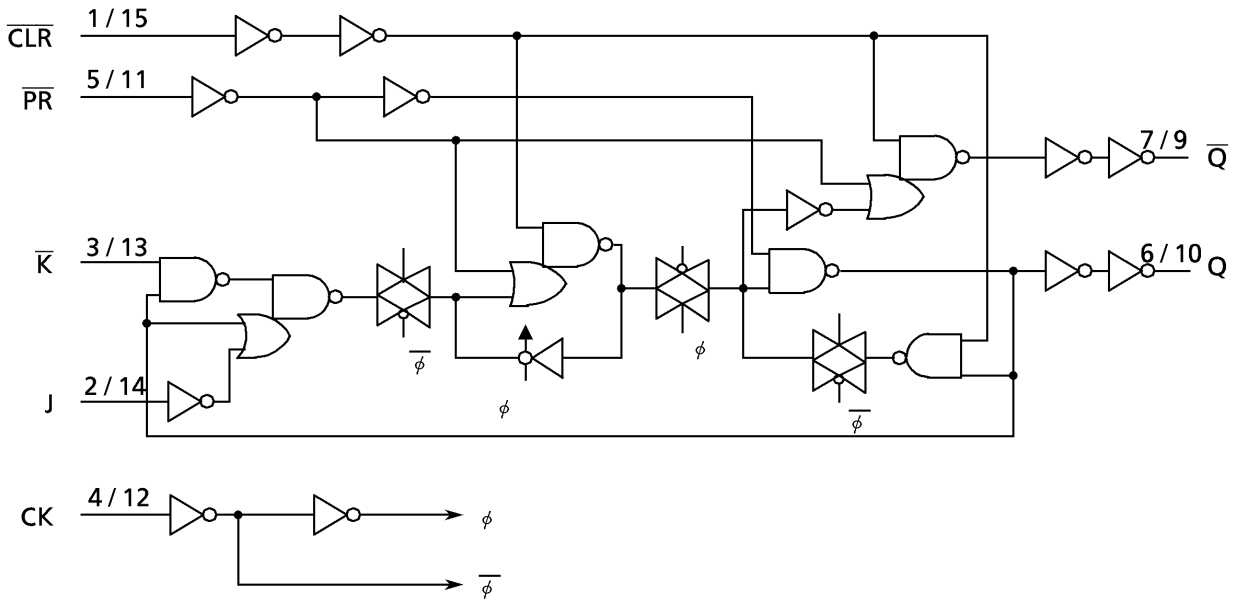
INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↑	Q_n	$\overline{Q}_n$	NO CHANGE
H	H	L	L	↑	L	H	
H	H	H	H	↑	H	L	
H	H	H	L	↑	$\overline{Q}_n$	Q_n	TOGGLE
H	H	X	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~ 100 (Vcc = 3.3 ± 0.3V) 0~ 20 (Vcc = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I_{OH} = −4mA I_{OH} = −24mA I_{OH} = −75mA*	3.0 4.5 5.5	2.58 3.94 —	— — —	— — —	2.48 3.80 3.85	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 12mA I_{OL} = 24mA I_{OL} = 75mA*	3.0 4.5 5.5	— — —	— — —	0.36 0.36 —	— — —	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	Ta = −40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		3.3 ± 0.3 5.0 ± 0.5	8.0 5.0	8.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	
Minimum Set - up Time	t_s		3.3 ± 0.3 5.0 ± 0.5	9.0 5.0	9.0 5.0	
Minimum Hold Time	t_h		3.3 ± 0.3 5.0 ± 0.5	0.0 0.0	0.0 0.0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		3.3 ± 0.3 5.0 ± 0.5	3.0 2.0	3.0 2.0	

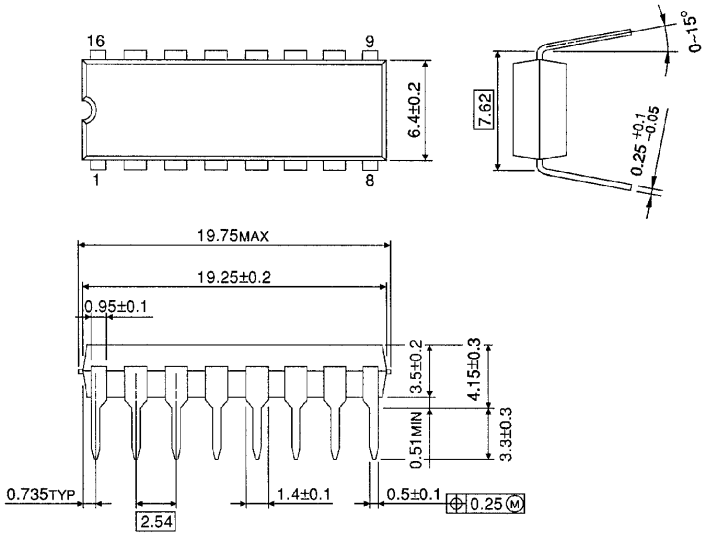
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF , R_L = 500 Ω , Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = −40~85°C		UNIT
		V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q , $\overline{Q}$)	t_{pLH} t_{pHL}	3.3 ± 0.3 5.0 ± 0.5	− −	8.2 6.1	13.9 8.7	1.0 1.0	16.0 10.0	ns
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q , $\overline{Q}$)	t_{pLH} t_{pHL}	3.3 ± 0.3 5.0 ± 0.5	− −	8.5 6.4	14.4 9.1	1.0 1.0	16.6 10.5	
Maximum Clock Frequency	f_{MAX}	3.3 ± 0.3 5.0 ± 0.5	55 100	120 160	− −	55 100	− −	MHz
Input Capacitance	C_{IN}		−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)		−	82	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

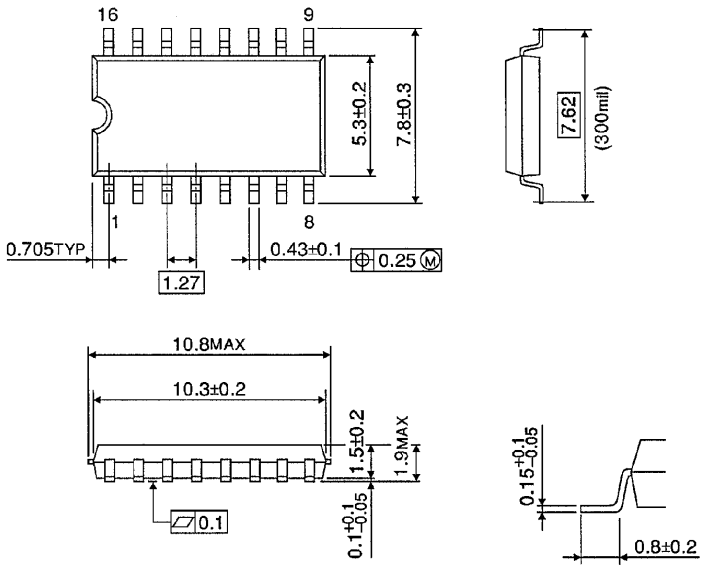
$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per F / F)}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

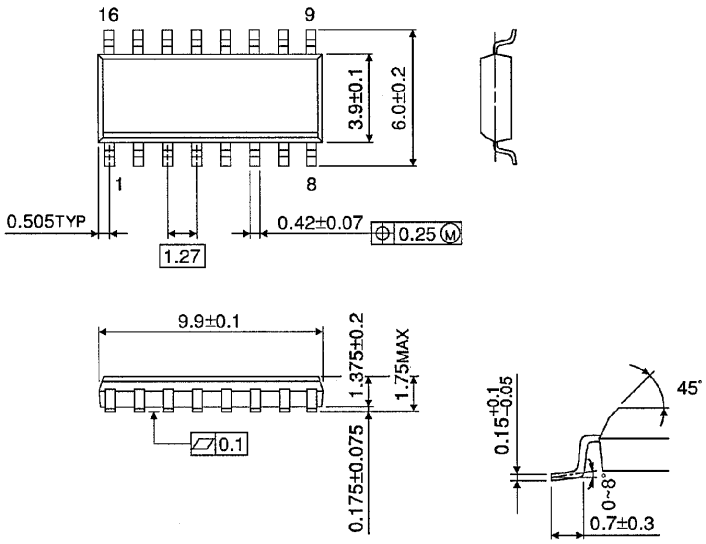
SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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