TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

2,097,152-WORD BY 16-BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC51WKM516AXBN is a 33,554,432-bit pseudo static random access memory(PSRAM) organized as 2,097,152 words by 16 bits. Using Toshiba's CMOS technology and advanced circuit techniques, it provides high density, high speed and low power. The device uses dual power supplies(2.6 to 3.3 V for core and 1.7 to 2.2 V for output buffer). The device also features SRAM-like W/R timing whereby the device is controlled by $\overline{CE1}$, $\overline{OE}$, and $\overline{WE}$ on asynchronous. The device has the page access operation. Page size is 8 words. The device also supports deep power-down mode, realizing low-power standby.

FEATURES

- Organized as 2,097,152 words by 16 bits
- Dual power supplies(2.6 to 3.3 V for core and 1.7 to 2.2 V for output buffer)
- Direct TTL compatibility for all inputs and outputs
- Deep power-down mode: Memory cell data invalid
- Page operation mode:
  Page read operation by 8 words
- Logic compatible with SRAM R/W ($\overline{WE}$) pin
- Standby current
  Standby 70 µA
  Deep power-down standby 5 µA
- Access Times:

Access Time	75 ns
$\overline{CE1}$ Access Time	75 ns
$\overline{OE}$ Access Time	25 ns
Page Access Time	30 ns

- Package:
  P-TFBGA48-0607-0.75AZ (Weight: g typ.)

PIN ASSIGNMENT (TOP VIEW)

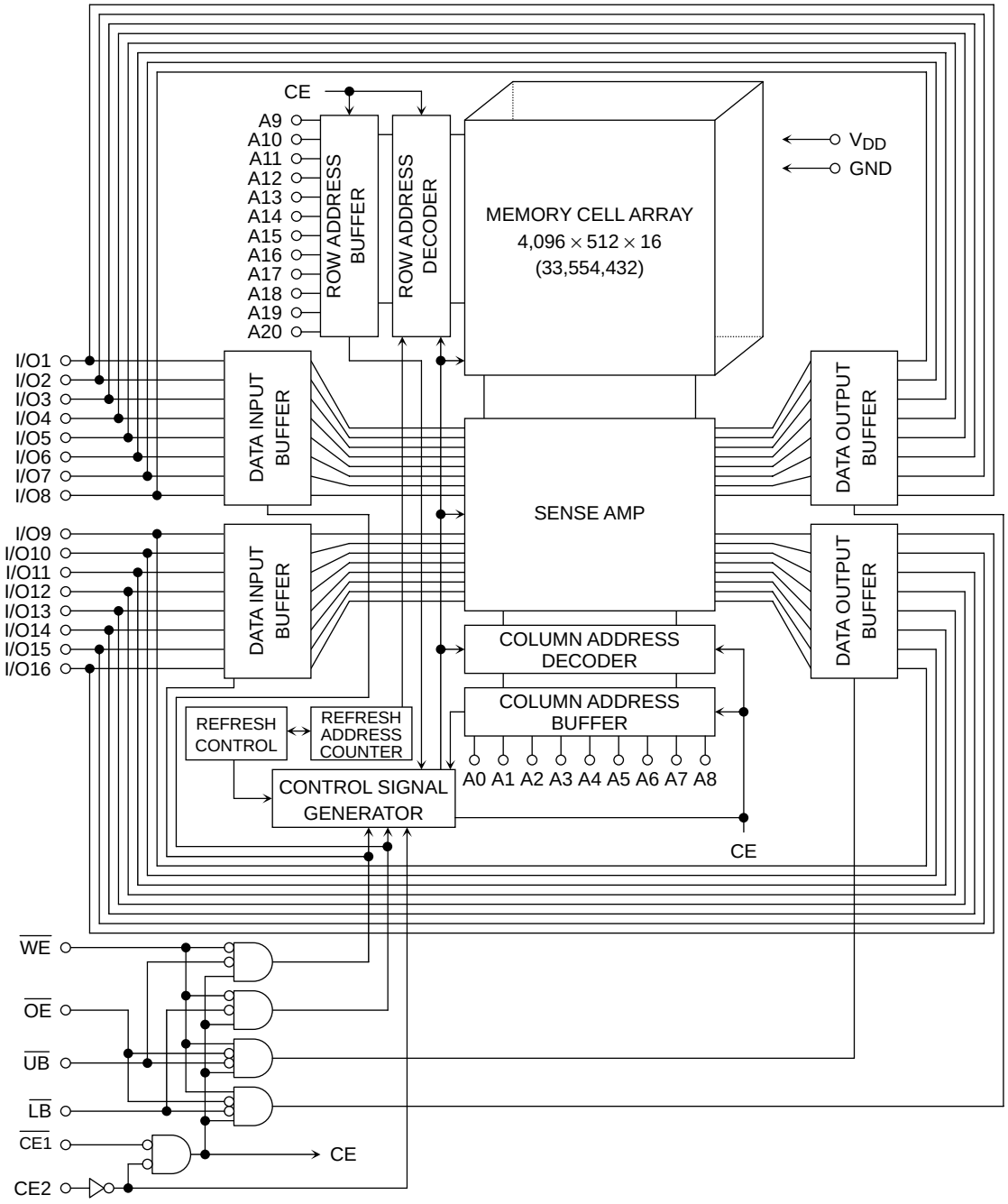
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	GND	I/O12	A17	A7	I/O4	V_{DD}
E	V_{DDQ}	I/O13	NC	A16	I/O5	GND
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	A19	A12	A13	$\overline{WE}$	I/O8
H	A18	A8	A9	A10	A11	A20

(FBGA48)

PIN NAMES

A0 to A20	Address Inputs
A0 to A2	Page Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE1}$	Chip Enable Input
CE2	Chip select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power Supply for Core
V_{DDQ}	Power Supply for Output Buffer
GND	Ground
NC	No Connection

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Add	I/O1 to I/O8	I/O9 to I/O16	POWER
Read(Word)	L	H	L	H	L	L	X	D_{OUT}	D_{OUT}	I_{DDO}
Read(Lower Byte)	L	H	L	H	L	H	X	D_{OUT}	High-Z	I_{DDO}
Read(Upper Byte)	L	H	L	H	H	L	X	High-Z	D_{OUT}	I_{DDO}
Write(Word)	L	H	X	L	L	L	X	D_{IN}	D_{IN}	I_{DDO}
Write(Lower Byte)	L	H	X	L	L	H	X	D_{IN}	Invalid	I_{DDO}
Write(Upper Byte)	L	H	X	L	H	L	X	Invalid	D_{IN}	I_{DDO}
Outputs Disabled	L	H	H	H	X	X	X	High-Z	High-Z	I_{DDO}
Standby	H	H	X	X	X	X	X	High-Z	High-Z	I_{DDS}
Deep Power-down Standby	H	L	X	X	X	X	X	High-Z	High-Z	I_{DDSD}

Notes: L = Low-level Input(V_{IL}), H = High-level Input(V_{IH}), X = V_{IH} or V_{IL}, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS (See Note 1)

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	–1.0 to 3.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	–1.0 to V_{DD} + 0.5 (3.6 V Max)	V
V_{IN}	Input Voltage for Address and Control Pins	–1.0 to 3.6	V
$V_{I/O}$	Input/Output Voltage for I/O Pins	–1.0 to V_{DDQ} + 0.5	V
$T_{opr.}$	Operating Temperature	–25 to 85	°C
$T_{strg.}$	Storage Temperature	–55 to 150	°C
T_{solder}	Soldering Temperature (10 s)	260	°C
P_D	Power Dissipation	0.6	W
I_{OUT}	Short Circuit Output Current	50	mA

DC RECOMMENDED OPERATING CONDITIONS (Ta = –25°C to 85°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{DD}	Power Supply Voltage	2.6	2.75	3.3	V
V_{DDQ}	Output Buffer Power Supply Voltage	1.7	1.8	2.2	
V_{IH}	Input High Voltage for Address and Control Pins	1.6	—	V_{DD} + 0.3*	
	Input High Voltage for I/O Pins	1.6	—	V_{DDQ} + 0.3*	
V_{IL}	Input Low Voltage	–0.3*	—	0.4	

* : V_{IH}(Max) V_{DD}+1.0 V/ V_{DDQ}+1.0 V with 10 ns pulse width
V_{IL}(Min) -1.0 V with 10 ns pulse width

DC CHARACTERISTICS (Ta = –25°C to 85°C, V_{DD} = 2.6 to 3.3 V, V_{DDQ} = 1.7 to 2.2 V) (See Note 3 to 4)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DDQ}		–1.0	—	+1.0	μA
I_{LO}	Output Leakage Current	Output disable, V_{OUT} = 0 V to V_{DD}		–1.0	—	+1.0	μA
V_{OH}	Output High Voltage	I_{OH} = – 100 μA		V_{DDQ} – 0.2	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 100 μA		—	—	0.2	V
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, I_{OUT} = 0 mA	t_{RC} = min	—	—	40	mA
I_{DDO2}	Page Access Operating Current	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, Page add. cycling, I_{OUT} = 0 mA	t_{PC} = min	—	—	25	mA
I_{DDS}	Standby Current(MOS)	$\overline{CE1}$ = V_{DD} – 0.2 V, CE2 = V_{DD} – 0.2 V		—	—	70	μA
I_{DDSD}	Deep Power-down Standby Current	CE2 = 0.2 V		—	—	5	μA

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is sampled periodically and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –25°C to 85°C, V_{DD} = 2.6 to 3.3 V, V_{DDQ} = 1.7 to 2.2 V) (See Note 5 to 11)

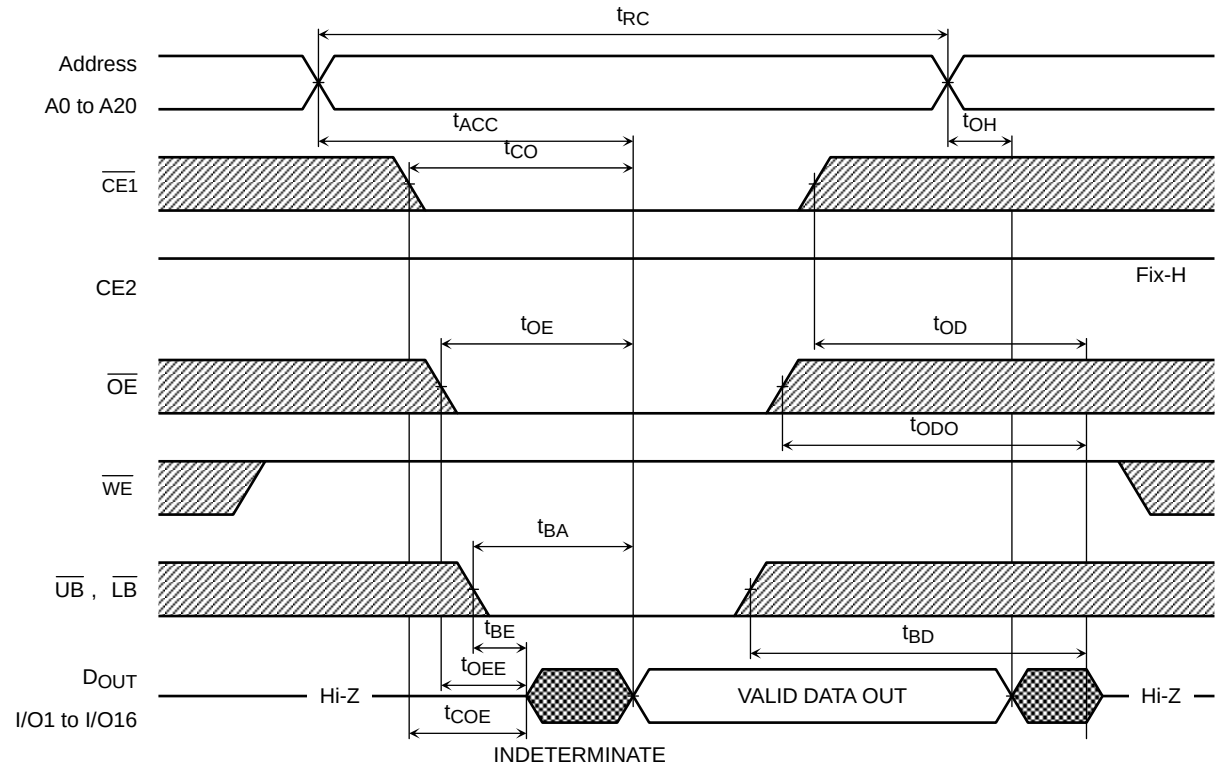
SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RC}	Read Cycle Time	75	10000	ns
t_{ACC}	Address Access Time	—	75	ns
t_{CO}	Chip Enable ($\overline{CE1}$) Access Time	—	75	ns
t_{OE}	Output Enable Access Time	—	25	ns
t_{BA}	Data Byte Control Access Time	—	25	ns
t_{COE}	Chip Enable Low to Output Active	10	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{BE}	Data Byte Control Low to Output Active	0	—	ns
t_{OD}	Chip Enable High to Output High-Z	—	20	ns
t_{ODO}	Output Enable High to Output High-Z	—	20	ns
t_{BD}	Data Byte Control High to Output High-Z	—	20	ns
t_{OH}	Output Data Hold Time	10	—	ns
t_{PM}	Page Mode Time	75	10000	ns
t_{PC}	Page Mode Cycle Time	30	—	ns
t_{AA}	Page Mode Address Access Time	—	30	ns
t_{AOH}	Page Mode Output Data Hold Time	10	—	ns
t_{WC}	Write Cycle Time	75	10000	ns
t_{WP}	Write Pulse Width	50	—	ns
t_{CW}	Chip Enable to End of Write	75	—	ns
t_{BW}	Data Byte Control to End of Write	60	—	ns
t_{AW}	Address Valid to End of Write	60	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{CEH}	Chip Enable High Pulse Width	10	—	ns
t_{WEH}	Write Enable High Pulse Width	15	—	ns
t_{ODW}	$\overline{WE}$ Low to Output High-Z	—	20	ns
t_{OEW}	$\overline{WE}$ High to Output Active	0	—	ns
t_{DS}	Data Set-up Time	30	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{CS}	CE2 Set-up Time	0	—	ns
t_{CH}	CE2 Hold Time	300	—	µs
t_{DPD}	CE2 Pulse Width	10	—	ms
t_{CHC}	CE2 Hold from $\overline{CE1}$	0	—	ns
t_{CHP}	CE2 Hold from Power On	30	—	µs

AC TEST CONDITIONS

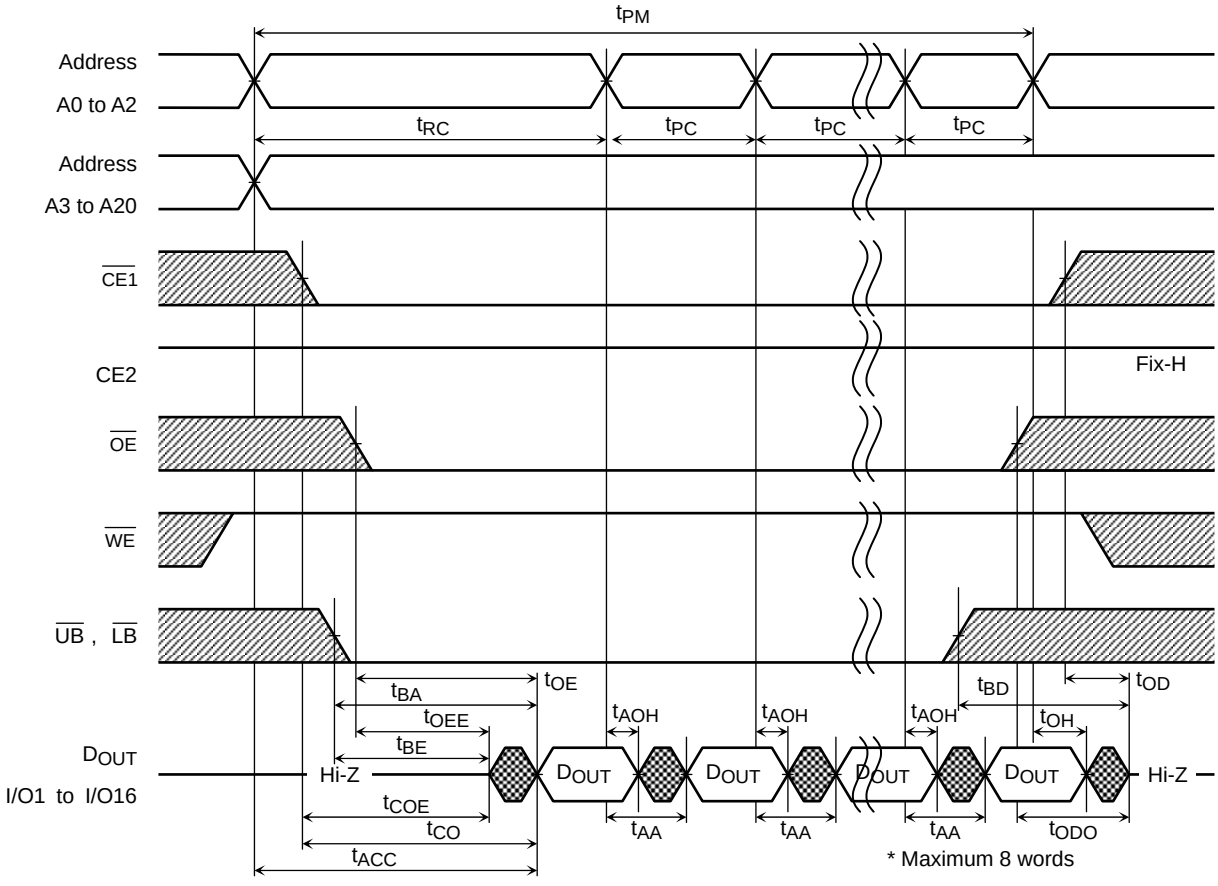
PARAMETER	CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	1.6 V, 0.2 V
Timing measurements	$V_{DDQ} \times 0.5$
Reference level	$V_{DDQ} \times 0.5$
t_R, t_F	5 ns

TIMING DIAGRAMS

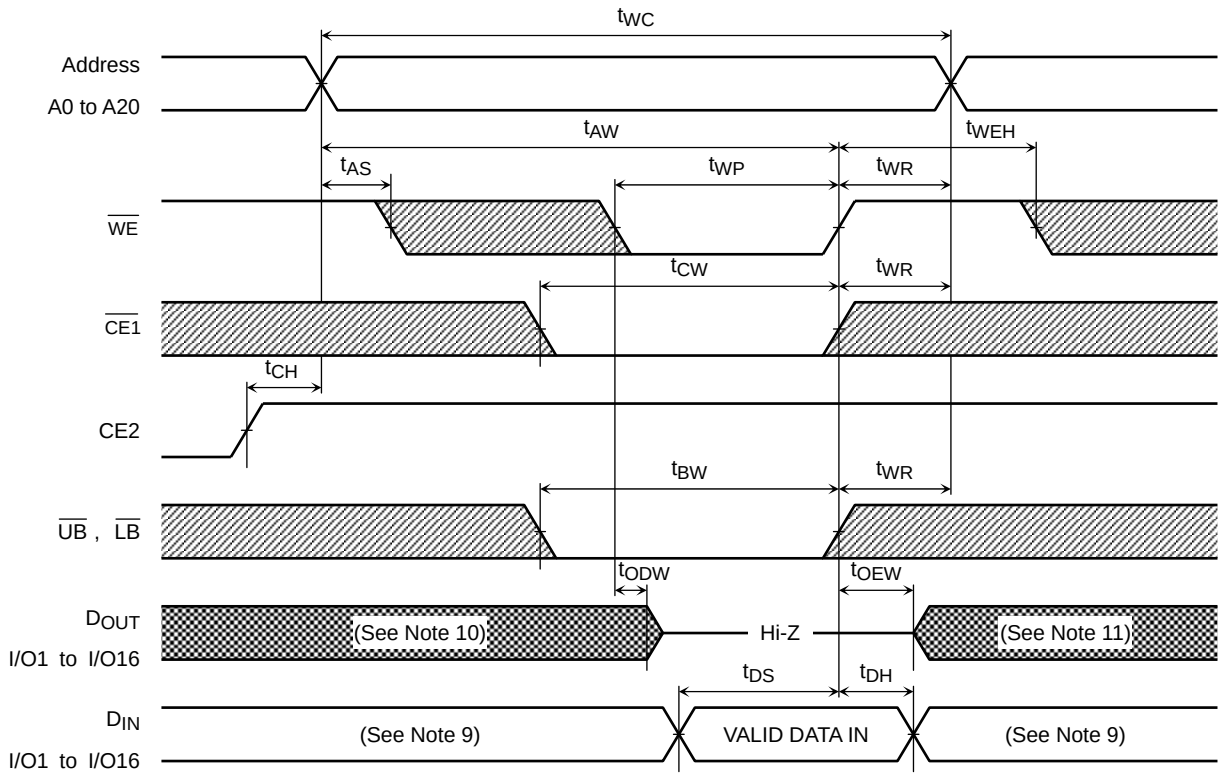
READ CYCLE



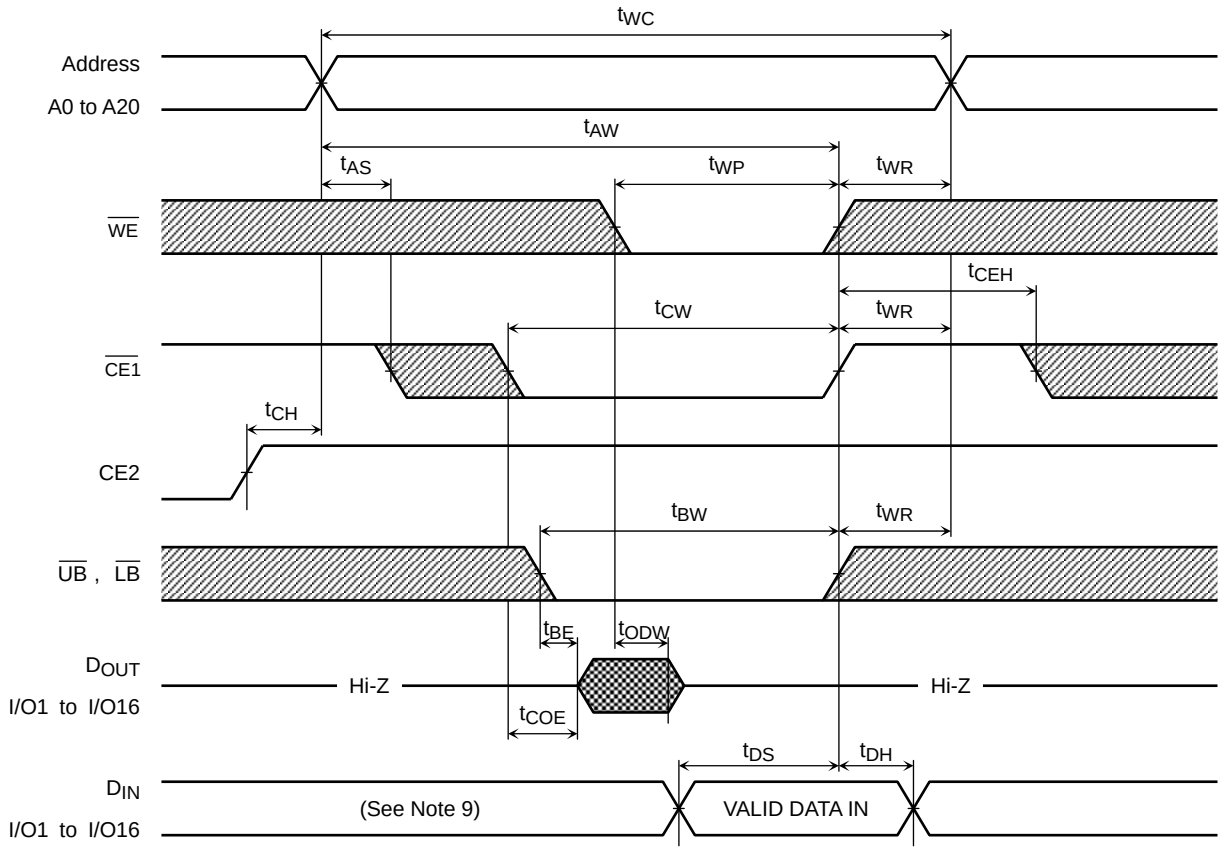
PAGE READ CYCLE (8 words access)



WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (See Note 8)

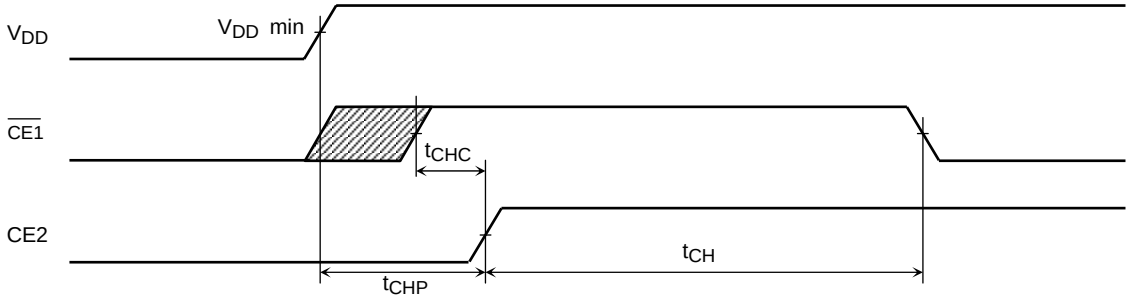


WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 8)



Deep Power-down Timing

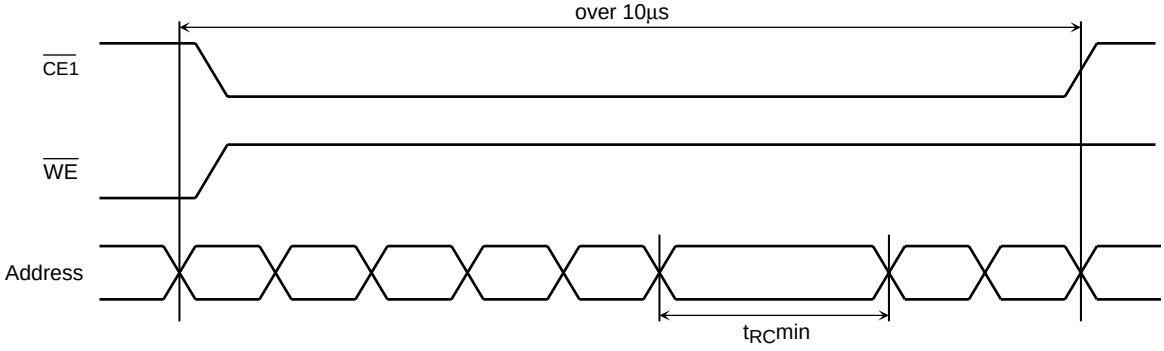
Power-on Timing



Provisions of Address Skew

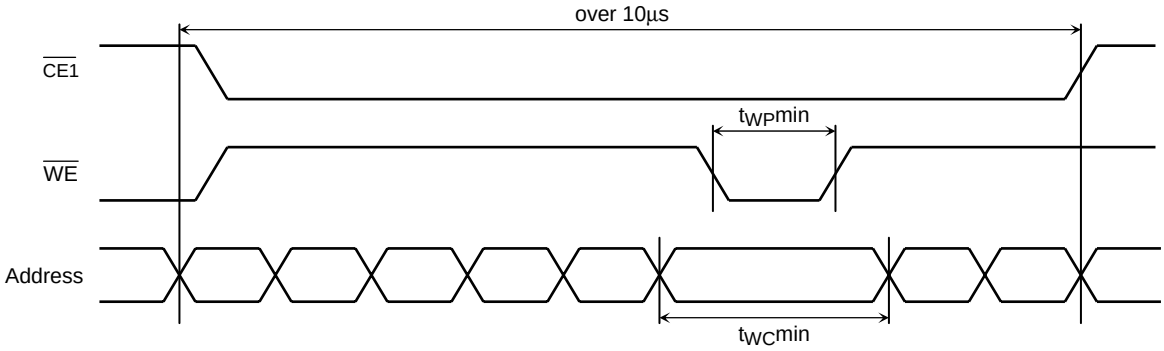
Read

In case, multiple invalid address cycles shorter than t_{RC}min sustain over 10µs in a active status, as least one valid address cycle over t_{RC}min must be needed during 10µs.



Write

In case, multiple invalid address cycles shorter than t_{WC}min sustain over 10µs in a active status, as least one valid address cycle over t_{WC}min with t_{WP}min must be needed during 10µs.



Notes:

(1) Stresses greater than listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

(2) All voltages are reference to GND.

(3) I_{DDO} depends on the cycle time.

(4) I_{DDO} depends on output loading. Specified values are defined with the output open condition.

(5) AC measurements are assumed t_R, t_F = 5 ns.

(6) Parameters t_{OD}, t_{ODO}, t_{BD} and t_{ODW} define the time at which the output goes the open condition and are not output voltage reference levels.

(7) Data cannot be retained at deep power-down stand-by mode.

(8) If $\overline{OE}$ is high during the write cycle, the outputs will remain at high impedance.

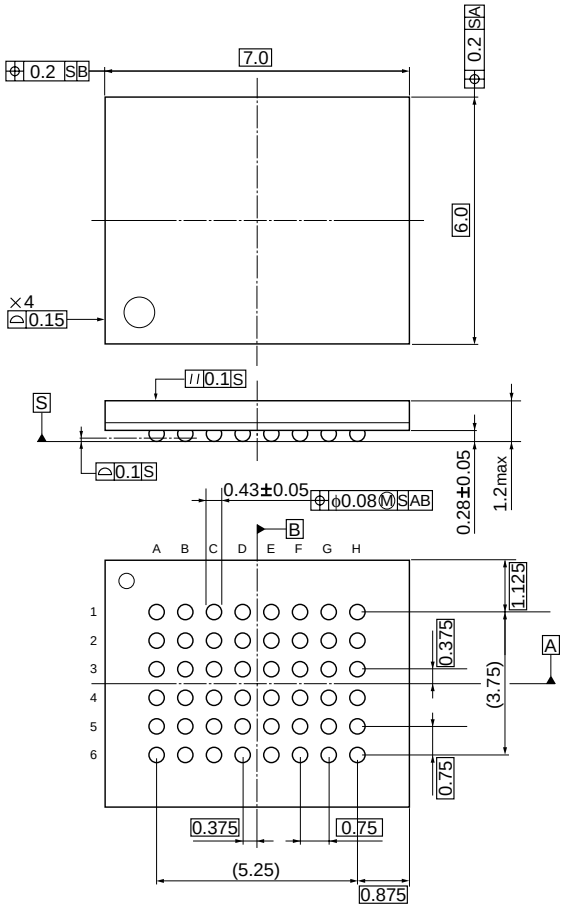
(9) During the output state of I/O signals, input signals of reverse polarity must not be applied.

(10) If $\overline{CE1}$ or $\overline{LB}$ / $\overline{UB}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

(11) If $\overline{CE1}$ or $\overline{LB}$ / $\overline{UB}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

PACKAGE DIMENSIONS

P-TFBGA48-0607-0.75AZ Unit:mm



Weight: g (typ)

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000707EBA

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