# **TBA510** CHROMA PROCESSING CIRCUIT

**GENERAL DESCRIPTION** – The TBA510 is a monolithic integrated circuit designed to perform the chrominance amplifier function for television receivers. It is constructed on a single silicon chip using the Fairchild Planar\* epitaxial process. A dc chroma gain control, which can be ganged to the receiver contrast control, is provided. Also incorporated is a variable gain automatic color control (ACC) stage, chroma blanking, burst gating, burst output stage. Two single output transistors provide burst and chroma output.





\*Planar is a patented Fairchild process.

CONNECTION DIAGRAM

16-PIN DIP (TOP VIEW)

PACKAGE OUTLINE 98





CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Input (pin 4)					
Peak-to-Peak Signal at Chroma Input (V <sub>4p-p</sub> )		15	150	300	mV <sub>p-p</sub>
Input Impedance of Chroma Signal (Z <sub>4</sub> )			3.0		kΩ
Burst Output (pin 11 and 12)					
DC Voltage at Color Burst Output (V12)			8.0		v
Peak-to-Peak Signal at Color Burst Output (V <sub>12p-p</sub> )	(Note 2)		1.0		V <sub>p-p</sub>
Collector Current of Color Burst Output (I11)			4.0		mA
Chroma Output (pin 8 and 9)		•			
DC Voltage at Chroma Output (Vg)			7.0		v
Peak-to-Peak Signal at Chroma Output (V <sub>9p-p</sub> )	(Note 3)		1.0		V <sub>n-n</sub>
Range of Contrast and Saturation Control		-30		+6.0	dB
Collector Current at Chroma Output (18)			5.0		mA
ACC Input (pin 2)					1
ACC Input Voltage (V <sub>2</sub> ) for Maximum Gain (Note 4)			2.5		v v
Input Impedance of ACC Control (Z <sub>2</sub> )		50			kΩ
Chroma Saturation Control Input (pin 15)					
Control Voltage Range (V15) (Note 4)		1.5		4.5	v
Input Impedance (Z <sub>15</sub> )		50			kΩ
Chroma Blanking Input (pin 14)	· · · · ·				
Switching Level Range (V14)		-5.0		-1.0	v
Input Impedance (Z <sub>14</sub> )			2.0		kΩ
Burst Gate Input (pin 13)					
Switching Level Range (V <sub>13</sub> )		-5.0		-2.2	v
Input Impedance (Z <sub>13</sub> )			4.0		kΩ
Color Killer Input (pin 5)					
Input Voltage (V5) for:					
Color on		2.5	1	4.0	v
Color off		0		1.8	l v
Signal Suppression at Color Off		50			dB
Input Impedance (Z <sub>5</sub> )		100			kΩ.

## FAIRCHILD • TBA510



#### NOTES:

NOTES:
NC - no connection (not to be used as a tie point).
Color burst output kept constant by ACC circuit.
Chroma output (emitter) at nominal saturation and maximum contrast.
Gain control characteristic positive.

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- Not to be used as a tie point. It is recommended that pins 7 and 10 be arounded.
- 8. Delay line driver (collector) Supplies the chroma signal drive to the delay line driver transformer, the "cold" end of which is connected to +12 V. The maximum permitted voltage excursion at this pin is 20 V peak. Maximum current, 12 mA peak.
- 9. Delay line driver (emitter)

Supplies the chroma to the network which provides the non-delayed signal to the delay line output transformer. The emitter is established internally at a potential of 6.8 ± 1.0 V and the external network, which must incorporate a resistive dc path to ground, must not demand more than 20 mA peak current.

- 10. No connection
- Not to be used as a tie point. (See pin 7.)
- 11. Color burst output (collector)

If a low impedance color burst is required (from the emitter of the color burst output, pin 12) pin 11 will be connected to the +12 V supply. The maximum voltage and current excursions permitted on pin 11 are 20 V peak and 20 mA peak.

### 12. Color burst output (emitter)

An external load resistor of 2.0 kΩ is required connected to ground and dc potential of 7.7 ± 1.0 V is established on pin 12 due to the internal circuitry. The burst output voltage is 1.0 V peak-to-peak.

13. Burst gate gating pulse

The horizontal flyback pulse can be used as a source of gating waveform. A negative going pulse of not greater than 5.0 V amplitude is necessary, the input impedance is 4.0 k $\Omega$  and the switching level is between -2.2 V and -5.0 V

14. Chroma blanking pulse input

A negative going horizontal flyback pulse can be used here. Its amplitude should not exceed -5.0 V. The input impedance at this pin is 2.0 k $\Omega$  and the switching level is about -1.0 V. During scan time, the dc voltage on this pin should not be negative.

#### 15. Chroma saturation control

The dc control voltage range required is from 1.5 to 4.5 V (highest gain at 4.5 V). The input impedance is > 50 k $\Omega$  and a control range from +6.0 to -30 dB is given.

16. Ground