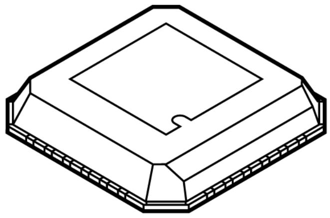
TOSHIBA Bipolar Linear IC Silicon Monolithic

TA2131FL

Low Current Consumption Headphone Amplifier for Portable MD Player (With Bass Boost Function)

The TA2131FL is a low current consumption headphone amplifier developed for portable digital audio. It is particularly well suited to portable MD players that are driven by a single dry cell. It also features a built-in bass boost function with AGC, and is capable of bass amplification of DAC output and analog signals such as tuner.
An ultra-compact QON package is utilized, enabling sets to be compacted.



QON24-P-0505-0.50

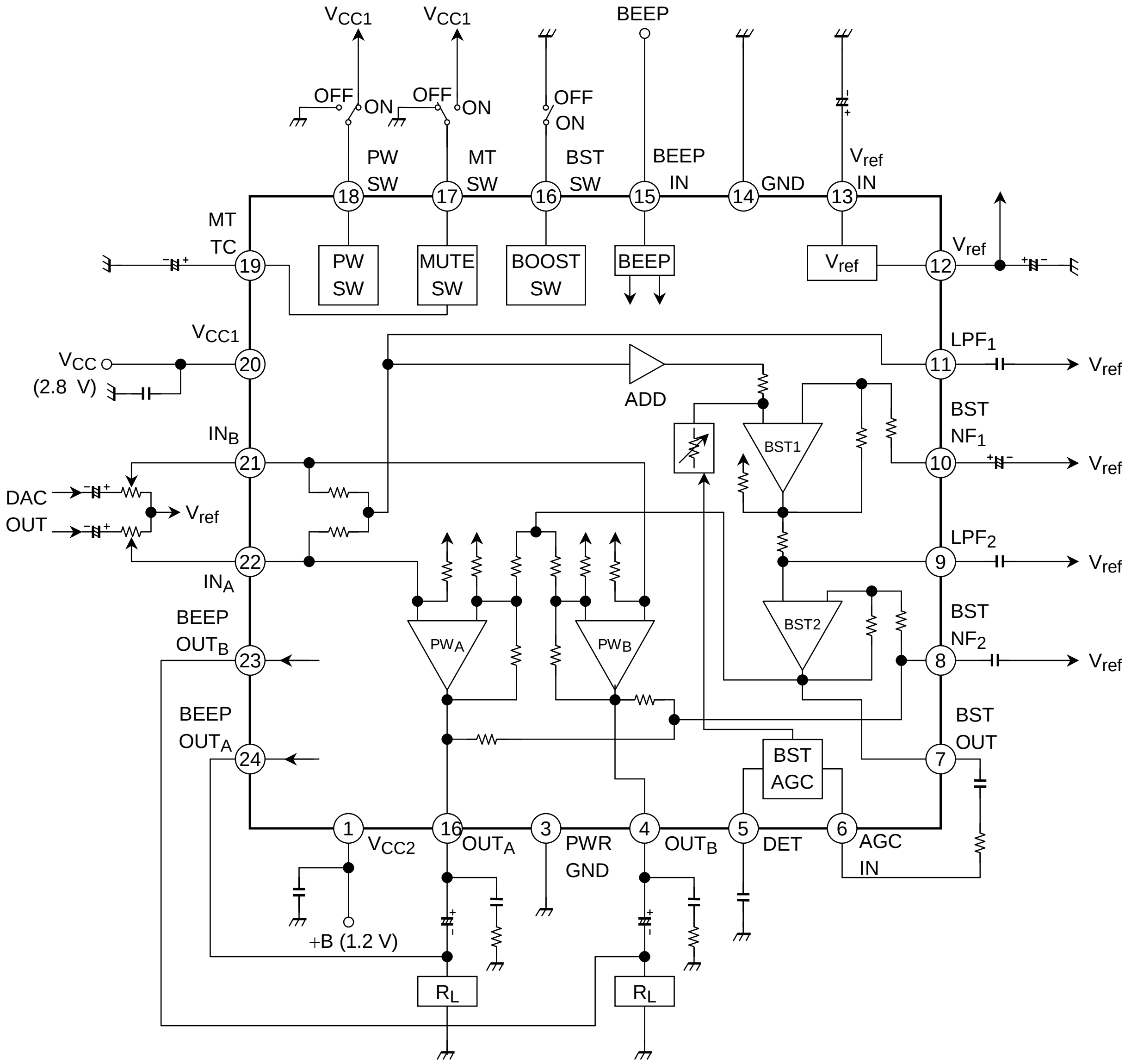
Weight: 0.05 g (typ.)

Actual product display name: 2131

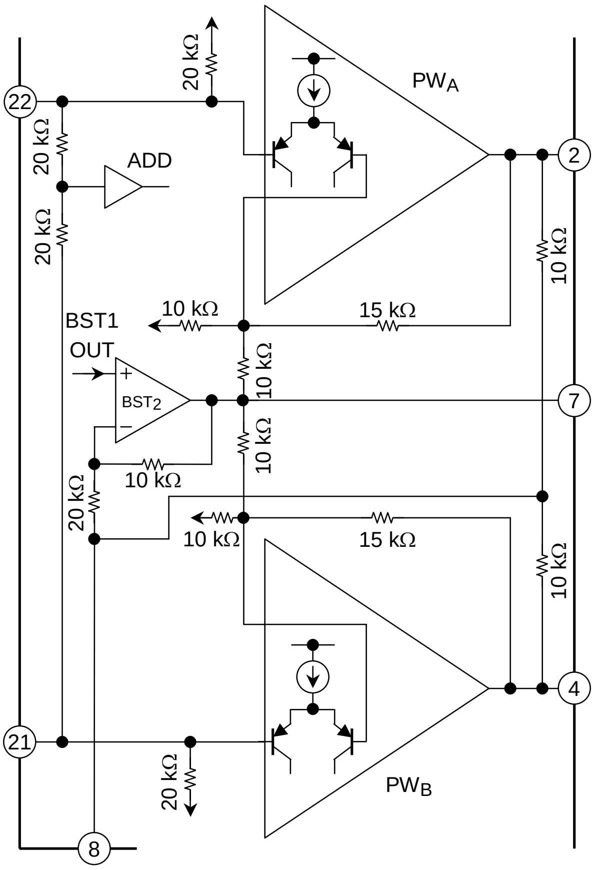
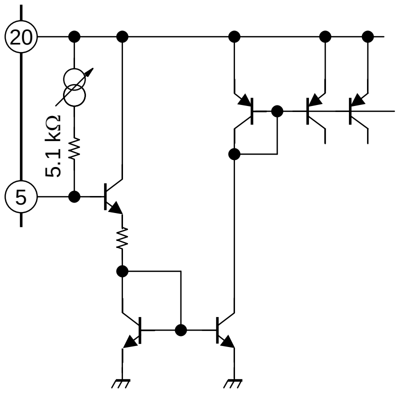
Features

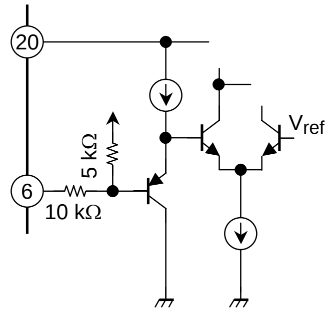
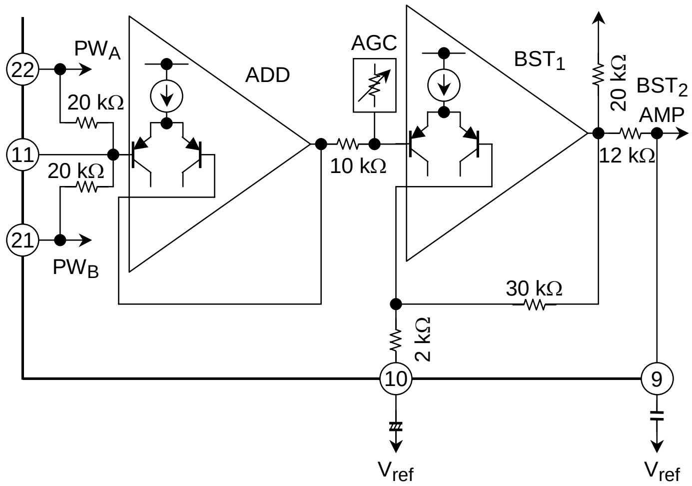
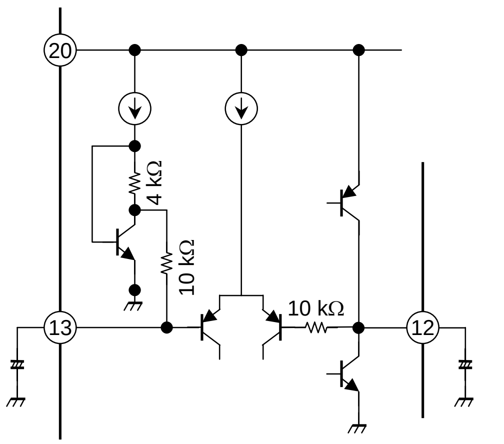
- Low current consumption: I_{CCQ} (V_{CC1}) = 0.55 mA (typ.)
  I_{CCQ} (V_{CC2}) = 0.20 mA (typ.)
- Output power: P_o = 8 mW (typ.)
  (V_{CC1} = 2.8 V, V_{CC2} = 1.2 V, f = 1 kHz, THD = 10%, R_L = 16 Ω)
- Low noise: V_{no} = −102dBV (typ.)
- Built-in low-pass boost (with AGC)
- I/O pin for beep sound
- Outstanding ripple rejection ratio
- Built-in power mute
- Built-in power ON/OFF switch
- Operating supply voltage range (Ta = 25°C): V_{CC1} = 1.8~4.5 V
  V_{CC2} = 0.9~4.5 V

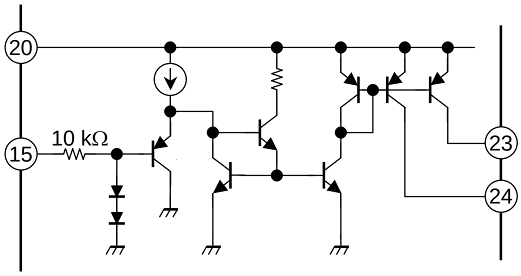
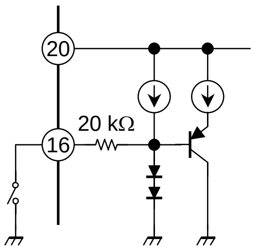
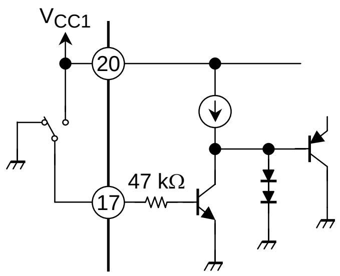
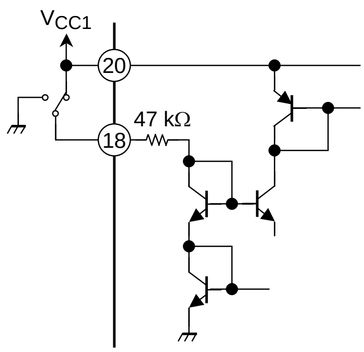
Block Diagram

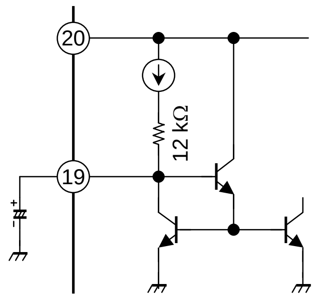


Terminal Explanation (Terminal voltage: Typical terminal voltage at no signal with test circuit, V_{CC1} = 2.8 V, V_{CC2} = 1.2 V, Ta = 25°C)

Terminal No.		Terminal Explanation	InternaL Circuit	Terminal Voltage (V)
1	V_{CC2}	V_{CC} (+B) at power amplifier output stage	—	1.2
2	OUT_A	Power amplifier output		0.61
4	OUT_B			
21	IN_B	Power amplifier input		0.61
22	IN_A			
7	BST OUT	BST amplifier 2 output terminal		0.61
8	BST NF_2	BST amplifier 2 NF terminal (low-pass compensation condenser connection terminal)		0.61
3	PWR GND	GND of power amplifier output stage	—	0
5	DET	Smoothing of boost AGC level detection		—

Terminal No.		Terminal Explanation	InternaL Circuit	Terminal Voltage (V)
6	AGC IN	Signal input level to BST amplifier is varied according to the input level to the boost AGC input terminal. Input impedance: 15 kΩ (typ.)		0.61
9	LPF_2	BST amplifier 1 output (filter terminal)		0.61
10	BST NF_1	BST amplifier 1 NF		0.61
11	LPF_1	ADD amplifier output (filter terminal)		0.61
12	V_{ref}	Reference voltage circuit		0.61
13	V_{ref} IN	Reference voltage circuit filter terminal		0.61
14	GND	GND of input stage in power amplifier	—	0

Terminal No.		Terminal Explanation	InternaL Circuit	Terminal Voltage (V)
15	BEEP IN	Beep sound input terminal Receives beep sound signals from microcomputer.		0
23	BEEP OUT_B	Beep sound output terminal		—
24	BEEP OUT_A			
16	BST SW	Bass boost ON/OFF switch “H” level/OPEN: BST ON “L” level: BST OFF Refer to function explanation 5		—
17	MT SW	Mute switch “L” level: Mute reset “H” level: Mute ON Refer to function explanation 5		—
18	PW SW	Power ON/OFF switch “H” level: IC operation “L” level: IC OFF Refer to function explanation 5		—

Terminal No.		Terminal Explanation	InternaL Circuit	Terminal Voltage (V)
19	MT TC	Mute smoothing Power mute switch Reduces the shock noise during switching		1.2
20	V_{CC1}	Main V_{CC}	—	2.8

Function Explanation

1. Bass Boost Function

1-1 Description of Operation

TA2131FL has a bass boost function for bass sound reproduction built-in to the power amplifier. With the bass boost function, at medium levels and lower, channel A and channel B are added for the low frequency component, and output to BST amplifier 2 (BST_2) in negative phase. That signal is inverted and added before being subjected to bass boost. If the signal of the low-frequency component reaches a high level, the boost gain is controlled to main a low distortion (see Fig.1).

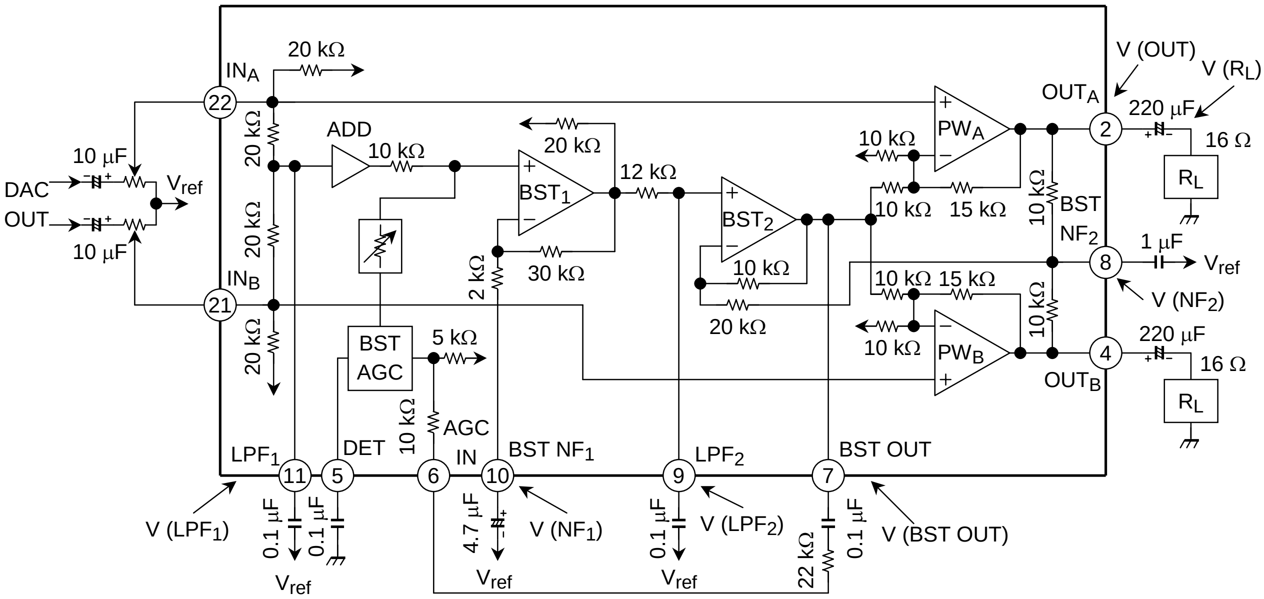


Figure 1 System Diagram of Bass Boost

1-2 AGC Circuit

The AGC circuit of the bass boost function detects with “AGC DET” the voltage component created by “BST_2,” and as the input level increases, the variable impedance circuit is changed, and the bass boost signal is controlled so that it is not assigned to BST amplifier 1. In this way, the bass signal to “BST_2” input is shut-off, and that boost gain is controlled.

1-3 Bass Boost System

As shown in Fig.1, the flow of the bass boost signal is that the signal received from power amplifier input goes through LPF_1, ADD amplifier, ATT (variable impedance circuit), BPF_1 (BST amplifier 1) and LPF_2, and the negative phase signal to the power amplifier input signal is output from BST amplifier 2. The reason why it becomes the negative phase of the BST amplifier 2 signal is that the phase is inverted by 180° in the audible bandwidth by the secondary characteristics of LPF_1 and LPF_2 in Fig.1.

Ultimately the main signal and the bass boost signal formed before BST_2 are added.

Fig.2 shows the frequency characteristics to each terminal.

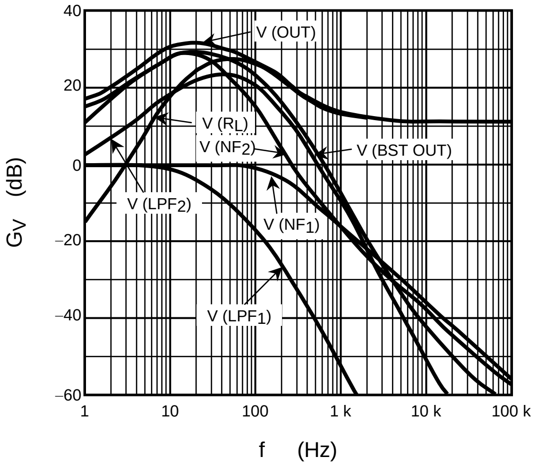


Figure 2 During Bass Boost (Frequency Characteristics to Each Terminal)

2. Low-Pass Compensation

2-1. Function

In C-couple type power amplifiers, it is necessary to give the output condenser C a large capacity to flatten out the frequency characteristics to the low frequency band (this is because the loss in the low frequency bandwidth becomes larger due to the effect of the high-pass filter comprising C and R_L).
Particularly when the headphone load is approximately 16 Ω and an attempt is being made to achieve frequency characteristics of ±3 dB at 20 Hz, a large capacity condenser of
C = 470 μF is required.
Bearing this situation in mind, a low-pass compensation function was built in to the TA2131FL, and while reducing the capacity of the output coupling condenser, almost flat (±3 dB) frequency characteristics in all audible bandwidths (20 Hz to 20 kHz) have been achieved.
Fig.3 shows the low-pass system diagram, and Fig.4 shows the frequency characteristics at each point.
In Fig.4, (a) represents the status lost by the low-pass as a result of the high-pass filter comprising the headphone load (R_L = 16 Ω) and the output coupling condenser (220 μF) in the C-coupling system.

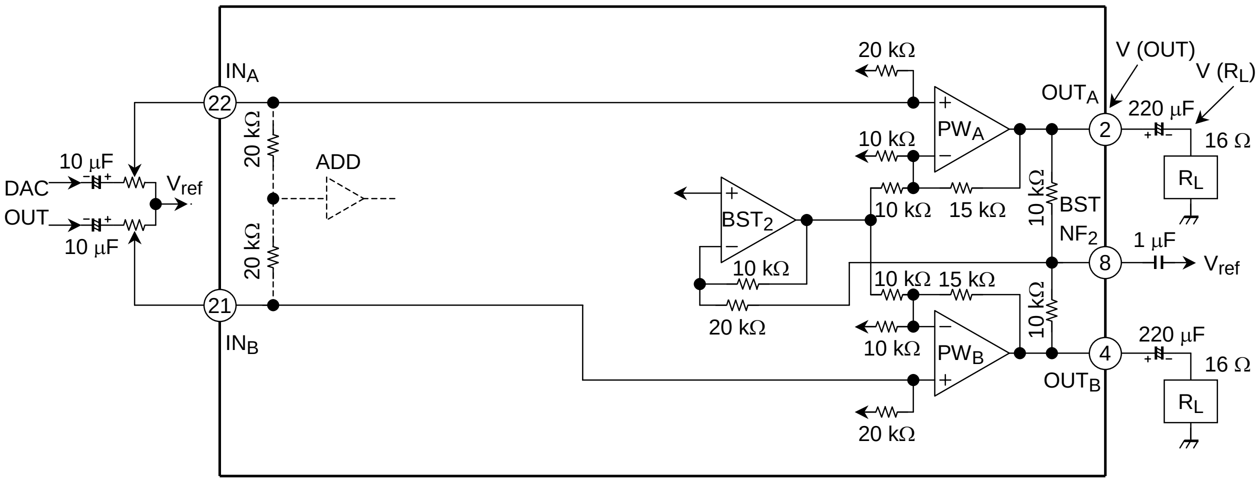


Figure 3 Low-Pass Compensation System Diagram

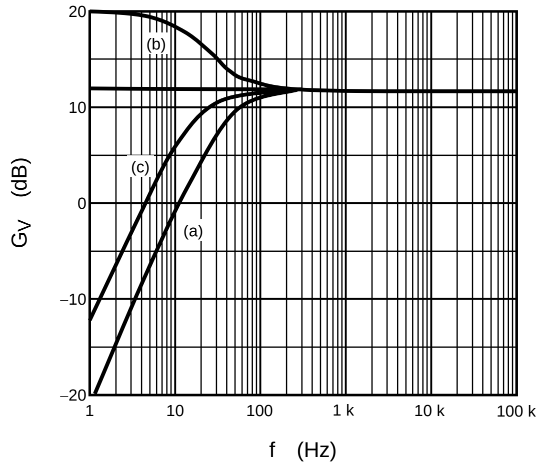


Figure 4 Power Amplifier Frequency Characteristics

<Principle of Low-Pass Compensation>

The low-pass component alone is extracted from the composite signal of PW_A/PW_B output, and that frequency signal is fed back to PW_A/PW_B once more via the inversion amplifier, thereby making it possible to increase the gain only of the low-pass component. The frequency characteristics of the power amplifier output V (OUT) in this state are shown in Fig.4 (b). In practice they are the frequency characteristics (c) viewed from load terminal V (R_L), and the low-pass is compensated relative to the state in (a).

2-2. Low-Pass Compensation Condenser and Crosstalk

In this low-pass compensation condenser circuit, processing is carried out using the composite signal of power amplifier output, so this affects crosstalk, according to the amount of compensation. f characteristics and crosstalk generated by the capacity of the condenser for compensation (8-pin) are shown below.

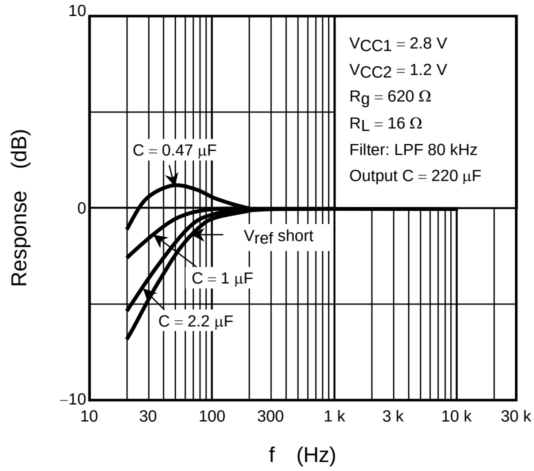


Figure 5 Condenser and f Characteristics for Low-Pass Compensation

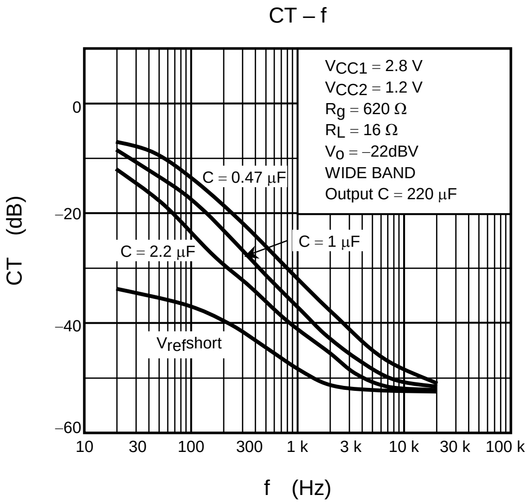
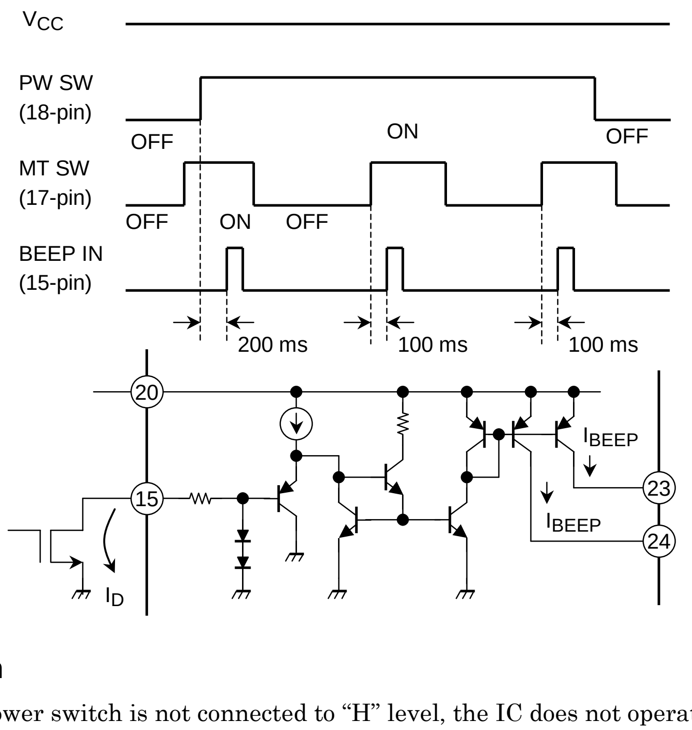


Figure 6 Low-Pass Compensation Condenser and Crosstalk

3. Beep

Beep sound signals from microcomputer can be received by the beep input terminal (15-pin).
The PW_A and PW_B of the power amplifier during power mute are turned OFF, and the beep signal input from BEEP-IN (15-pin) is output from the BEEP-OUT terminal (23/24-pin) as fixed current, after passing through the converter and current amplification stage. Connecting this terminal to the headphone load outputs the beep sound.
If the beep sound is not input, fix the BEEP-IN (15-pin) terminal to GND level.

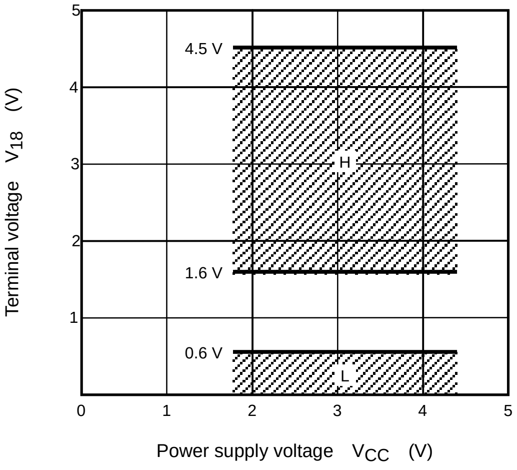


4. Power Switch

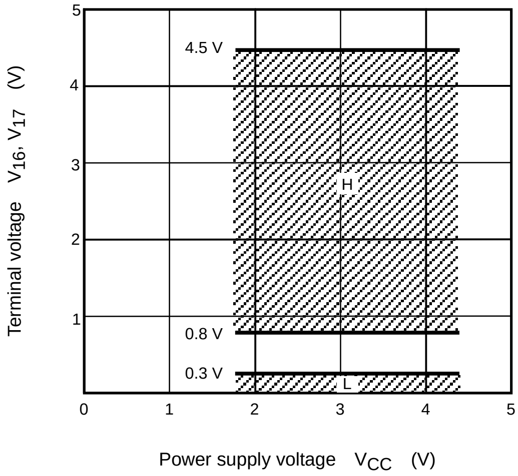
As long as the power switch is not connected to “H” level, the IC does not operate. If it malfunctions due to external noise, however, it is recommended to connect a pull-down resistor externally (the power switch is set to be highly sensitive).

5. Threshold Voltages of Switches

(1) PW SW



(2) MT SW, BST SW



	PW SW (V_{18})
"H" level	IC operation
"L" level	IC OFF

	MT SW (V_{17})
"H" level	Mute ON
"L" level	Mute reset

	BST SW (V_{16})
"H" level/OPEN	BST ON
"L" level	BST OFF

6. These capacitors which prevent oscillation of the power amplifier, and are between the V_{ref} and V_{CC}-GND must have a small temperature coefficient and outstanding frequency characteristics.

Maximum Ratings

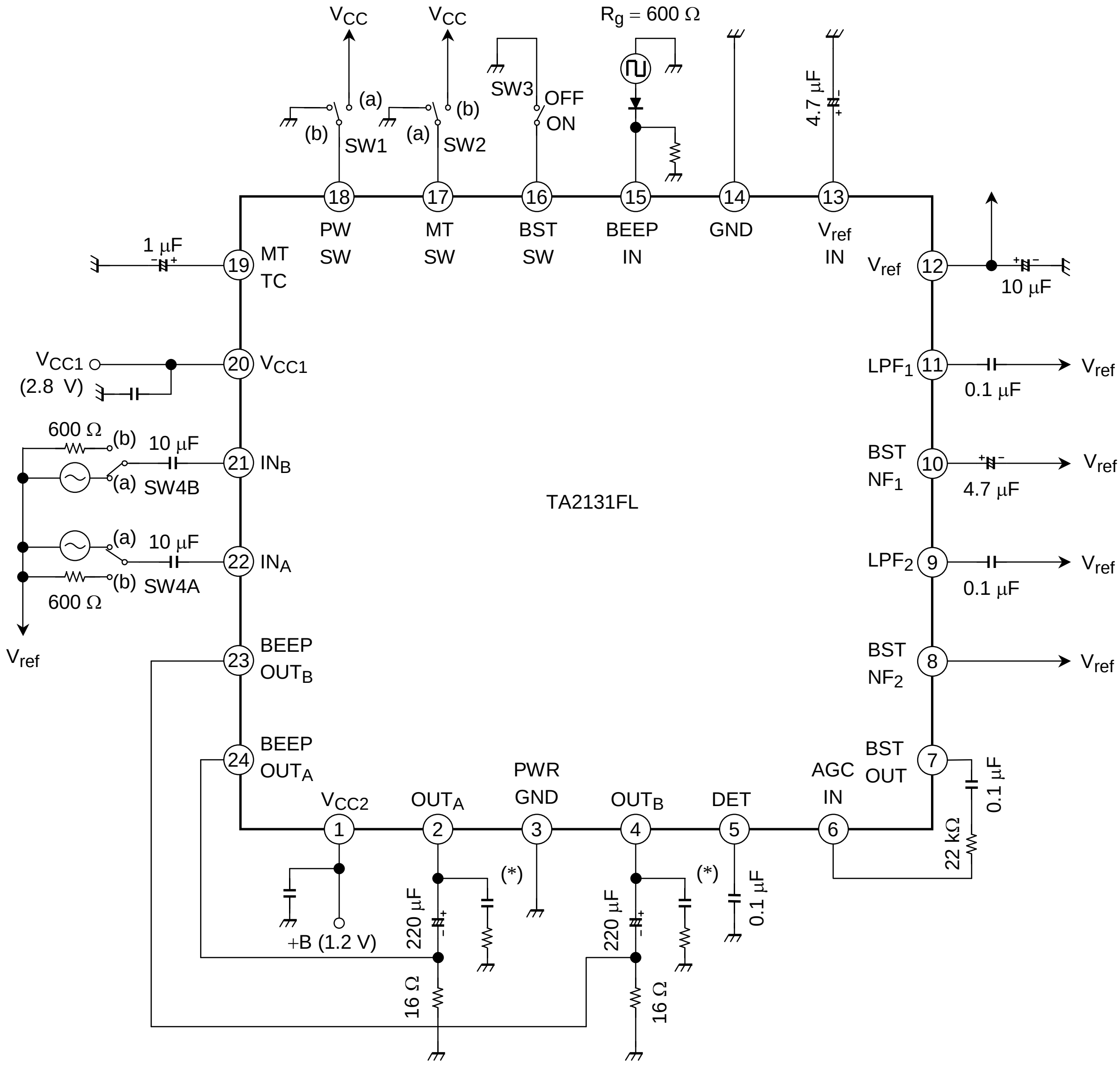
Characteristic	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5	V
Output current	$I_{o\ (peak)}$	100	mA
Power dissipation	P_D (Note)	350	mW
Operating temperature	T_{opr}	−25~75	°C
Storage temperature	T_{stg}	−55~150	°C

Note: Derated above Ta = 25°C in the proportion of 2.8 mW/°C.

Electrical Characteristics (Unless specified otherwise, V_{CC1} = 2.8 V, V_{CC2} = 1.2 V, R_g = 600 Ω, R_L = 16 Ω, f = 1 kHz, Ta = 25°C)

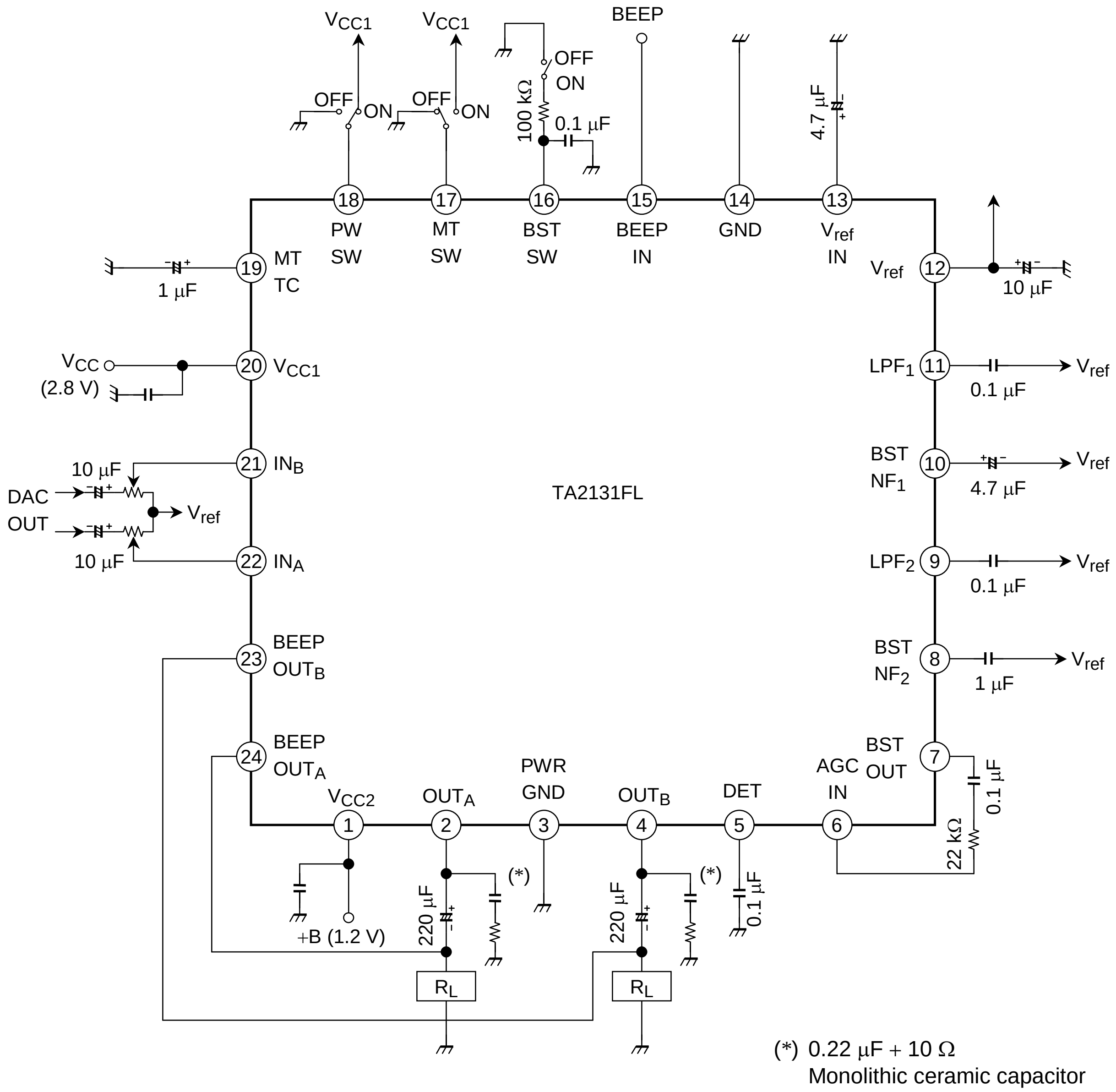
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Quiescent supply current		I_{CC1}	IC off (V_{CC1}), SW1: b, SW2: b	—	0.1	5	μA
		I_{CC2}	IC off (V_{CC2}), SW1: b, SW2: b	—	0.1	5	
		I_{CC3}	Mute on (V_{CC1}), SW1: a, SW2: b	—	0.35	0.50	mA
		I_{CC4}	Mute on (V_{CC2}), SW1: a, SW2: b	—	5	10	μA
		I_{CC5}	No signal (V_{CC1}), SW1: a, SW2: a	—	0.55	0.75	mA
		I_{CC6}	No signal (V_{CC2}), SW1: a, SW2: a	—	0.20	0.40	
Power supply current during drive		I_{CC7}	P_o = 0.5 mW + 0.5 mW output (V_{CC1})	—	0.6	—	
		I_{CC8}	P_o = 0.5 mW + 0.5 mW output (V_{CC2})	—	5.3	—	
Power Section	Gain	G_V	V_o = −22dBV	10	12	14	dB
	Channel balance	CB	V_o = −22dBV	−1.5	0	1.5	
	Output power	$P_{o\ max}$	THD = 10%	5	8	—	mW
	Total harmonic distortion	THD	P_o = 1 mW	—	0.1	0.3	%
	Output noise voltage	V_{no}	R_g = 600 Ω, Filter: IHF-A, SW4: b	—	−102	−96	dBV
	Crosstalk	CT	V_o = −22dBV	−42	−48	—	dB
	Ripple rejection ratio	RR1	f_r = 100 Hz, V_r = −20dBV inflow to V_{CC2}	−71	−77	—	
		RR2	f_r = 100 Hz, V_r = −20dBV inflow to V_{CC1}	−54	−64	—	
	Mute attenuation	ATT	V_o = −12dBV, SW2: a → b	−90	−100	—	
	Beep sound output voltage	VBEEP	V Beep IN = 2 $V_{p\text{-}o}$, SW2: b	−53	−48	−43	dBV
Boost gain		BST1	V_o = −20dBV, f = 100 Hz, SW3: ON → OPEN	1	4	7	dB
		BST2	V_o = −30dBV, f = 100 Hz, SW3: ON → OPEN	10	13	16	
		BST3	V_o = −50dBV, f = 100 Hz, SW3: ON → OPEN	13.5	16.5	19.5	

Test Circuit

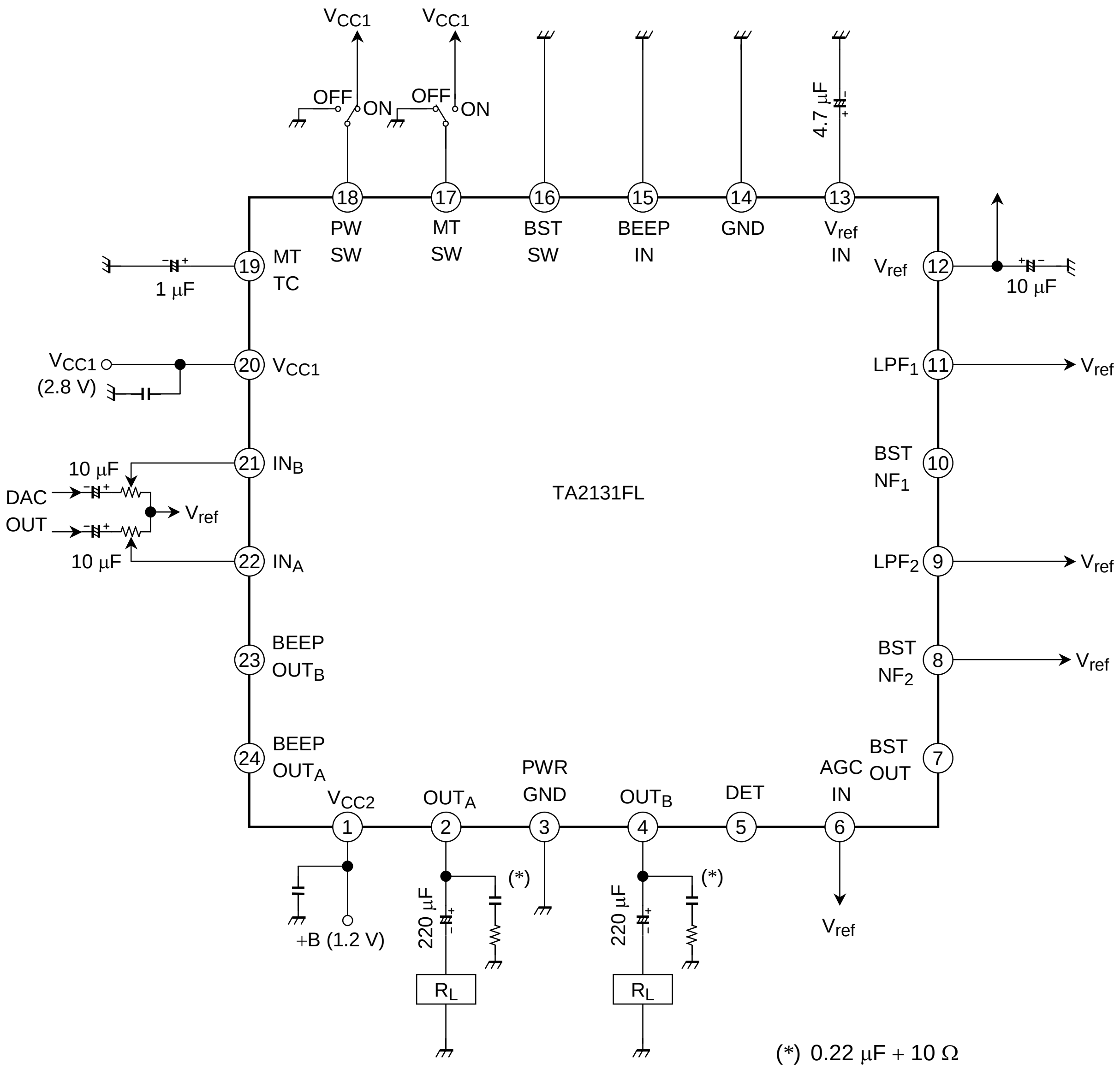


(*) 0.22 μF + 10 Ω
Monolithic ceramic capacitor

Application Circuit 1

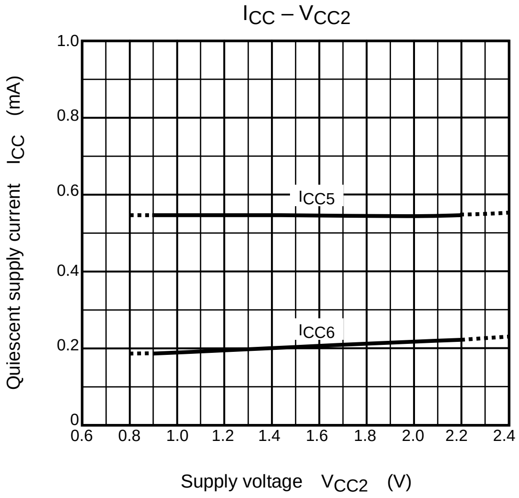


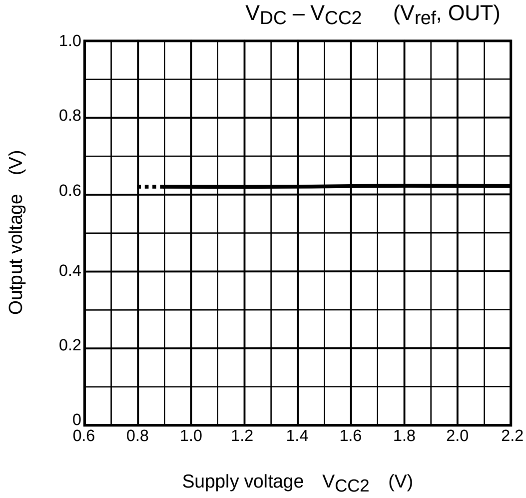
Application Circuit 2 (Low-Pass Compensation/Bass Boost Function/Beep Not Used)

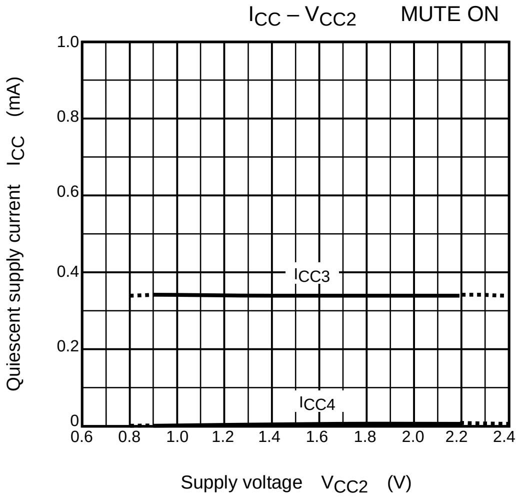


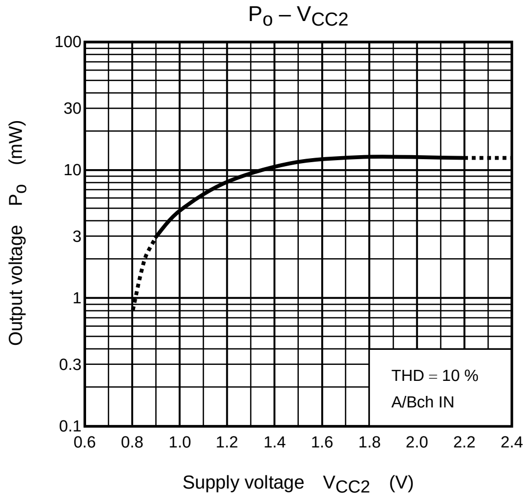
(*) 0.22 μF + 10 Ω
Monolithic ceramic capacitor

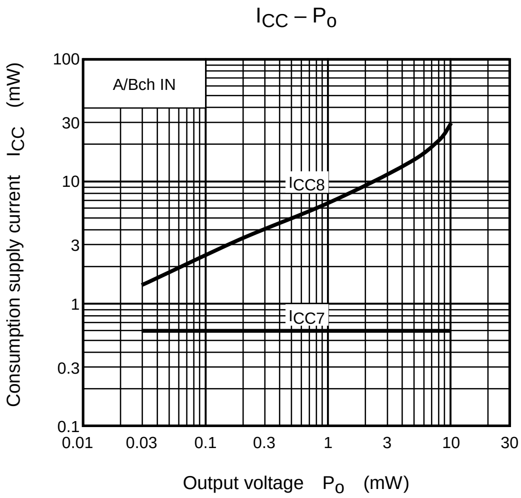
Characteristics (Unless otherwise specified $V_{CC1} = 2.8$ V, $V_{CC2} = 1.2$ V, $R_g = 600\ \Omega$, f = 1 kHz, Ta = 25°C)

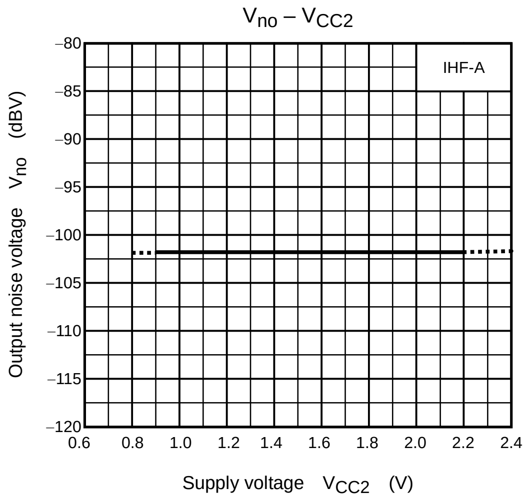


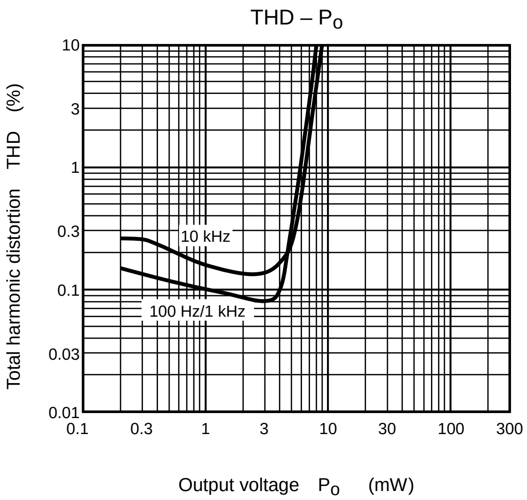


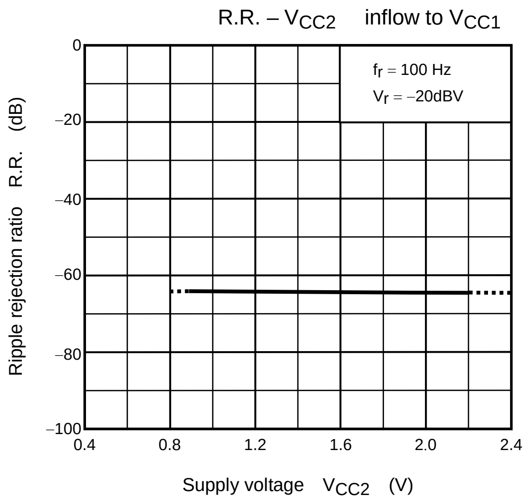


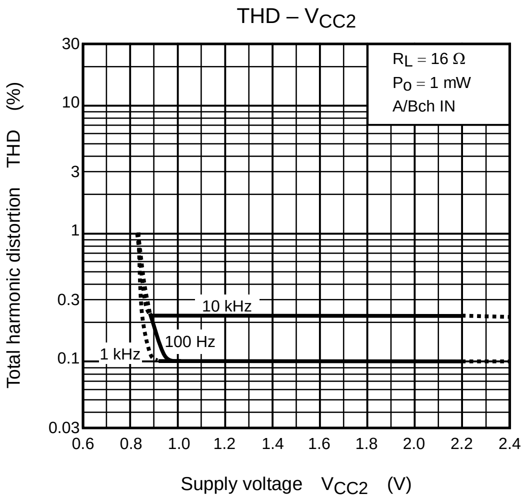


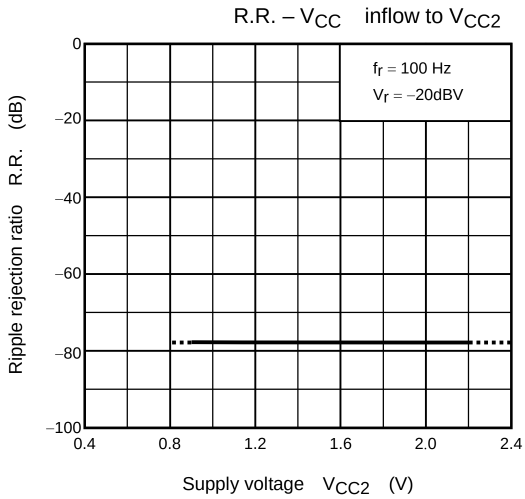


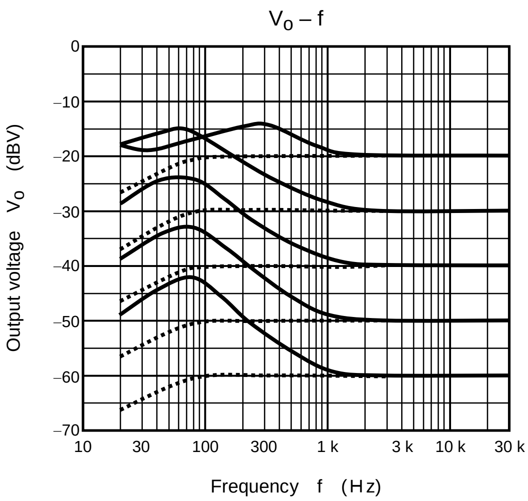


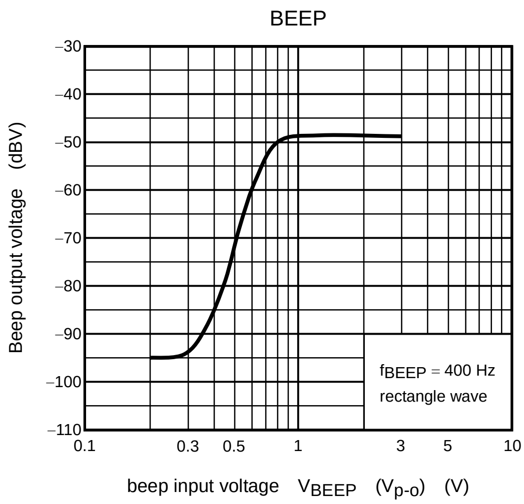

THD – P_o
Total harmonic distortion THD (%)
10
3
1
0.3
0.1
0.03
0.01
10 kHz
100 Hz/1 kHz
0.1 0.3 1 3 10 30 100 300
Output voltage P_o (mW)

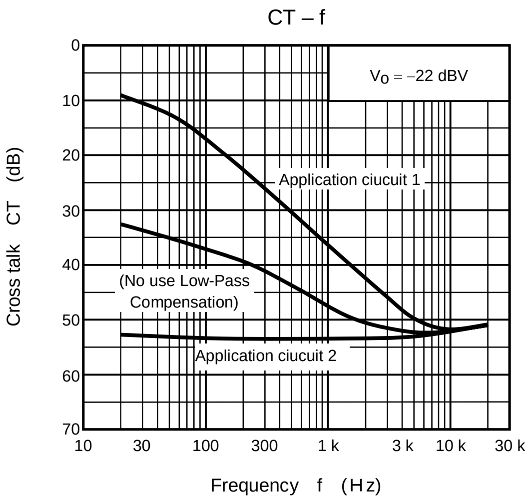

R.R. – V_{CC2} inflow to V_{CC1}
f_r = 100 Hz
V_r = −20dBV
Ripple rejection ratio R.R. (dB)
0
−20
−40
−60
−80
−100
0.4 0.8 1.2 1.6 2.0 2.4
Supply voltage V_{CC2} (V)

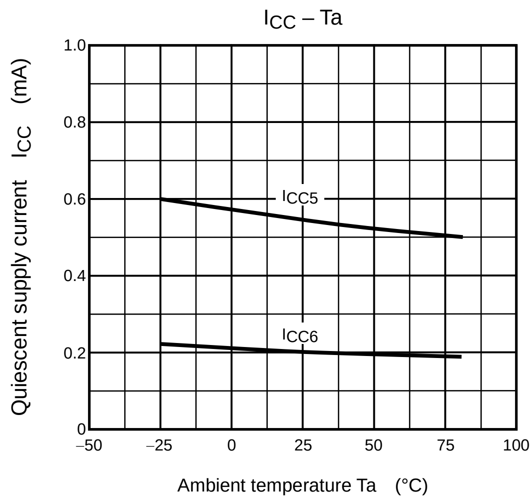

THD – V_{CC2}
R_L = 16 Ω
P_o = 1 mW
A/Bch IN
Total harmonic distortion THD (%)
30
10
3
1
0.3
0.1
0.03
10 kHz
100 Hz
1 kHz
0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4
Supply voltage V_{CC2} (V)

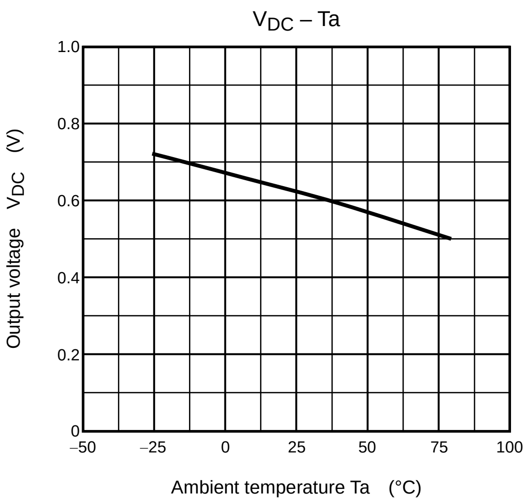

R.R. – V_{CC} inflow to V_{CC2}
f_r = 100 Hz
V_r = −20dBV
Ripple rejection ratio R.R. (dB)
0
−20
−40
−60
−80
−100
0.4 0.8 1.2 1.6 2.0 2.4
Supply voltage V_{CC2} (V)


V_o – f
Output voltage V_o (dBV)
0
−10
−20
−30
−40
−50
−60
−70
10 30 100 300 1 k 3 k 10 k 30 k
Frequency f (Hz)

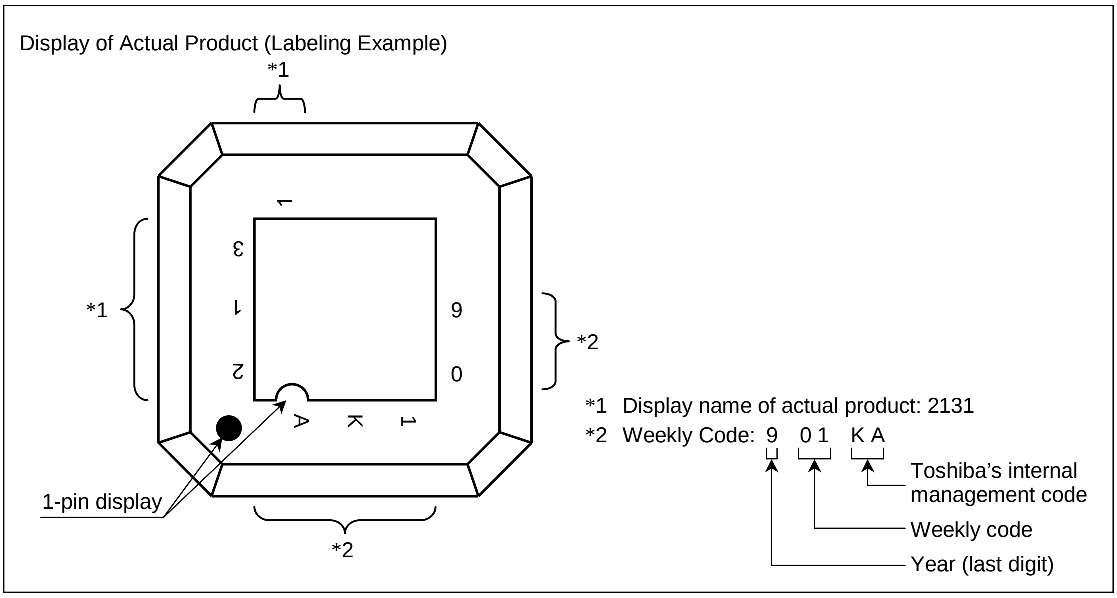

BEEP
Beep output voltage (dBV)
−30
−40
−50
−60
−70
−80
−90
−100
−110
f_{BEEP} = 400 Hz
rectangle wave
0.1 0.3 0.5 1 3 5 10
beep input voltage V_{BEEP} (V_{p-o}) (V)


CT – f
V_O = −22 dBV
Application ciucuit 1
(No use Low-Pass Compensation)
Application ciucuit 2
Cross talk CT (dB)
0
10
20
30
40
50
60
70
10
30
100
300
1 k
3 k
10 k
30 k
Frequency f (Hz)


I_{CC} – Ta
I_{CC5}
I_{CC6}
Quiescent supply current I_{CC} (mA)
1.0
0.8
0.6
0.4
0.2
0
–50
–25
0
25
50
75
100
Ambient temperature Ta (°C)

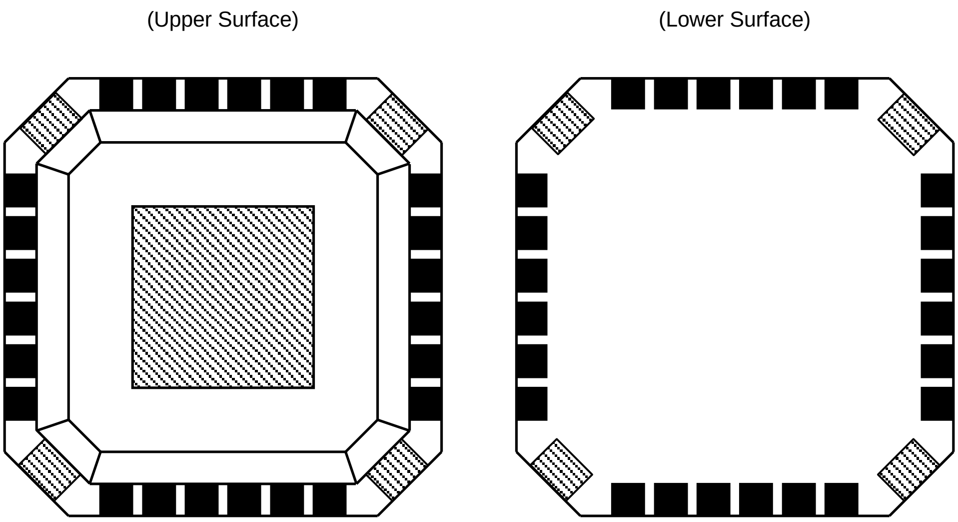

V_{DC} – Ta
Output voltage V_{DC} (V)
1.0
0.8
0.6
0.4
0.2
0
–50
–25
0
25
50
75
100
Ambient temperature Ta (°C)

Display of Actual Product



Requests Concerning Use of QON

Outline Drawing of Package



When using QON, please take into account the following items.

(1) Do not carry out soldering on the island section in the four corners of the package (the section shown on the lower surface drawing with diagonal lines) with the aim of increasing mechanical strength.

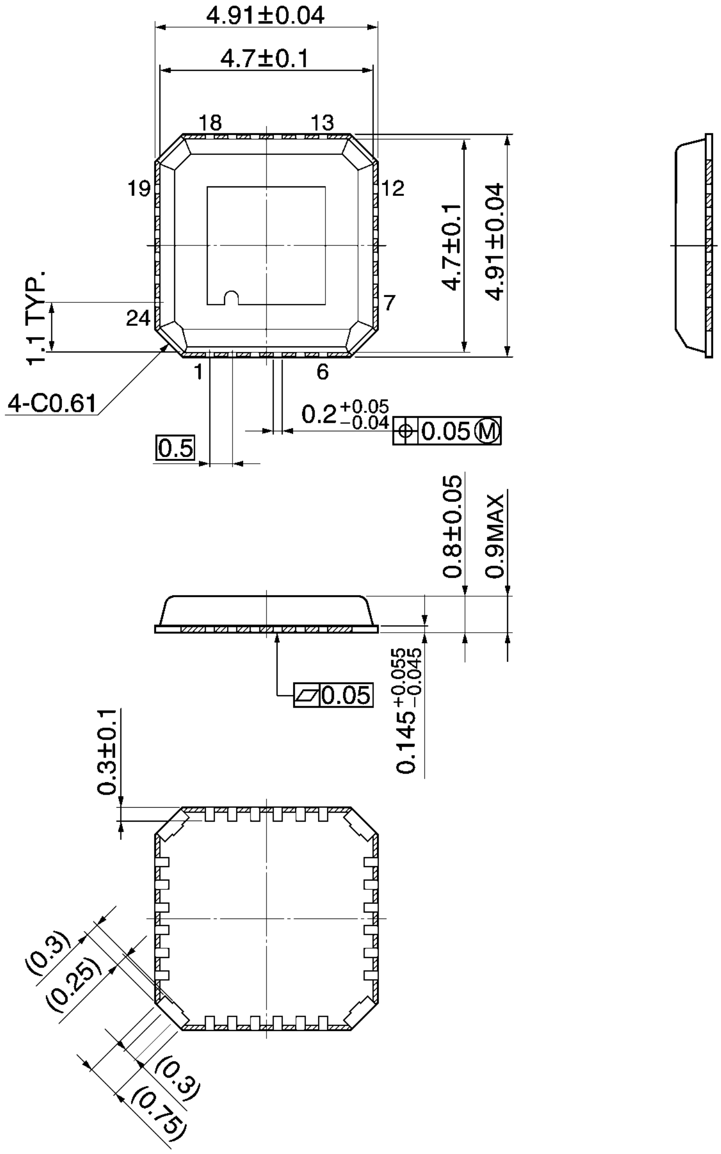
(2) The island section exposed on the package surface (the section shown on the upper surface drawing with diagonal lines) must be used as *1 below while electrically insulated from outside.

Note 1: Ensure that the island section (the section shown on the lower surface drawing with diagonal lines) does not come into contact with solder from through-holes on the board layout.

- When mounting or soldering, take care to ensure that neither static electricity nor electrical overstress is applied to the IC (measures to prevent anti-static, leaks, etc.).
- When incorporating into a set, adopt a set design that does not apply voltage directly to the island section.

Package Dimensions

QON24-P-0505-0.50 Unit: mm



Note 1) The solder plating portion in four corners of tne package shall not be treated as an external terminal.

Note 2) Don`t carry out soldering to four corners of the package.

Note 3) [hatched box] area : Resin surface

Weight: 0.05 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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