TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6L79

Source Driver for TFT LCD Panels

The T6L79 is a 64-grayscale-level and 384-channel output source driver for TFT LCD panels. The device accepts 8-bit × 6-dot digital CMOS-level inputs, for which the direction of data transfer can be selected by the U/D pin. The 10 (5 × 2) external power supply and the internal DA converter realize display of 260,000 colors, on which reference analog voltage inputs is made.

The DA converter supports one side dot line inversion, achieving high picture quality. The output dynamic range is a generous 7.3 to 9.8 Vp-p.

Base on high-speed CMOS, the T6L79 offers both low power consumption and high-speed operation. To configure an SXGA or XGA-compatible TFT-LCD module, it allows a maximum operating frequency 45 MHz.

Unit: mm

T6L79	User Pitch Area	
	IN	OUT

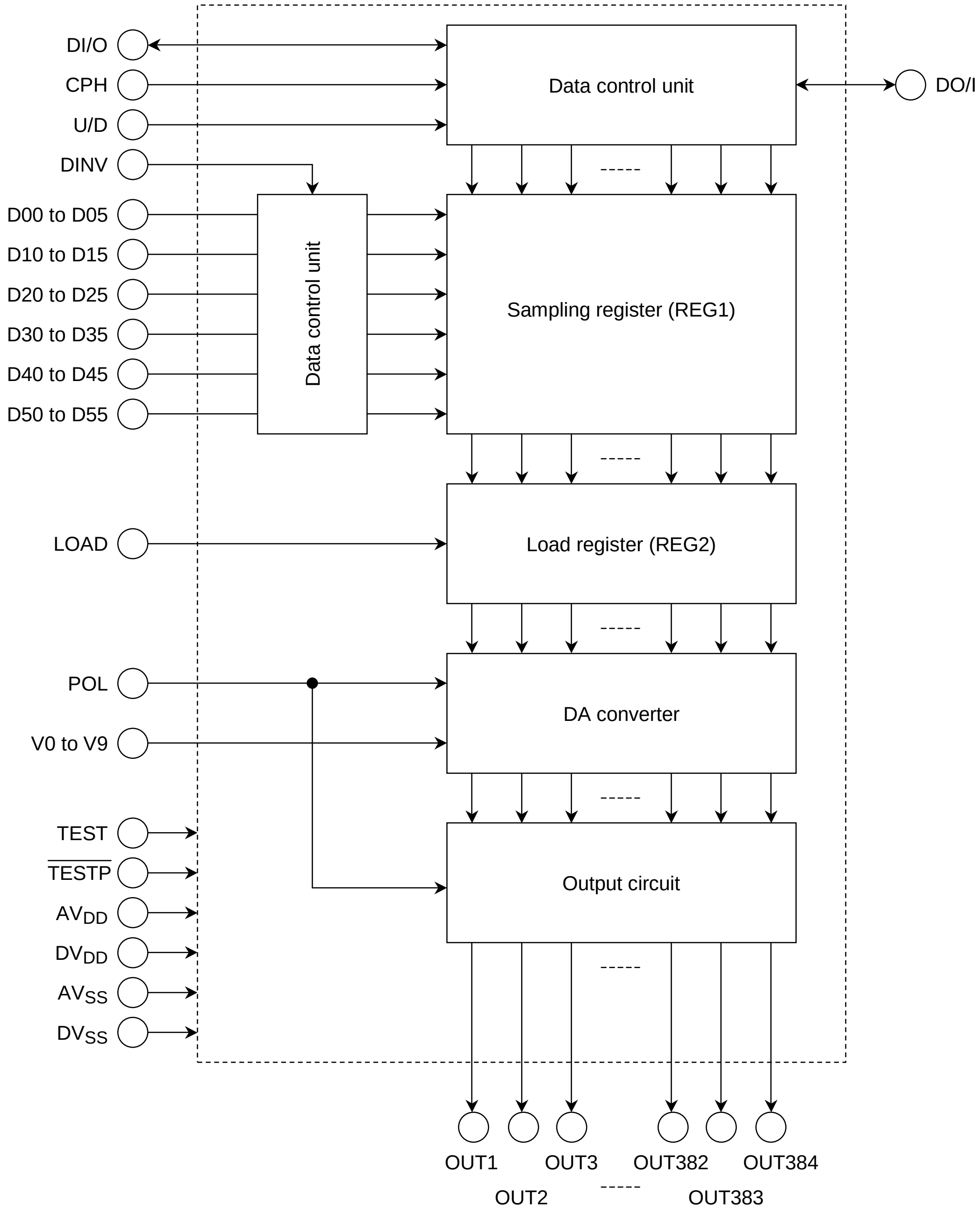
For the latest TCP specifications and product line-up, contact Toshiba or your local sales office.

TCP (Tape Carrier Package)

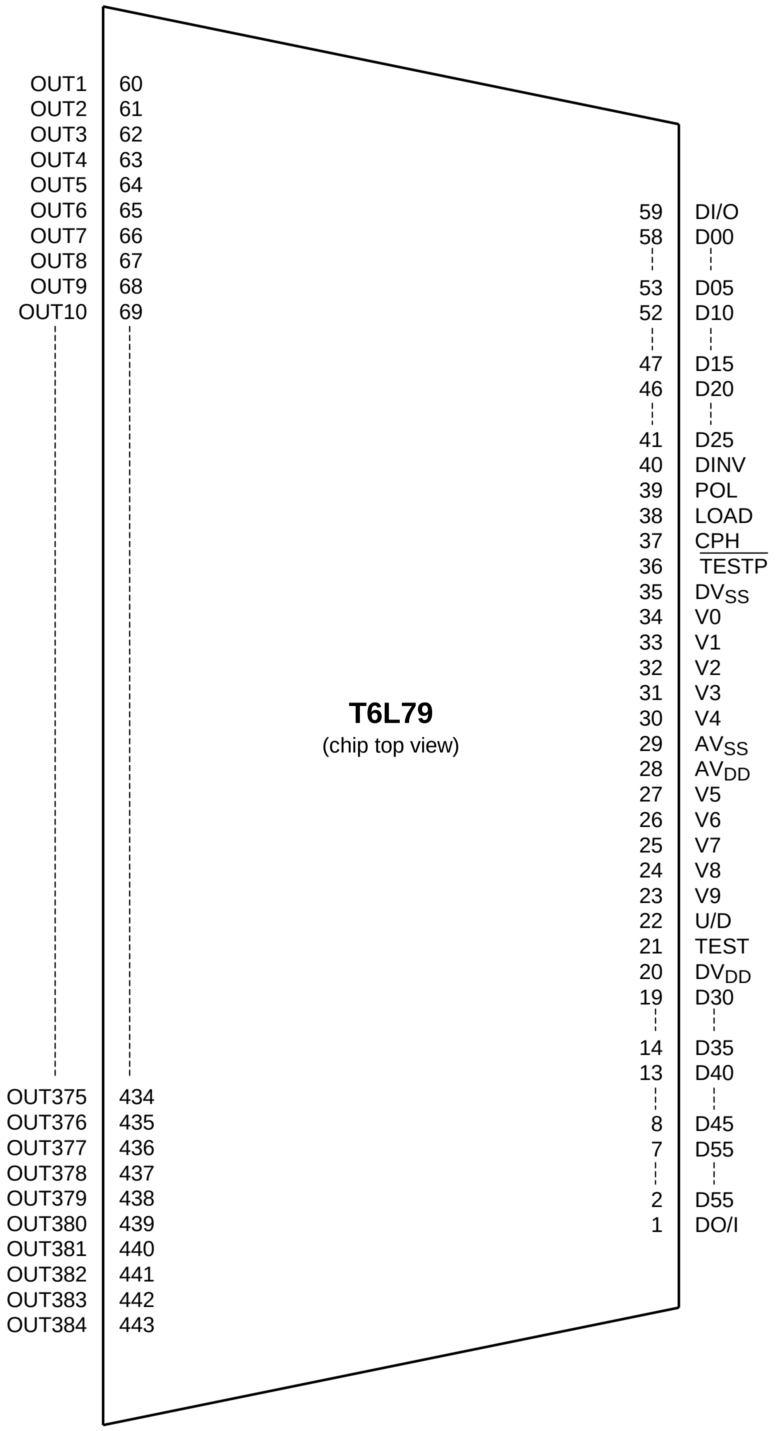
Features

- Grayscale data : Digital CMOS-level 36-bit (6-bit × 6-input) parallel transfer method, selectable transfer direction
- Panel drive outputs : 384 outputs, 64 grayscale levels, R-DAC system, reference analog voltage inputs, 10 external power supplies (5 × 2), one side dot line inversion drive
- High-speed operation : 45 MHz max
- Power supply voltage : Digital power supply voltage . . . 3.0 to 3.6 V
  Analog power supply voltage . . . 7.5 to 10.0 V
- Operating temperature: −20 to 75°C
- Package: Tape carrier package (TCP)
- Cascading of multiple devices

Block Diagram



Pin Assignment



The figure above shows an example of the pin assignment in the TCP. It does not specify the pad layout on the chip. For the latest TCP specifications, contact Toshiba or your local sales office.

Pin Functions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Data transfer enable pins
These pins are used to input/output grayscale data.
Input and output are switched as shown below according to the setting of the U/D pin.
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
When DI/O or DO/I is set to input
High level input to the pin is latched into the internal logic in sync with the rising edge of CPH. If the internal logic is in standby state, the device is ready for data transfer. Grayscale data are sequentially latched starting from the next rising edge of CPH.
When DI/O or DO/I is set to output
Sends enable signal to the T6L79 at the next stage of the LCD driver. After outputting High level, the pin enters standby state.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer direction select pin
Controls the transfer direction of grayscale data. The data are transferred in the following order in sync with the rising edge of CPH:
When U/D = High: OUT1 to OUT6, OUT7 to OUT12 . . . OUT379 to OUT384
When U/D = Low: OUT379 to OUT384, OUT373 to OUT378 . . . OUT1 to OUT6
The voltage applied to this pin must be DC level, High or Low.</td></tr>
<tr><td>CPH</td><td>I</td><td>Data transfer clock pin
Transfers grayscale data. Sequentially latches grayscale data into REG1 in sync with the rising edge of CPH. Input clocks at least three cycles after High level of the LOAD pin.</td></tr>
<tr><td>D00 to D05
D10 to D15
D20 to D25
D30 to D35
D40 to D45
D50 to D55</td><td>I</td><td>Grayscale data bus pins
Inputs output data consisting of 6 bits for six channels in one transfer. The relationship between grayscale data and output pins is as follows:
Grayscale data $= 32 \times Dn5 + 16 \times Dn4 + 8 \times Dn3 + 4 \times Dn2 + 2 \times Dn1 + Dn0$
(*) $n = 0, 1, . . . , 5$</td></tr>
<tr><td>LOAD</td><td>I</td><td>Data load input pin
High level input to the pin is latched into the internal logic in sync with the rising edge of CPH. Then, the REG1 data are transferred to REG2. The voltage changes to that corresponding to grayscale data in sync with the falling edge of LOAD.</td></tr>
<tr><td>DINV</td><td>I</td><td>Data polarity inverting pin
Selects inversion or non-inversion of grayscale data bus at the rising edge of CPH.
DINV = Low: Data bus not inverted
DINV = High: Data bus inverted
"H" or "L" level is discriminated at the rising edge of CPH same as gray data bus.</td></tr>
<tr><td>POL</td><td>I</td><td>Polarity inverting pin
Latches the input signal into the internal logic in sync with the rising edge of LOAD.
POL = Low: The reference voltage for odd-numbered outputs is input from V0 to V4; for even-numbered outputs, V5 to V9.
POL = High: The reference voltage for odd-numbered outputs is input from V5 to V9; for even-numbered outputs, V0 to V4.</td></tr>
<tr><td>V0 to V9</td><td>I</td><td>Reference analog voltage input pins
Externally input reference analog voltage inputs voltage.
Hold the input voltage during output of the voltage corresponding to grayscale data.
$AV_{DD} - 0.1 > V0 > V1 > V2 > V3 > V4 > 0.5 \times AV_{DD} > V5 > V6 > V7 > V8 > V9 > AV_{SS} + 0.1$</td></tr>
<tr><td>TEST</td><td>I</td><td>Test pin
Leave the pin open or set to DV_{SS} level.</td></tr>
<tr><td>$\overline{\text{TESTP}}$</td><td>I</td><td>Test pin
Controlling the output amp constant current supply reduces current dissipation.
In Low Power Mode ($\overline{\text{TESTP}}$ = Low), current dissipation is reduced to 2/3 of the value in Normal Current Dissipation Mode. The pin is internally pulled up to DV_{DD}.
$\overline{\text{TESTP}}$ = High or the pin left open: Normal Current Dissipation Mode
$\overline{\text{TESTP}}$ = Low: Low-Current-Dissipation Mode</td></tr>
<tr><td>OUT1 to OUT384</td><td>O</td><td>LCD panel drive pins</td></tr>
<tr><td>AV_{DD}</td><td></td><td>Analog power supply pin</td></tr>
<tr><td>AV_{SS}</td><td></td><td>Analog GND pin
Apply the same voltage as that of digital GND pin.</td></tr>
<tr><td>DV_{DD}</td><td></td><td>Digital power supply pin</td></tr>
<tr><td>DV_{SS}</td><td></td><td>Digital GND pin
Apply the same voltage as that of analog GND pin.</td></tr>
</table>

Device Operation

(1) Starting data transfer

High level input to the data transfer enable pin (DI/O or DO/I) is latched into the internal logic in sync with the rising edge of CPH, setting the device to ready for transfer.

Set the period for High level input to the data transfer enable pin to one clock.

(2) Data transfer method

Grayscale data are transferred from the data bus to the sampling register (REG1) in sync with the rising edge of CPH. Grayscale data for six channels are simultaneously written in one transfer. Transfer completes after 64 times and the device enters standby state. Data to be written to REG1 are the result of operations between the grayscale data bus and DINV.

Note 1: Do not input High level to LOAD during data transfer.

(3) Ending data transfer

High level is output from the data transfer enable pin (DO/I or DI/O) from the rising edge of CPH, one cycle before the last data are latched, to the next rising edge of CPH.

(4) LCD panel drive output

Inputting High level to LOAD in sync with the rising edge of CPH following High level output from DO/I (DI/O) transfers data from the sampling register (REG1) to the load register (REG2) and outputs a voltage corresponding to the grayscale data in sync with the falling edge of LOAD.

Note 2: Input High level to LOAD at least three clock cycles.

The T6L79 has a capacity for polarity inverting corresponding to dot-inverting operation. By POL signal to the pin which is latched into the internal logic in sync with the rising edge of LOAD, the polarity of odd-numbered outputs and even-numbered outputs are inverted.

By changing the cycle of POL signal, n-line inverting operation is available to correspond.

POL = "L"	The reference voltage for odd-numbered outputs is input from V0 to V4, for even-numbered outputs, V5 to V9
POL = "H"	The reference voltage for odd-numbered outputs is input from V5 to V9, for even-numbered outputs, V0 to V4

(5) $\overline{\text{TESTP}}$ (Low power control function)

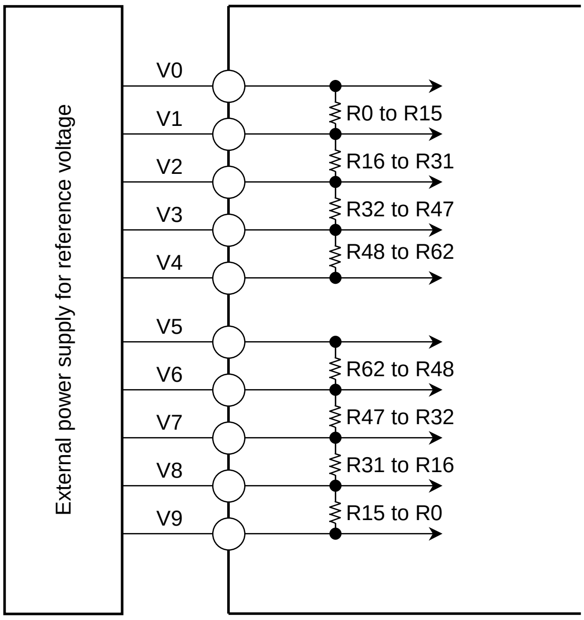
Output amp bias current can be switched between two values using the $\overline{\text{TESTP}}$ pin. The current dissipation in Low Current Dissipation Mode can be reduced to 2/3 of that in Normal Current Dissipation mode.

Note 3: Input the stabilized DC voltage (DV_{DD}, DV_{SS}) to the $\overline{\text{TESTP}}$ pin.

$\overline{\text{TESTP}}$ = "H"	$\overline{\text{TESTP}}$ = "L"
Normal current dissipation mode	Low current dissipation mode

(6) Reference analog voltage inputs power supply circuit

The DA converter consists of ladder resistors and switches. Resistors are serially connected between the supply voltage input pins for reference analog voltage inputs.



- **Resistors between power supply pins for reference analog voltage inputs (typical)**

Unit: Ω

Resistor Name	Resistance Values	Resistor Name	Resistance Values	Resistor Name	Resistance Values	Resistor Name	Resistance Values
R_0	648.0	R_{16}	243.0	R_{32}	81.0	R_{48}	81.0
R_1	607.5	R_{17}	202.5	R_{33}	81.0	R_{49}	81.0
R_2	567.0	R_{18}	202.5	R_{34}	81.0	R_{50}	81.0
R_3	526.5	R_{19}	202.5	R_{35}	81.0	R_{51}	81.0
R_4	486.0	R_{20}	162.0	R_{36}	81.0	R_{52}	81.0
R_5	445.5	R_{21}	162.0	R_{37}	81.0	R_{53}	121.5
R_6	445.5	R_{22}	162.0	R_{38}	81.0	R_{54}	121.5
R_7	405.0	R_{23}	121.5	R_{39}	81.0	R_{55}	121.5
R_8	405.0	R_{24}	121.5	R_{40}	81.0	R_{56}	162.0
R_9	324.0	R_{25}	121.5	R_{41}	81.0	R_{57}	162.0
R_{10}	324.0	R_{26}	121.5	R_{42}	81.0	R_{58}	202.5
R_{11}	283.5	R_{27}	81.0	R_{43}	81.0	R_{59}	202.5
R_{12}	283.5	R_{28}	81.0	R_{44}	81.0	R_{60}	243.0
R_{13}	283.5	R_{29}	81.0	R_{45}	81.0	R_{61}	405.0
R_{14}	243.0	R_{30}	81.0	R_{46}	81.0	R_{62}	648.0
R_{15}	243.0	R_{31}	81.0	R_{47}	81.0		

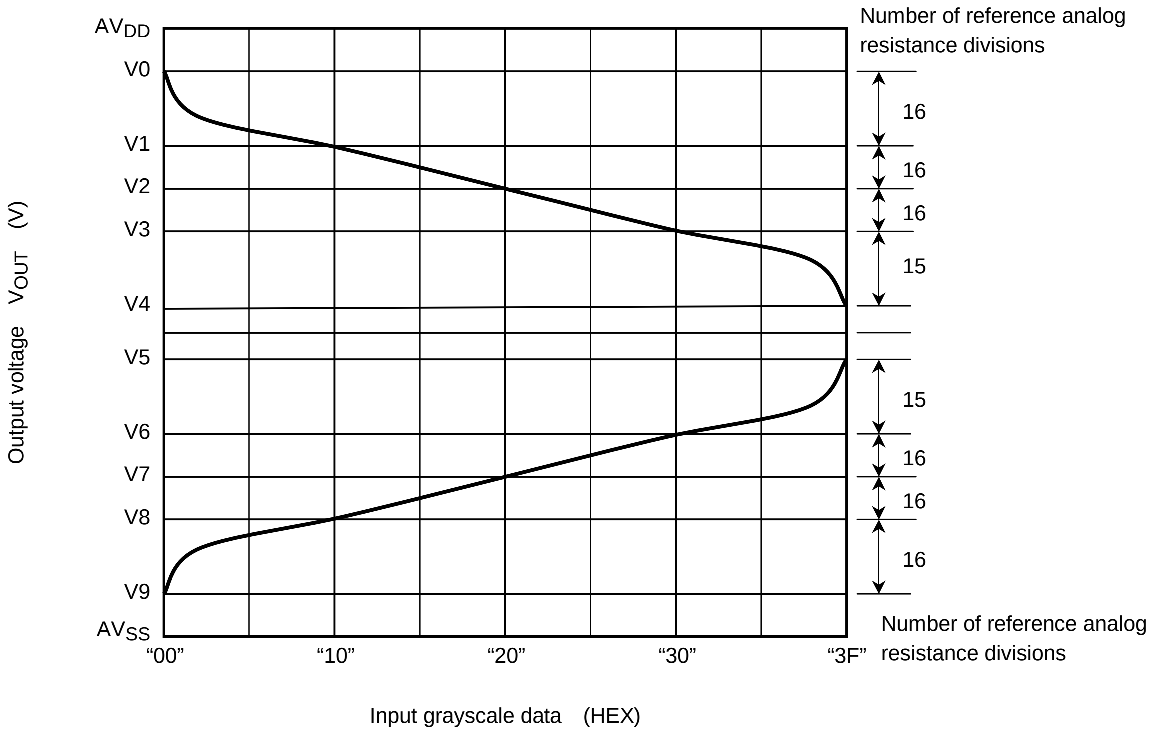
(7) Relationship between grayscale data and output voltage

The output voltage is determined according to the grayscale data values and the ten power supply voltages for reference analog voltage inputs. When U/D is High or Low, the grayscale data and the output pins correspond as shown in the table below.

Grayscale Data	Output	
	U/D = “H”	U/D = “L”
D00 to D05	OUT (6m – 5)	OUT (6p – 5)
D10 to D15	OUT (6m – 4)	OUT (6 p – 4)
D20 to D25	OUT (6m – 3)	OUT (6p – 3)
D30 to D35	OUT (6m – 2)	OUT (6p – 2)
D40 to D45	OUT (6m – 1)	OUT (6p – 1)
D50 to D55	OUT (6m)	OUT (6p)

(*) m = 1, 2, 3, • • • , 62, 63, 64
p = 64, 63, 62, • • • , 3, 2, 1

- **Schematic of reference analog voltage inputs**



- **Relationship 1 between grayscale data and output voltage (grayscale data: 00H to 1FH)**

(*) n = 0, 1, • • •, 5

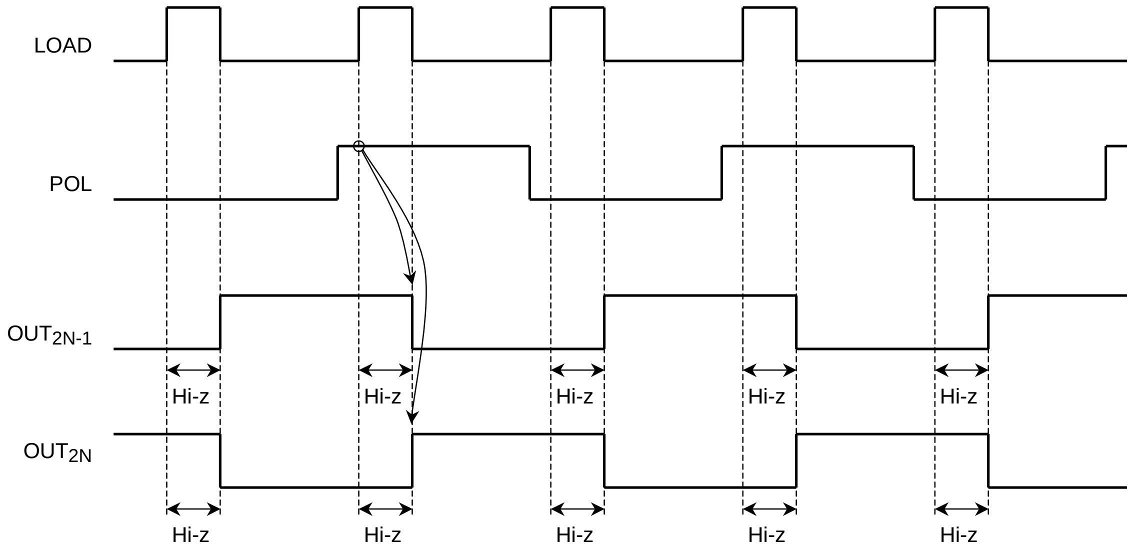
Grayscale Data	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	Output Voltage (reference value) V5 < V4 < V3 < V2 < V1 < V0 < AV_{DD}, DINV = L		AV_{SS} < V9 < V8 < V7 < V6 < V5 < V4, DINV = L	
00H	0	0	0	0	0	0	V00H	V0	V00H’	V9
01H	0	0	0	0	0	1	V01H	V1 + (V0 − V1) × 5872.5/6520.5	V01H’	V9 + (V8−V9) × 648.0/6520.5
02H	0	0	0	0	1	0	V02H	V1 + (V0 − V1) × 5265.0/6520.5	V02H’	V9 + (V8−V9) × 1255.5/6520.5
03H	0	0	0	0	1	1	V03H	V1 + (V0 − V1) × 4698.0/6520.5	V03H’	V9 + (V8−V9) × 1822.5/6520.5
04H	0	0	0	1	0	0	V04H	V1 + (V0 − V1) × 4171.5/6520.5	V04H’	V9 + (V8−V9) × 2349.0/6520.5
05H	0	0	0	1	0	1	V05H	V1 + (V0 − V1) × 3685.5/6520.5	V05H’	V9 + (V8−V9) × 2835.0/6520.5
06H	0	0	0	1	1	0	V06H	V1 + (V0 − V1) × 3240.0/6520.5	V06H’	V9 + (V8−V9) × 3280.5/6520.5
07H	0	0	0	1	1	1	V07H	V1 + (V0 − V1) × 2794.5/6520.5	V07H’	V9 + (V8−V9) × 3726.0/6520.5
08H	0	0	1	0	0	0	V08H	V1 + (V0 − V1) × 2389.5/6520.5	V08H’	V9 + (V8−V9) × 4131.0/6520.5
09H	0	0	1	0	0	1	V09H	V1 + (V0 − V1) × 1984.5/6520.5	V09H’	V9 + (V8−V9) × 4536.0/6520.5
0AH	0	0	1	0	1	0	V0AH	V1 + (V0 − V1) × 1660.5/6520.5	V0AH’	V9 + (V8 − V9) × 4860.0/6520.5
0BH	0	0	1	0	1	1	V0BH	V1 + (V0 − V1) × 1336.5/6520.5	V0BH’	V9 + (V8 − V9) × 5184.0/6520.5
0CH	0	0	1	1	0	0	V0CH	V1 + (V0 − V1) × 1053.0/6520.5	V0CH’	V9 + (V8 − V9) × 5467.5/6520.5
0DH	0	0	1	1	0	1	V0DH	V1 + (V0 − V1) × 769.5/6520.5	V0DH’	V9 + (V8 − V9) × 5751.0/6520.5
0EH	0	0	1	1	1	0	V0EH	V1 + (V0 − V1) × 486.0/6520.5	V0EH’	V9 + (V8 − V9) × 6034.5/6520.5
0FH	0	0	1	1	1	1	V0FH	V1 + (V0 − V1) × 243.0/6520.5	V0FH’	V9 + (V8 − V9) × 6277.5/6520.5
10H	0	1	0	0	0	0	V10H	V1	V10H’	V8
11H	0	1	0	0	0	1	V11H	V2 + (V1 − V2) × 1984.5/2227.5	V11H’	V8 + (V7 − V8) × 243.0/2227.5
12H	0	1	0	0	1	0	V12H	V2 + (V1 − V2) × 1782.0/2227.5	V12H’	V8 + (V7 − V8) × 445.5/2227.5
13H	0	1	0	0	1	1	V13H	V2 + (V1 − V2) × 1579.5/2227.5	V13H’	V8 + (V7 − V8) × 648.0/2227.5
14H	0	1	0	1	0	0	V14H	V2 + (V1 − V2) × 1377.0/2227.5	V14H’	V8 + (V7 − V8) × 850.5/2227.5
15H	0	1	0	1	0	1	V15H	V2 + (V1 − V2) × 1215.0/2227.5	V15H’	V8 + (V7 − V8) × 1012.5/2227.5
16H	0	1	0	1	1	0	V16H	V2 + (V1 − V2) × 1053.0/2227.5	V16H’	V8 + (V7 − V8) × 1174.5/2227.5
17H	0	1	0	1	1	1	V17H	V2 + (V1 − V2) × 891.0/2227.5	V17H’	V8 + (V7 − V8) × 1336.5/2227.5
18H	0	1	1	0	0	0	V18H	V2 + (V1 − V2) × 769.5/2227.5	V18H’	V8 + (V7 − V8) × 1458.0/2227.5
19H	0	1	1	0	0	1	V19H	V2 + (V1 − V2) × 648.0/2227.5	V19H’	V8 + (V7 − V8) × 1579.5/2227.5
1AH	0	1	1	0	1	0	V1AH	V2 + (V1 − V2) × 526.5/2227.5	V1AH’	V8 + (V7 − V8) × 1701.0/2227.5
1BH	0	1	1	0	1	1	V1BH	V2 + (V1 − V2) × 405.0/2227.5	V1BH’	V8 + (V7 − V8) × 1822.5/2227.5
1CH	0	1	1	1	0	0	V1CH	V2 + (V1 − V2) × 324.0/2227.5	V1CH’	V8 + (V7 − V8) × 1903.5/2227.5
1DH	0	1	1	1	0	1	V1DH	V2 + (V1 − V2) × 243.0/2227.5	V1DH’	V8 + (V7 − V8) × 1984.5/2227.5
1EH	0	1	1	1	1	0	V1EH	V2 + (V1 − V2) × 162.0/2227.5	V1EH’	V8 + (V7 − V8) × 2065.5/2227.5
1FH	0	1	1	1	1	1	V1FH	V2 + (V1 − V2) × 81.0/2227.5	V1FH’	V8 + (V7 − V8) × 2146.5/2227.5

- **Relationship 2 between grayscale data and output voltage (grayscale data: 20H to 3FH)**

(*) n = 0, 1, • • •, 5

Grayscale Data	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	Output Voltage (reference value)			
							V5 < V4 < V3 < V2 < V1 < V0 < AV_{DD}, DINV = L		AV_{SS} < V9 < V8 < V7 < V6 < V5 < V4, DINV = L	
20H	1	0	0	0	0	0	20H	V2	20H'	V7
21H	1	0	0	0	0	1	21H	V3 + (V2 − V3) × 1215.0/1296.0	21H'	V7 + (V6 − V7) × 81.0/1296.0
22H	1	0	0	0	1	0	22H	V3 + (V2 − V3) × 1134.0/1296.0	22H'	V7 + (V6 − V7) × 162.0/1296.0
23H	1	0	0	0	1	1	23H	V3 + (V2 − V3) × 1053.0/1296.0	23H'	V7 + (V6 − V7) × 243.0/1296.0
24H	1	0	0	1	0	0	24H	V3 + (V2 − V3) × 972.0/1296.0	24H'	V7 + (V6 − V7) × 324.0/1296.0
25H	1	0	0	1	0	1	25H	V3 + (V2 − V3) × 891.0/1296.0	25H'	V7 + (V6 − V7) × 405.0/1296.0
26H	1	0	0	1	1	0	26H	V3 + (V2 − V3) × 810.0/1296.0	26H'	V7 + (V6 − V7) × 486.0/1296.0
27H	1	0	0	1	1	1	27H	V3 + (V2 − V3) × 729.0/1296.0	27H'	V7 + (V6 − V7) × 567.0/1296.0
28H	1	0	1	0	0	0	28H	V3 + (V2 − V3) × 648.0/1296.0	28H'	V7 + (V6 − V7) × 648.0/1296.0
29H	1	0	1	0	0	1	29H	V3 + (V2 − V3) × 567.0/1296.0	29H'	V7 + (V6 − V7) × 729.0/1296.0
2AH	1	0	1	0	1	0	2AH	V3 + (V2 − V3) × 486.0/1296.0	2AH'	V7 + (V6 − V7) × 810.0/1296.0
2BH	1	0	1	0	1	1	2BH	V3 + (V2 − V3) × 405.0/1296.0	2BH'	V7 + (V6 − V7) × 891.0/1296.0
2CH	1	0	1	1	0	0	2CH	V3 + (V2 − V3) × 324.0/1296.0	2CH'	V7 + (V6 − V7) × 972.0/1296.0
2DH	1	0	1	1	0	1	2DH	V3 + (V2 − V3) × 243.0/1296.0	2DH'	V7 + (V6 − V7) × 1053.0/1296.0
2EH	1	0	1	1	1	0	2EH	V3 + (V2 − V3) × 162.0/1296.0	2EH'	V7 + (V6 − V7) × 1134.0/1296.0
2FH	1	0	1	1	1	1	2FH	V3 + (V2 − V3) × 81.0/1296.0	2FH'	V7 + (V6 − V7) × 1215.0/1296.0
30H	1	1	0	0	0	0	30H	V3	30H'	V6
31H	1	1	0	0	0	1	31H	V4 + (V3 − V4) × 2713.5/2794.5	31H'	V6 + (V5−V6) × 81.0/2794.5
32H	1	1	0	0	1	0	32H	V4 + (V3 − V4) × 2632.5/2794.5	32H'	V6 + (V5−V6) × 162.0/2794.5
33H	1	1	0	0	1	1	33H	V4 + (V3 − V4) × 2551.5/2794.5	33H'	V6 + (V5−V6) × 243.0/2794.5
34H	1	1	0	1	0	0	34H	V4 + (V3 − V4) × 2470.5/2794.5	34H'	V6 + (V5−V6) × 324.0/2794.5
35H	1	1	0	1	0	1	35H	V4 + (V3 − V4) × 2389.5/2794.5	35H'	V6 + (V5−V6) × 405.0/2794.5
36H	1	1	0	1	1	0	36H	V4 + (V3 − V4) × 2268.0/2794.5	36H'	V6 + (V5−V6) × 526.5/2794.5
37H	1	1	0	1	1	1	37H	V4 + (V3 − V4) × 2146.5/2794.5	37H'	V6 + (V5−V6) × 648.0/2794.5
38H	1	1	1	0	0	0	38H	V4 + (V3 − V4) × 2025.0/2794.5	38H'	V6 + (V5−V6) × 769.5/2794.5
39H	1	1	1	0	0	1	39H	V4 + (V3 − V4) × 1863.0/2794.5	39H'	V6 + (V5−V6) × 931.5/2794.5
3AH	1	1	1	0	1	0	3AH	V4 + (V3 − V4) × 1701.0/2794.5	3AH'	V6 + (V5−V6) × 1093.5/2794.5
3BH	1	1	1	0	1	1	3BH	V4 + (V3 − V4) × 1498.5/2794.5	3BH'	V6 + (V5−V6) × 1296.0/2794.5
3CH	1	1	1	1	0	0	3CH	V4 + (V3 − V4) × 1296.0/2794.5	3CH'	V6 + (V5−V6) × 1498.5/2794.5
3DH	1	1	1	1	0	1	3DH	V4 + (V3 − V4) × 1053.0/2794.5	3DH'	V7 + (V5−V6) × 1741.5/2794.5
3EH	1	1	1	1	1	0	3EH	V4 + (V3 − V4) × 648.0/2794.5	3EH'	V7 + (V5−V6) × 2146.5/2794.5
3FH	1	1	1	1	1	1	3FH	V4	3FH'	V5

- **Relationship between LOAD and POL output waveforms**

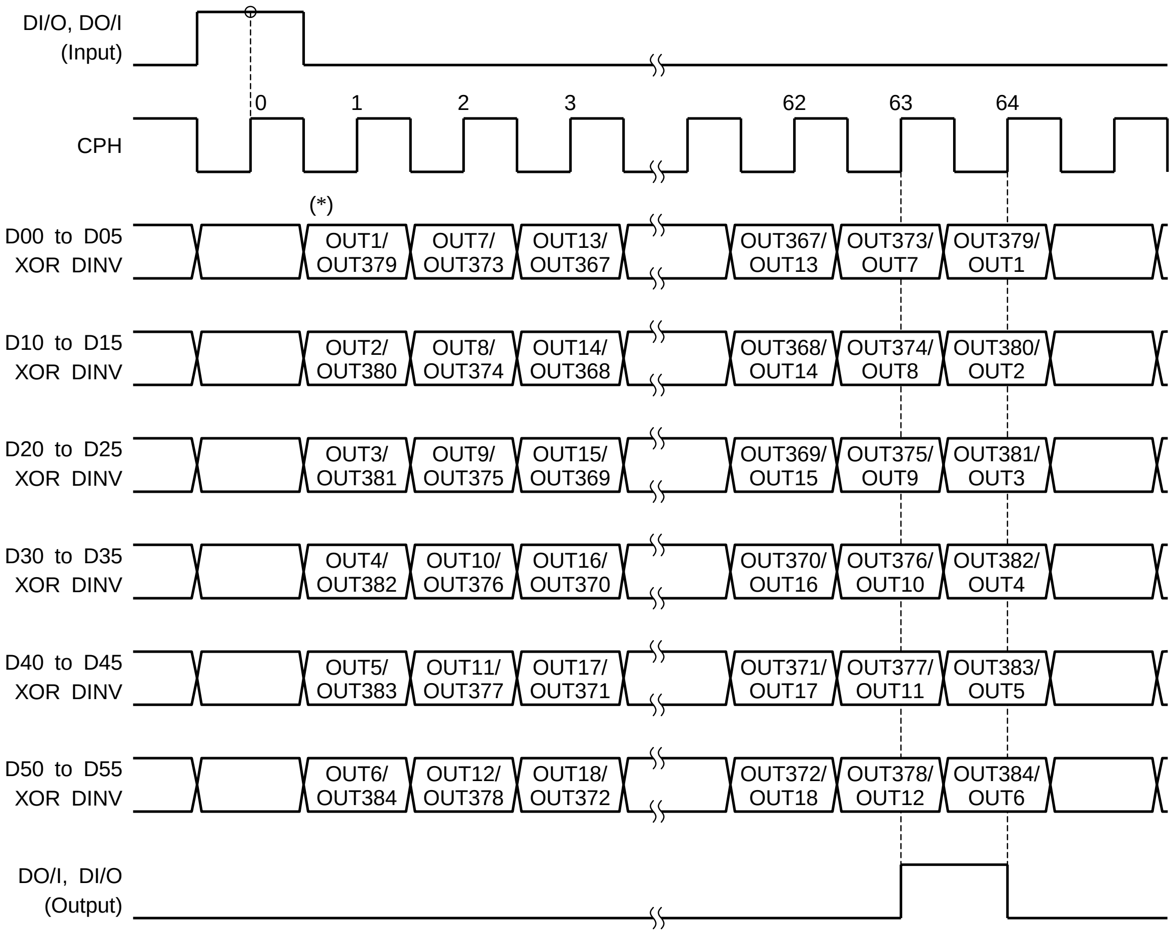


POL	OUT_{2N-1}	OUT_{2N}
L	V0 to V4	V5 to V9
H	V5 to V9	V0 to V4

(*) OUT_{2N-1} (odd-numbered outputs)
OUT_{2N} (even-numbered outputs)

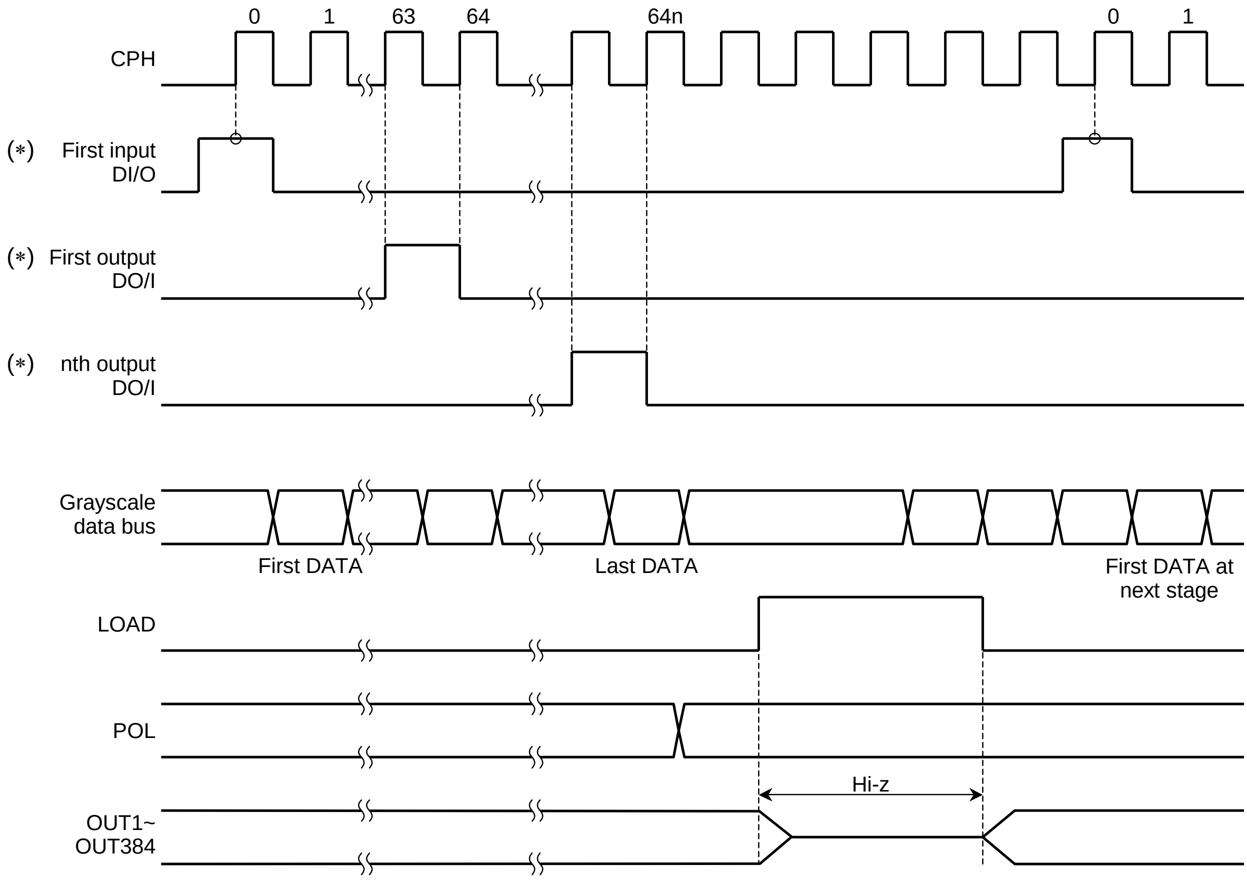
Timing Chart

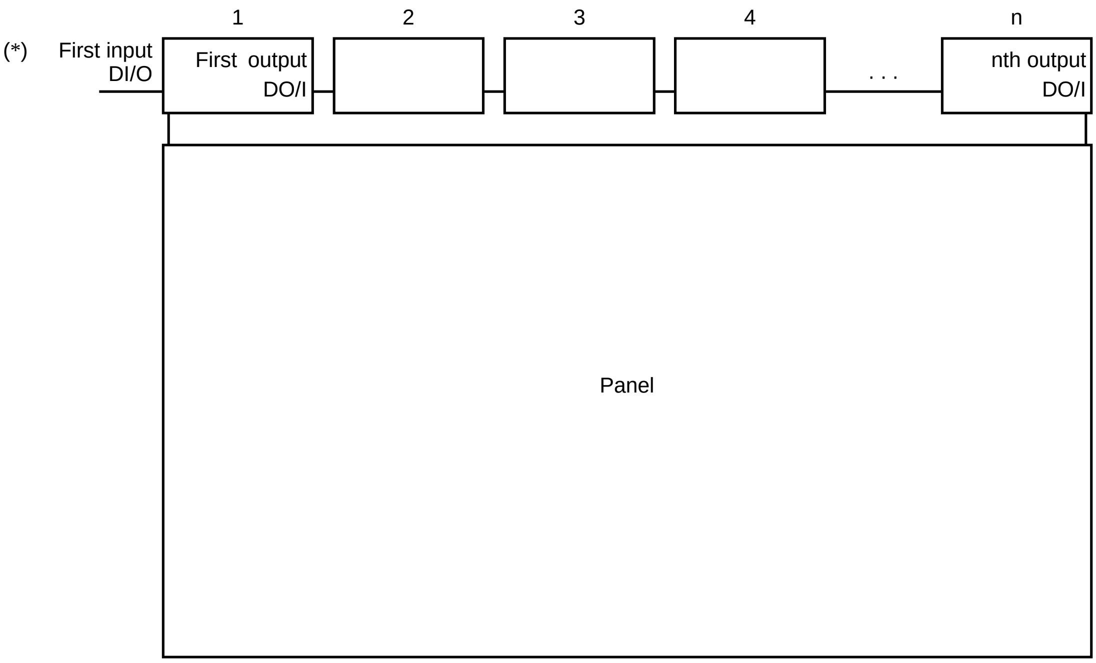
- **Start pulse and data sequence**



(*) Upper: OUT1 → U/D = High level
Lower: OUT379 → U/D = Low level

- **Loading and cascading operation**





Maximum Ratings ($DV_{SS} = AV_{SS} = 0$ V)

Characteristics	Symbol	Rating	Unit	Applicable Pin
Digital supply voltage	DV_{DD}	−0.3 to 4.0	V	
Analog supply voltage	AV_{DD}	−0.3 to 11.0	V	
Gamma correction voltage	V (0:9)	−0.3 to AV_{DD} + 0.3	V	V0 to V9
Digital input voltage	V_{IN}	−0.3 to DV_{DD} + 0.3	V	
Storage temperature	T_{stg}	−55 to 125	°C	

Operating Range ($DV_{SS} = AV_{SS} = 0$ V)

Characteristics	Symbol	Rating	Unit	Applicable Pin
Digital supply voltage	DV_{DD}	3.0 to 3.6	V	
Analog supply voltage	AV_{DD}	7.5 to 10.0	V	
Gamma correction voltage	V (0:9)	0.1 to AV_{DD} − 0.1	V	V0 to V9
Operating temperature	T_{opr}	−20 to 75	°C	
Operating frequency	f_{CPH}	40 (max)	MHz	CPH
Output load capacitance	C_L	75	pF/PIN	OUT1 to OUT384
Input capacitance	C_{IN}	8 (max)	pF	DI/O, DO/I
		5 (max)		Input pins except DI/O, DO/I

Electrical Characteristics

DC Characteristics

(DV_{DD} = 3.0 to 3.6 V, AV_{DD} = 7.5 to 10.0 V, DV_{SS} = AV_{SS} = 0 V, Ta = –20 to 75°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Pin
Input voltage	Low level	V_{IL}	—	—	0	—	0.3 × DV_{DD}	V	Logic input
	High level	V_{IH}		—	0.7 × DV_{DD}	—	DV_{DD}		
Output voltage	Low level	V_{OL}	—	I_{OL} =1 mA	0	—	0.5	V	Logic output
	High level	V_{OH}		I_{OH} = –1 mA	DV_{DD} – 0.5	—	—		
Output voltage range		VDO	—	—	AV_{SS} + 0.1	—	AV_{DD} – 0.1	V	OUT1 to OUT384
Output voltage deviation		ΔV_O	—	(Note 4)	–20	—	20	mV	OUT1 to OUT384
				(Note 5)	–30	—	30		
Output amplitude voltage deviation		ΔVp-p	—	(Note 6)	–10	—	10	mV	OUT1 to OUT384
				(Note 7)	–20	—	20	mV	
				(Note 8)	–30	—	30	mV	
Gamma resistance fluctuation		$R\gamma$	—	—	7.7	12.8	18	kΩ	V0 to V4 V5 to V9
Leakage current		I_{IN}	—	—	–1	—	1	μA	Logic input
Standby current		ID_{STB}	—	—	—	—	1	μA	DV_{DD}
Current dissipation		DI_{DD}	—	(Note 9)	—	—	5	mA	DV_{DD}
		AI_{DD1}			—	—	6		AV_{DD}
		AI_{DD2}			—	—	4		
		AI_{DD3}		(Note 10)	—	—	16		
		AI_{DD4}			—	—	16		
Output current		I_{chg}	—	Vout = 8.9 V, AV_{DD} = 9 V Vx = 4 V (Note 11)	—	—	–20	μA	OUT1 to OUT384
		I_{dis}	—	Vout = 0.1 V, AV_{DD} = 9 V Vx = 1 V (Note 11)	30	—	—		

Note4: AV_{DD} = 9V, AV_{SS} = 0 V, AV_{SS} + 1.5 V ≤ VOUT ≤ AV_{DD} – 1.5 V
ΔVO is the numerical different the anticipated value of LCD panel drive output voltage (refer for (7) relationship between grayscale data and output voltage) from each LCD panel drive output voltage, These relationship shows as following formula.
ΔVO = [each LCD panel drive pin output voltage] – [anticipated value of LCD panel drive output voltage]

Note 5: AV_{DD} = 9 V, AV_{SS} = 0 V, AV_{SS} + 0.1 V ≤ VOUT < AV_{SS} + 1.5 V、AV_{DD} – 1.5 V < VOUT ≤ AV_{DD} – 0.1 V
The formula for ΔVO is same as Note 4.

Note 6: AV_{DD} = 9 V, AV_{SS} = 0 V, AV_{SS} + 1.5 V < VOUT < AV_{DD} – 1.5 V
ΔVpp is the numerical different the remainder of the average of all LCD panel drive output voltage at positive electrode and negative electrode from each LCD panel drive output voltage
ΔVpp = {[the remainder of each LCD panel drive output voltage at positive electrode (V0 to V4) and negative electrode (V5 to V9)]– [all LCD panel drive output voltage at positive electrode (V0 to V4) and negative electrode (V5 to V9) of LCD panel drive output voltage]} in the same grayscale

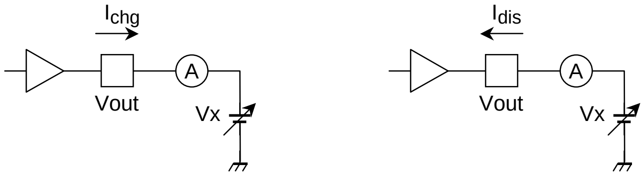
Note 7: AV_{DD} = 9 V, AV_{SS} = 0 V, AV_{SS} + 0.8 V < VOUT ≤ AV_{SS} + 1.5 V, AV_{DD} – 1.5 V ≤ VOUT < AV_{DD} – 0.8 V
The formula for ΔVpp is same as Note 6.

Note 8: AV_{DD} = 9 V, AV_{SS} = 0 V, AV_{SS} + 0.1 V ≤ VOUT ≤ AV_{SS} + 0.8 V, AV_{DD} – 0.8 V ≤ VOUT ≤ AV_{DD} – 0.1 V
The formula for ΔVpp is same as Note 6.

Note 9: LOAD cycle = 20 μs, f_{CPH} = 32.5 MHz
DI_{DD}: dot-checkered input pattern, no loaded
$AI_{DD}1$: V0 to V4 = V5 to V9 = 4.5 V, AV_{DD} = 9 V, LCD panel drive load = 200 Ω + 80 pF, $\overline{TESTP}$ = "H"
$AI_{DD}2$: V0 to V4 = V5 to V9 = 4.5 V, AV_{DD} = 9 V, LCD panel drive load = 200 Ω + 80 pF, $\overline{TESTP}$ = "L"

Note 10: LOAD cycle = 20 μs, f_{CPH} = 32.5 MHz
$AI_{DD}3$: V0 = 8.9 V, V4 = V5, V9 = 0.1 V, AV_{DD} = 9 V, LCD panel drive load = 200 Ω + 80 pF, $\overline{TESTP}$ = "H"
$AI_{DD}4$: V0 = 8.9 V, V4 = V5, V9 = 0.1 V, AV_{DD} = 9 V, LCD panel drive load = 200 Ω + 80 pF, $\overline{TESTP}$ = "L"

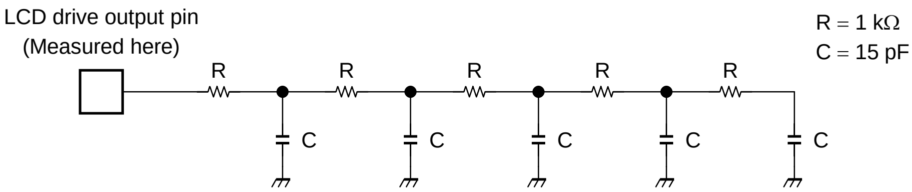
Note 11: Voltage applied to LCD panel drive

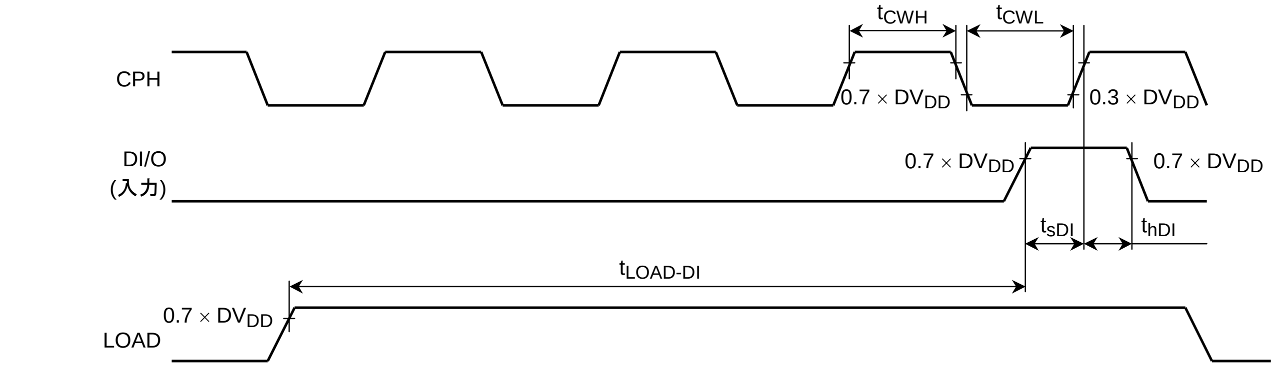


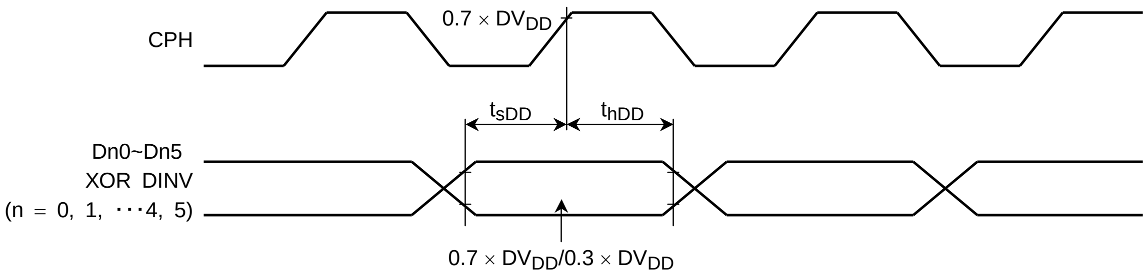
AC Characteristics
(DV_{DD} = 3.0 to 3.6 V, AV_{DD} = 7.5 to 10.0 V, DV_{SS} = AV_{SS} = 0 V, Ta = –20 to 75°C)

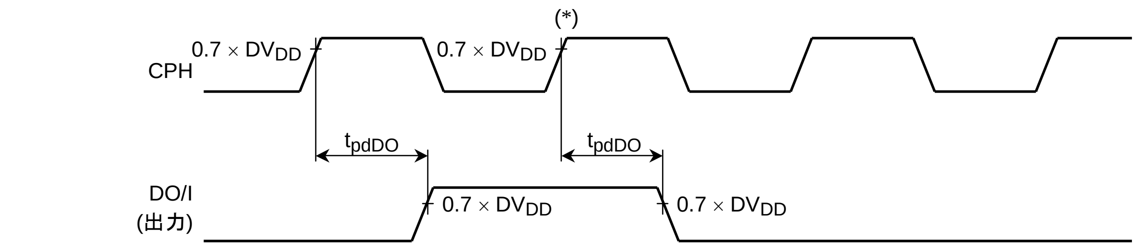
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
CPH pulse width H	t_{CWH}	—	—	4	—	—	ns
CPH pulse width L	t_{CWL}	—	—	4	—	—	ns
Enable setup time	t_{sDI}	—	—	4	—	—	ns
Enable hold time	t_{hDI}	—	—	0	—	—	ns
Data DINV setup time	t_{sDD}	—	—	4	—	—	ns
Data DINV hold time	t_{hDD}	—	—	0	—	—	ns
LOAD high period	t_{LWH}	—	—	3	—	—	CPH cycle
LOAD enable input period	$t_{LOAD\text{-}D1}$	—	—	2	—	—	CPH cycle
LOAD enable output period	$t_{LD\text{-}LOAD}$	—	—	1	—	—	CPH cycle
LOAD setup time	t_{sLD}	—	—	6	—	—	ns
POL setup time	t_{sDP}	—	—	4	—	—	ns
POL hold time	t_{hDP}	—	—	6	—	—	ns
Enable output delay time	t_{pdDO}	—	C_L = 15 pF	—	—	15	ns
Output delay time 1	t_{pdDE}	—	C_L = 75 pF R = 5 kΩ Target output voltage × 0.9 (Note 12)	—	—	6	μs
Output delay time 2	t_{pdDX}	—	C_L = 75 pF R = 5 kΩ Target output voltage ± ΔV_O (Note 12)	—	—	11	μs

Note 12: Output load condition

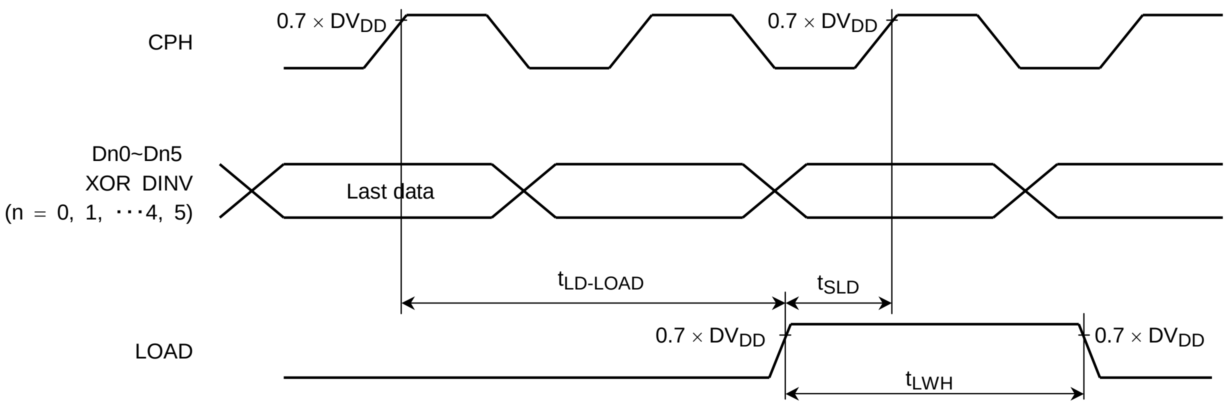


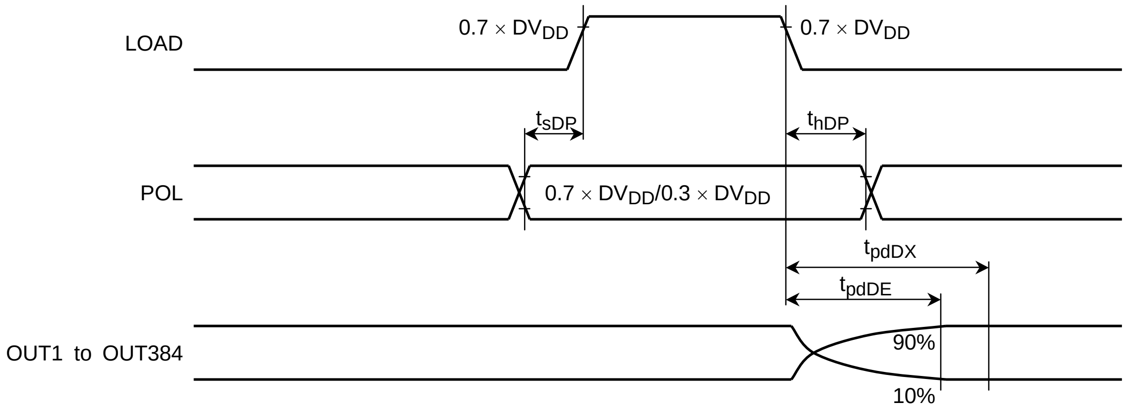






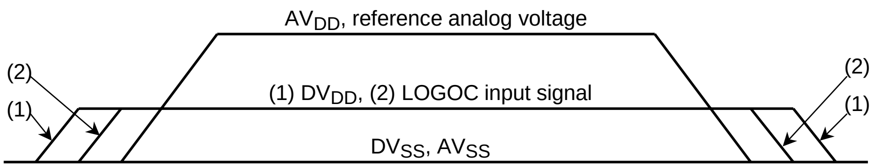
Note: Timing for loading OUT379 to OUT384
Timing for loading OUT1 to OUT6





Power-On Sequence

At power ON, the sequence is: DV_{DD} → LOGOC input signal → AV_{DD}, reference analog voltage
At power OFF, the sequence is the reverse of that for power ON.
Turn ON/OFF power supplies for AV_{DD} and reference analog voltage inputs simultaneously.
As long as the voltage condition, $AV_{DD} > DV_{DD}$, is satisfied, all power supplies can be turned OFF simultaneously.



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