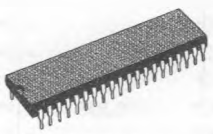
SGS-THOMSON MICROELECTRONICS

ST6306/07/08
ST6316/17/18

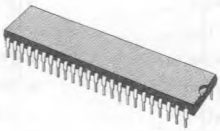
8-BIT HCMOS MCUs FOR TV FREQUENCY SYNTHESIS

ADVANCE DATA

- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4MHZ OR 8MHZ CLOCK OPTIONS
- PROGRAM ROM : 8192 BYTES
- DATA ROM : USER SELECTABLE SIZE
- DATA RAM : 256 BYTES
- DATA EEPROM : 128 BYTES
- 40/42 SHRINK/48 DIP PACKAGES
- 14/15 BIT PHASE LOCKED LOOP PERIPHERAL (PLL, ST6316/17/18 ONLY, ST6306/07/08 HAVE MORE I/Os)
- 20/22/24 (ST6306/07/08) SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 8 DIRECT LED DRIVING OUTPUTS
- 18/20/24 (ST6316/17/18) SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 8 DIRECT LED DRIVING OUTPUTS
- TWO TIMERS EACH INCLUDING AN 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER
- DIGITAL WATCHDOG FUNCTION
- SERIAL PERIPHERAL INTERFACE (SPI) SUPPORTING S-BUS/ I^2CBUS AND STANDARD SERIAL PROTOCOLS
- FOUR 6-BIT PWM D/A CONVERTERS
- AFC A/D CONVERTER WITH 0.5V RESOLUTION
- INFRARED SIGNAL PRE-PROCESSOR
- THREE INTERRUPT VECTORS (IR, Timer 1 & 2)



PDIP-40



PDIP-48

- ON-CHIP CLOCK OSCILLATOR
- ON-BOARD POWER-ON RESET CIRCUITRY
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- 1.625µS TCYCLE (with 8.0 MHz clock)
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- TRUE LIFO 6-LEVEL STACK
- ALL ROM TYPES ARE SUPPORTED BY PIN-TO-PIN PIGGYBACK VERSIONS.
- THE DEVELOPMENT TOOL OF THE ST63XX MICROCONTROLLERS CONSISTS OF THE EMST63 -HW/TVS EMULATION AND DEVELOPMENT SYSTEM AND CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS PC.

Figure 1 : ST6306/07/08 Pin Configurations

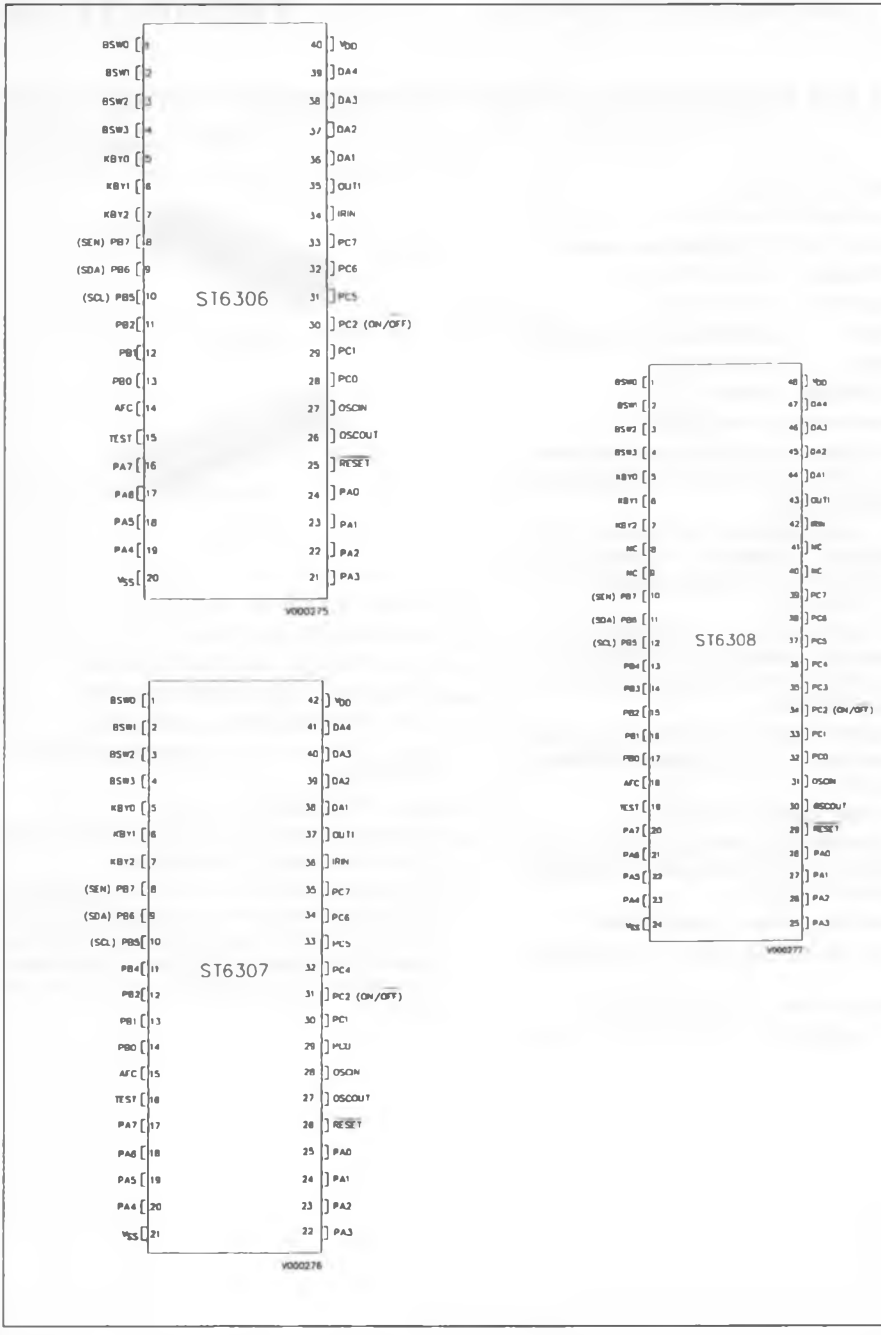
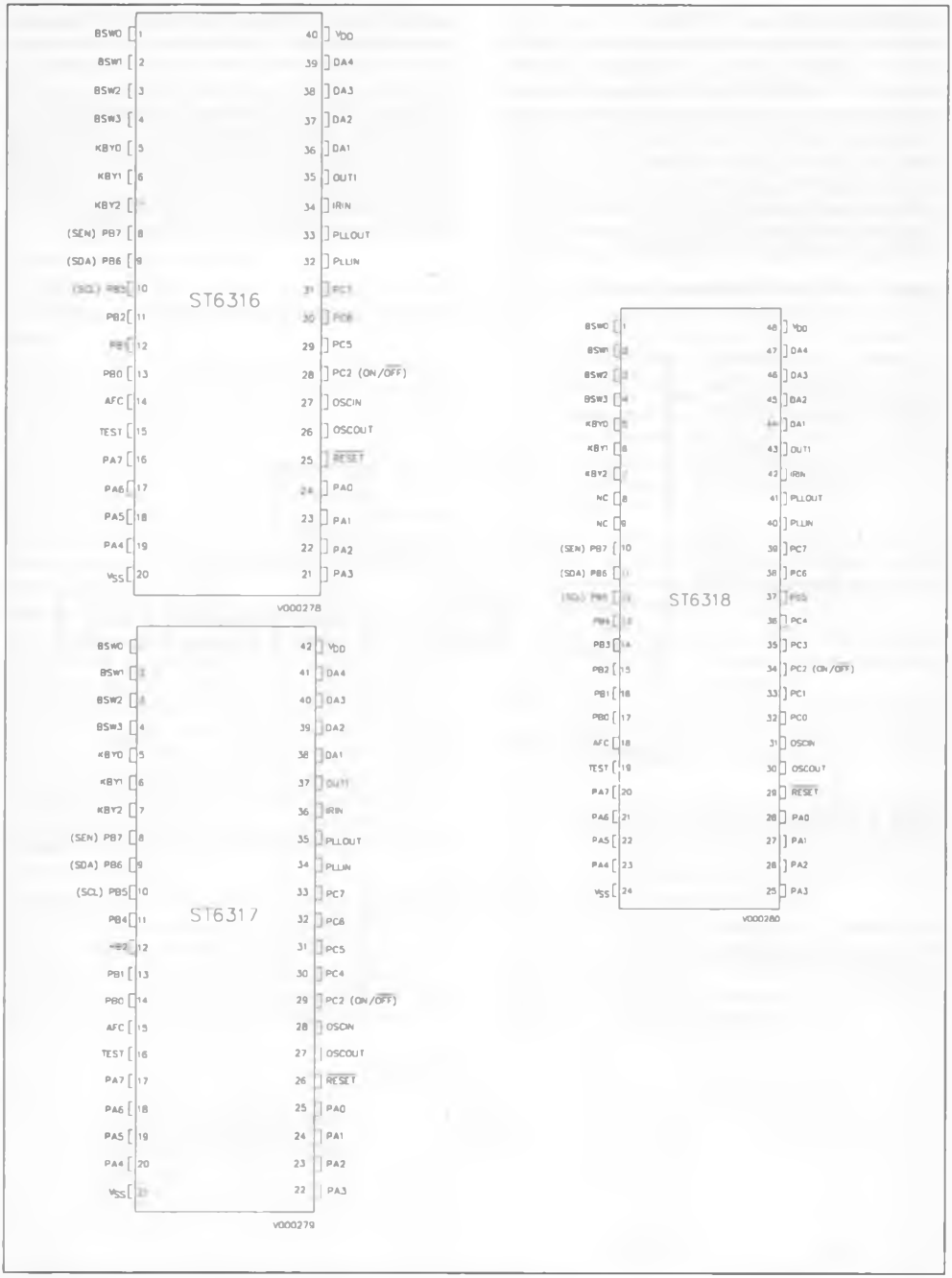


Figure 2 : ST6316/17/18 Pin Configurations



GENERAL DESCRIPTION

The ST6306/07/08 and ST6316/17/18 microcontrollers are powerful members of the 8-bit HCMOS ST63XX family, a series of devices specially oriented to TV applications. Different packages and configurations are available to offer different performance/cost tradeoffs. All ST63XX members are based on a building block approach: to a common Core is associated a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility, short design and testing time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST6306/07/08 are: two 8-bit counter with a 7-bit programmable prescaler (Timer), a Digital Watchdog Timer, a Serial Peripheral Interface (SPI), a 6-Bit PWM D/A Converter, an AFC A/D converter with 0.5V resolution. The ST6316/17/18 have the same configuration plus an on-chip 14/15 bit Phase Locked Loop peripheral (PLL) . In addition all these devices have 128 bytes of on-chip EEPROM.

Figure 3 : ST6306/07/08 System Description.

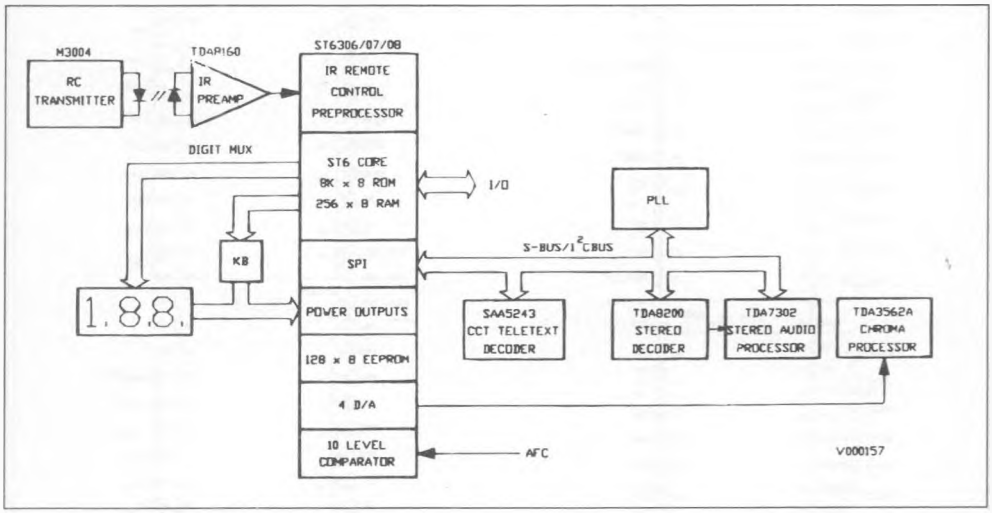
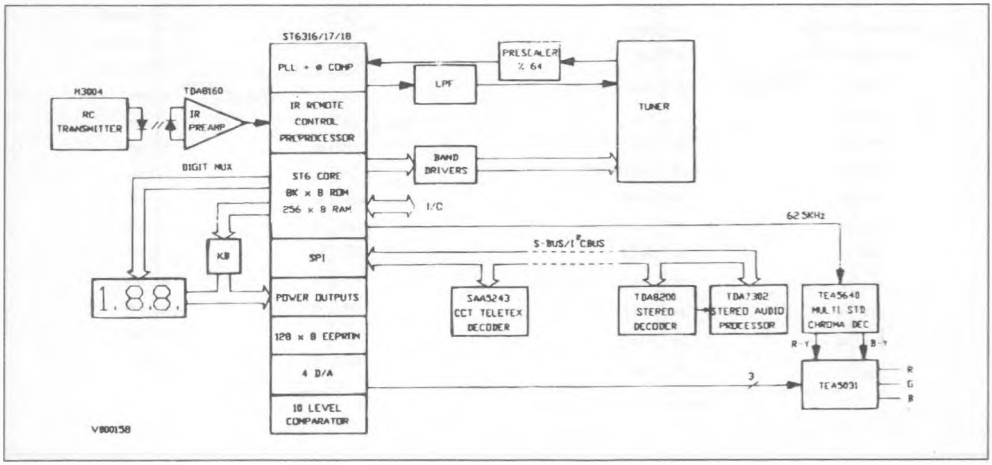


Figure 4 : ST6316/17/18 System Description.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN and OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A crystal quartz, a ceramic resonator or an external signal has to be connected between these two pins in order to allow the right operating of the MCU. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. A mask option allows the selection of a 4MHz or 8MHz oscillator frequency.

$\overline{\text{RESET}}$. The active low RESET pin is used to restart the microcontroller from the beginning of its program.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode if kept high when Reset is active. This pin has to be connected to VSS for normal operation.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has an open-drain (13.2V Max) output configuration with direct LED driving capability (30mA, 1V).

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor or output. In output mode the push-pull or open-drain configuration is available as ROM mask option. PB5, PB6 and PB7 lines when in output modes are "ANDed" with the SPI control signals. PB5 is connected with the SPI clock signal (SCK), PB6 with the SPI data signal (SDA) while PB7 is connected with SPI enable signal (SEN). PB3 is not available on ST6307/17. PB3 and PB4 are not available on ST6306/16.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor or output. In output mode the push-pull or open-drain configuration is available as ROM mask option. PC2 (12V Max) is also used as TV set On-Off switch. PC0 and PC1 are not available on ST6316/17 as these pins are connected to the PLL cell. PC3 is not available on ST 6307/17. PC3 and PC4 are not available on ST6306/16.

IRIN. This pin is the external interrupt input of the MCU and is directly connected to the infra-red signal pre-processor which allows, through a band pass filter, to reduce the number of interrupts sent to the Core. A mask option allows the direct connection of the interrupt pin to the Core Non maskable interrupt line.

DA1-DA4. These pins are the four PWM D/A outputs (32KHz repetition) of the 6-bit on-chip D/A converter. The PWM function can be disabled by software ; in this case these lines can be used as general purpose open-drain outputs (13.2V Drive).

OUT1. This pin is the 62.5KHz output available to drive multi-standard chroma processors. This function can be disabled by software allowing the use of this pin as general purpose open-drain output (13.2V drive).

AFC. This is the input of the on-chip 10 level A/D that can be used for AFC function. This pin is an high impedance input that can withstand signal with an amplitude up to 13.2V.

BSW0-BSW3. These outputs are provided to select up to 4 tuning bands. These pins have an open-drain (13.2V drive) output configuration.

KBY0-KBY2. These input pins are intended as common lines for keyboard scanning. They have CMOS level threshold and have on-chip 100Kohm pull-up resistor.

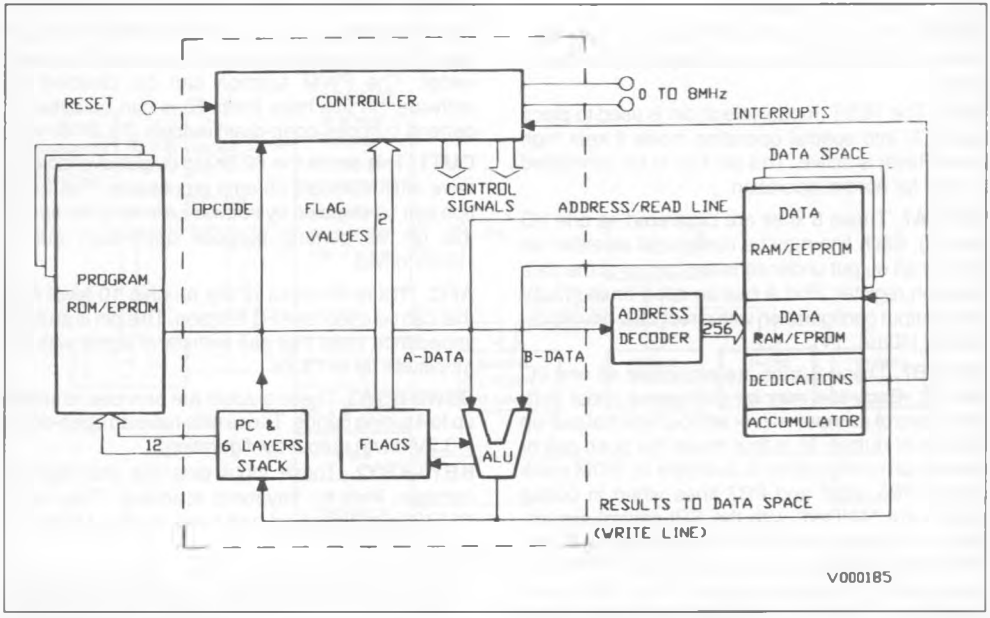
PLLIN. This is the PLL input pin. The signal coming from an external 64 divider is fed to PLLIN. Maximum input frequency is 16MHz and minimum required signal amplitude is 500mVpp. The PLL is not available in the ST6306/07/08 types.

PLLOUT. This is the PLL output pin. This three-state output generates tuning correction pulses at the comparison frequency of 976.5Hz (488.2 and 1.95KHz optionally selectable). The PLL is not available in the ST6306/07/08 types.

ST63XX CORE

The ultra small and fast Micro-Core of the ST63XX TV chips microcontrollers is designed to provide the economy of small die size through advanced HCMOS technologies. The ST63XX Core can directly address 4 Kbyte of program memory with extension capability by 2 Kbyte bank addition. The directly addressable data space is 256 bytes sized with extension capability by 64 byte bank addition. The data ROM which is addressed in the data space is physically located in the program area. The core includes an 8-bit accumulator, two 8-bit index registers and a 12-bit program counter. Three pairs of flags monitor the processor operations while a six levels LIFO hardware stack is available for subroutine & interrupt return address storage. One NMI and four normal interrupt vectors are available. STOP and WAIT modes are included to reduce overall power consumption.

Figure 5 : ST63XX Core Block Diagram.



PROGRAM ROM PAGING

ST63XX has 12 address bits for program ROM, thus giving a program address space of 4 Kbytes. In the highest twelve bytes of the ROM are located the restart and INT vectors. To go beyond the 4K limit, the lower half of the program address space (0..7FFH) has been used as paged address space, the current page being selected by a banking register. Only the lower part of address space has been bank-switched because of interrupt (vectors and drivers) and common subroutines, that should be available all the time.

DATA ROM WINDOWING

Data ROM is physically the same ROM as for program space. Simply, it is possible to read as data all the program ROM space with the range 40H..7FH of the data address space and the contents of the Data ROM Window Register. The six least significant bits of data address space become the least significant address bits of the program ROM address to be build. This only when addressing the data space locations mentioned above. The bits coming out from Data ROM Window register become the most significant ones ; they are 6 if the program ROM is of 4Kbytes, 7 if 8Kbytes. So, when addressing location 40H of data space, and 0 is loaded in the register, the physical location addressed is at location 0.

PAGED RAM ADDRESS RANGE

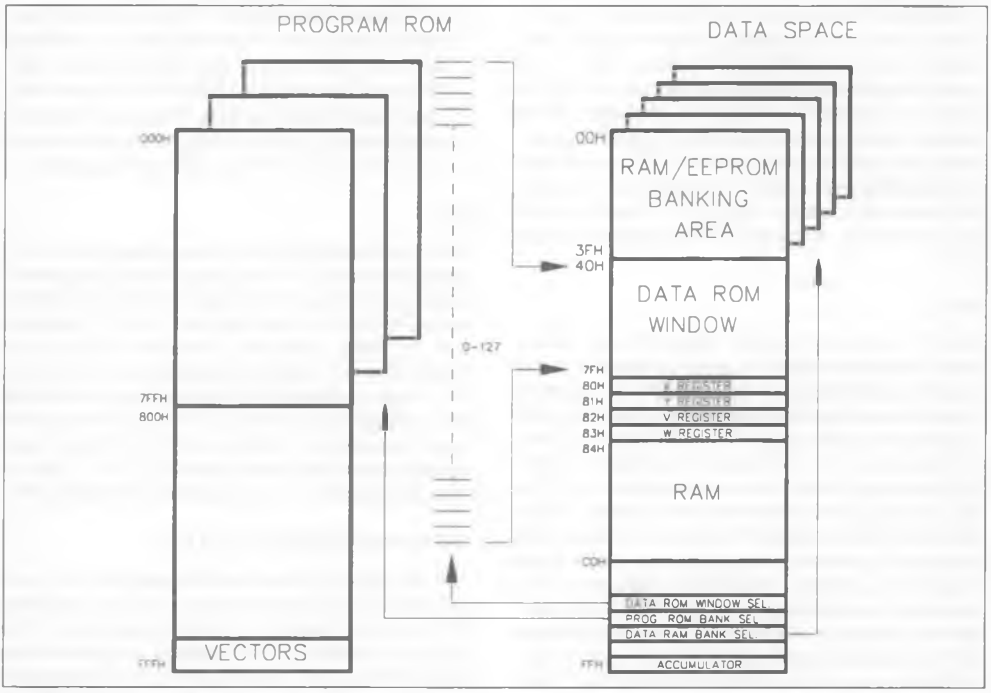
A 64 bytes range inside the data space is paged to allow extension of the RAM memory available for the user. Paged RAM address range can be switched to address up to 8 different 64 bytes pages, in which any kind of memory and/or additional control registers can be mapped. On ST6306/07/08 and ST6316/17/18 three pages are available. These 192 bytes plus 64 Bytes of non-paged RAM give a total of 256 RAM bytes available for the user.

EEPROM

128 bytes of EEPROM are available to store normalized TV audio and video user/factory values as well as 40 favorite programs. The EEPROM is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. Any EEPROM location can be read just like any other data location, also in terms of access time.

A writing of an EEPROM location takes about 5msec and during this time the EEPROM is not accessible by the Core. Two programming modes are available : BYTE MODE (BMODE) and PARALLEL MODE (PMODE). The BMODE is the normal way to write the EEPROM and consists in accessing one byte per time. The PMODE consists in accessing up to 8 bytes per time.

Figure 6 : ST63XX Memory Addressing Description.



I/O PORTS

Each ST63XX general I/O port normally consists of eight identical cells, each containing a separately addressable data latch and data direction latch ; together they form an eight bit data register and an eight bit data direction register. The I/O uses two addresses of the data space, one for the data register and one for the data direction register. Each of the eight pins can be programmed independently as an input or as an output with various additional modes under control of the data direction register. When programmed as an input a pull-up resistor can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode ; this is defined during manufacture by a program ROM mask option. One I/O port (A) has an open-drain (13.2V drive) output configuration with high current drive capability for direct LED driving.

TIMERS

Each Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes : event counter, input gated and output modes. The content of the 8-bit counter can be read/written in the Timer/Counter register. The state of the 7-bit prescaler can be read in the prescaler register. A maskable interrupt is associated with the end-of-count.

DIGITAL WATCHDOG

The digital watchdog consists of a down counter that can be used to provide a controlled recovery from a software upset. The check time can be set differently for different routines within the general program. After a reset the watchdog is automatically activated. Once the watchdog is enabled it can not be cleared by software without generating a Reset. The reset is prevented if the register is reloaded with the desired value before the watchdog register time-out. When the watchdog is active the STOP instruction is deactivated and a WAIT instruction is automatically executed instead of the STOP. Deactivation of the watchdog is available as manufacturing mask option.

SPI

The SPI macrocell has been designed to be cost effective and very flexible in order to interface to the external peripherals generally present in TV applications that are often characterized by different serial input/output specifications (Audio Processors, Teletext Decoders, etc.). The reason of an hardware serial interface is that with the increasing features of the TV, in particular the newer teletext features and the greater diffusion of digital TV devices, it is necessary to be able to interface at speeds faster than those practical by software. The ST6 TV devices are designed with a serial peripheral interface which maintains the software SPI flexibility but adds hardware SPI configurations suitable for devices which typically require a greater exchange of data in the TV application. The three pins dedicated for serial data transfer (single master only) can be operated in the following ways : directly by software, as an S-BUS, as an I^2CBUS (two pins), and as an standard SPI (shift register). When using the hardware SPI, a fixed clock rate of 62.5kHz is provided which is considered a good value for TV applications.

6-BIT PWM D/A CONVERTER AND 62.5 OUTPUT

The D/A macrocell offers four PWM D/A outputs (31.2Khz repetition) with six bit resolution and with possibilities to disable the PWM in order to use the pins as standard open drain outputs. In addition a 62.5KHz output pin is available. Also this function which can be disabled and the line can be used as a standard open drain output.

AFC, KB, BAND SWITCH

This macrocell contains many dedicated functions for TV applications :

- An A/D converter with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5V to effectively double the resolution.
- A keyboard input register of three bits which provides three inputs lines dedicated to keyboard scanning. These lines are CMOS levels compatible with an on-chip 100Kohm pull-up resistor.
- Band switch select outputs. These pins are provided to select up to 4 tuning bands and have an open-drain (13.2V drive) output configuration.

PLL

This macrocell contains a phase-locked loop (PLL) synthesizer with a 14 bit (option 15-bit) programmable divider. The dividing ratio is given by the value loaded in the PLL data registers. The PLL operates with a tuning resolution frequency of 976.5Hz (488.2Hz and 1.95KHz available as options). The PLL input is capacitively coupled with the signal coming from an external 64 divider. The maximum input frequency is 16MHz and the minimum input voltage amplitude (peak to peak) is 0.5V. This on-chip peripherals is not available on ST6306/07/08.

INFRARED DIGITAL FILTER

The IR signal pre-processor is designed to be used with M3004 or M708 transmitters and with any other IR transmitter having a carrier frequency in the range 35.8-40KHz. (For details of the transmitters please refer to their specifications). The unique feature of this pre-processor is its band pass filter. It can distinguish the signal in the presence of extreme noise conditions and thus ensures a minimum number of interrupt the ST63XX core, leaving the latter to concentrate on other tasks. This celle can be bypassed by ROM mask option. In this case the INT pin is connected directly to the NMI of ST63 Core.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST63XX TV family is supported by a complete set of emulation devices. This set includes the ST63PXX piggyback devices for pin-to-pin replacement of all DIP masked devices.

The EMST63-HW/TVS hardware emulator and development system is also available offering powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to shorten the total system development time of the final application. The ST63XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS™ personal computers.