SM566

Spread Spectrum Clock Generator

FEATURES

- 25 to 200 MHz Operating Frequency Range
- Wide (9) Range of Spread Selection
- Accepts Clock and Crystal Inputs
- Provides 4 clocks
  (SSCLK1A, SSCLK1b, SSCLK2, REFOUT)
- Low Power Dissipation
  3.3V = 85 mw. (Typical @ 40 MHz, No Load.)
- Center Spread Modulation
- Low Cycle-to Cycle Jitter
- Available in 16-pin (150 mil.) SOIC package

APPLICATIONS

- SVGA and XVGA Controllers
- LCD Panels and Monitors
- Printers and MFPs

BENEFITS

- Peak EMI reduction by 8 to 16dB
- Fast Time to Market
- Cost Reduction

GENERAL DESCRIPTION

The CYPRESS SM566 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital electronic systems.

The SM566 uses a Cypress proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and frequency modulate the input frequency of the digital clock. By frequency modulating the clock, (SSCLK1a/b and SSCLK2), the measured EMI at the fundamental and harmonic frequencies is greatly reduced. The modulated output frequency is centered on the input frequency.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time to market without degrading system performance.

The SM566 provides 4 output clocks, SSCLK1a, SSCLK1b, SSCLK2 and REFOUT. SSCLK1a/b and SSCLK2 are modulated clocks and REFOUT is a buffered copy of the reference clock or oscillator. The SM566 frequency and spread % ranges are selected by programming S0, S1, S2 and S3 digital inputs. S0 and S1 use three (3) logic states including High (H), Low (L) and Middle (M) logic levels to select one of 9 available Frequency and Spread % ranges. Refer to page 6 for details on programming Tri-Level inputs S0 and S1. Programming details for S2 and S3 can be found on pages 6 and 8.

The SM566 will operate over a wide range of frequencies from 25 to 200 MHz. Operation to 200 MHz is possible with the use of Dual Drivers at pins 8 and 9. With a wide range of selectable bandwidths, the SM566 is a very flexible Low EMI clock. Modulation can be disabled to provide a 4 output conventional clock.

REFOUT can be used as a baseline comparison when making dB reduction measurements of the modulated clock outputs, SSCLK1a and/or SSCLK1b.

The SM566 is available in a 16 pin SOIC (150-mil.) package with a commercial operating temperature range of 0 to 70°C.

BLOCK DIAGRAM

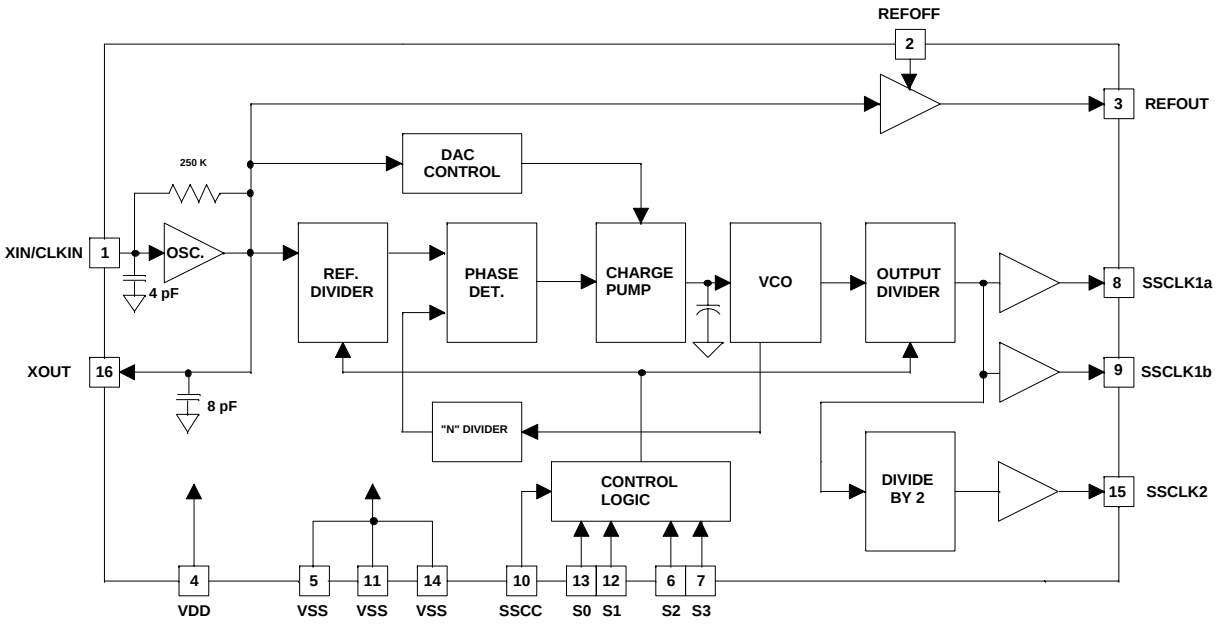


Figure 1. Block Diagram

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
SM566BZ	16 Pin SOIC	0 to 70°C

Table 1. Ordering Information

PIN CONFIGURATION

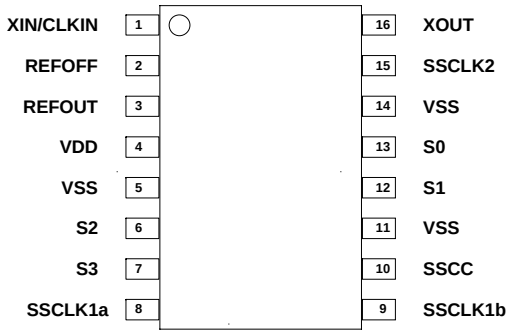


Figure 2. 16 Pin SOIC Pin Assignment

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	Xin/CLKIN	I	Clock or Crystal connection input. Refer to the Table-5, 6 or 7 (page 8) for input frequency range selection.
2	REFOFF	I	Input pin enables REFOUT clock at pin 3. REFOFF has 400K Ω internal pull-up resistor. Logic “0” enables REFOUT, logic “1” disables REFOUT. Default = Disabled.
3	REFOUT	O	Buffered, non-modulated output clock derived from XIN/CLKIN input frequency. There is a 180 ° phase shift from XIN to REFOUT.
4	VDD	P	Positive power supply. Bypass to ground with 0.1-uF capacitor.
5, 11, 14	VSS	G	Power supply ground.
6	S2	I	VCO Range control. Refer to page 8 for detailed programming information. Has 400K Ω internal pull-up to VDD.
7	S3	I	VCO Range control. Refer to page 8 for detailed programming information. Has 400K Ω internal pull-up to VDD.
8	SSCLK1a	O	Modulated clock output. Pins 8 and 9 are identical but separate drivers.
9	SSCLK1b	O	Modulated clock output. Pins 8 and 9 are identical but separate drivers.
10	SSCC	I	Spread Spectrum Clock Control (Enable/Disable) function. SSCG function is enabled when input is high and disabled when input is low. Internal 400K Ω pull-up defaults to modulation ON.
12	S1	I	Tri-Level Logic input control pin used to select Frequency and Bandwidth. Refer to Page 8 for Frequency/Bandwidth selection. Tri-Level Logic programming details can be found on page 6.
13	S0	I	Tri-Level Logic input control pin used to select Frequency and Bandwidth. Refer to Page 8 for Frequency/Bandwidth selection. Tri-Level Logic programming details can be found on page 6.
15	SSCLK2	O	Modulated output clock. Frequency of SSCLK2 = SSCLK1a/2. BW % of SSCLK2 is equal to BW % of SSCLK1a/b.
16	XOUT	O	Oscillator output pin connected to crystal. Leave this pin unconnected If an external clock drives Xin/CLK.

Table 2. Pin Description

ABSOLUTE MAXIMUM RATINGS[1]:

Supply Voltage (AVDD or DVDD): +6V
AVDD - DVDD: +/-300mV
AGND - DGND: +/-300mV

Operating Temperature: 0 to 70°C
Storage Temperature: -65 to +150°C
Junction Temperature (10-sec. soldering): +300°C

DC ELECTRICAL CHARACTERISTICS:

Test Conditions: VDD=3.3V, T=25°, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Power Supply Range	2.97	3.3	3.63	V	+/- 10 %
VINH	Input High Voltage	0.85VDD	VDD	VDD	V	S0 and S1 only.
VINM	Input Middle Voltage	0.40VDD	0.50VDD	0.60VDD	V	S0 and S1 only.
VINL	Input Low Voltage	0.0	0.0	0.15VDD	V	S0 and S1 only.
VOH1	Output High Voltage	2.4	-	-	V	IOH = 6 ma, SSCLKa
VOH2	Output High Voltage	2.0	-	-	V	IOH = 20 ma, SSCLKb
VOL1	Output Low Voltage	-	-	0.4	V	IOH = 6 ma, SSCLKa
VOL2	Output Low Voltage	-	-	1.2	V	IOH = 20 ma, SSCLKb
Cin1	Input Capacitance	3	4	5	pF	Xin/CLK (Pin 1)
Cin2	Input Capacitance	6	8	10	pF	Xout (Pin 16)
Cin2	Input Capacitance	3	4	5	pF	All input pins except 1.
IDD1	Power Supply Current	-	27	32	ma	FIN = 40 MHz, 15pf @ all outputs.
IDD1	Power Supply Current	-	23	28	ma	FIN = 40 MHz, No Load
IDD2	Power Supply Current	-	50	58	ma	FIN = 165 MHz,15pf @ all outputs.
IDD2	Power Supply Current	-	39	46	ma	FIN = 165 MHz, No Load

Table 3.

TIMING ELECTRICAL CHARACTERISTICS:

Test Conditions: VDD=3.3V, T=25°C, CL=15pF. Rise/Fall time @ 0.4 and 2.4V, duty cycle at 1.5 V. Mod. ON.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
ICLKFR	Input Frequency Range	27		200	MHz	Non crystal, 3.0 volts Pk-Pk. Ext. source.
trise(a)	Clock Rise Time	1.2	1.4	1.6	ns	SSCLK1a or SSCLK1b, Freq. = 100 MHz
tfall(a)	Clock Fall Time	1.2	1.4	1.6	ns	SSCLK1a or SSCLK1b, Freq. = 100 MHz
trise(a+b)	Clock Rise Time	1.3	1.5	1.7	ns	SSCLK1 (a+b), CL = 33 pF, 100 MHz
tfall(a+b)	Clock Fall Time	1.3	1.5	1.7	ns	SSCLK1 (a+b), CL = 33 pF, 100 MHz
trise(a+b)	Clock Rise Time	1.4	1.6	1.8	ns	SSCLK1 (a+b), CL = 33 pF, 200 MHz
tfall(a+b)	Clock Fall Time	1.4	1.6	1.8	ns	SSCLK1 (a+b), CL = 33 pF, 200 MHz
trise(2)	Clock Rise Time	1.1	1.3	1.5	ns	SSCLK2, Pin 15, CL = 15 pF, 12.5 MHz
tfall(2)	Clock Fall Time	1.2	1.4	1.6	ns	SSCLK2, Pin 15, CL = 15 pF, 12.5 MHz
trise(REF)	Clock Rise Time	1.3	1.5	1.7	ns	REFOUT, Pin 3, CL = 15 pF, 65 MHz
tfall(REF)	Clock Fall Time	1.6	1.8	2.0	ns	REFOUT, Pin 3, CL = 15 pF, 65 MHz

[1] **Note: Single Power Supply:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

DTYin	Input Clock Duty Cycle	20	50	80	%	XIN/CLK (Pin 1)
DTYout	Output Clock Duty Cycle	45	50	55	%	SSCLK1a/SSCLKb (Pin 8 and 9)
CCJ	Cycle-to-Cycle Jitter	-	200	225	ps	F = 100 MHz, SSCLK1a/1b CL = 33 pF
CCJ	Cycle-to-Cycle Jitter	-	325	350	ps	F = 200 MHz, SSCLK1a/1b CL = 33 pF

Table 4.

Output Clock Architecture

The SM566 provides 4 separate output clocks, REFOUT, SSCLK1a, SSCLK1b and SSCLK2, for use in a wide variety of applications. Each clock output is described below in detail.

REFOUT

REFOUT is a 3.3-volt CMOS level non-modulated inverted copy of the clock at XIN/CLKIN. As an inverted clock, the output clock at REFOUT is 180 degrees out of phase with the input clock at XIN/CLK. Placing a high (1) logic state on REFOFF, pin 2, will disable the REFOUT clock. When REFOUT is disabled, REFOUT, pin 3, is at a high (1) logic state.

SSCLK1a/b

SSCLK1a and SSCLK1b are Spread Spectrum clock outputs used for the purpose of reducing EMI in digital systems. SSCLK1a and SSCLK1b can be connected in several different ways to provide flexibility in application designs. Each clock can drive separate nets with a capacitive load of up to 15 pF each or connected together to provide drive to a single net with a capacitive load as high as 33 pF. When both clocks are connected together, the SM566 is capable of driving 3.3 volt CMOS compatible clocks to frequencies as high as 200 MHz. If one clock output is not connected to a load, negligible EMI will be generated at the unused pin because there is no current being driven. The frequency and bandwidth of SSCLK1a and SSCLK1b is programmed by the logic states presented to S2 and S3. The frequency multiplication at SSCLK1a and SSCLK1b is either 1X or 2X, controlled by S2 and S3. The modulated output clock SSCLK1 is provided at pins 8 and 9 with each pin having separate but identical drivers. Refer to figure 3 below.

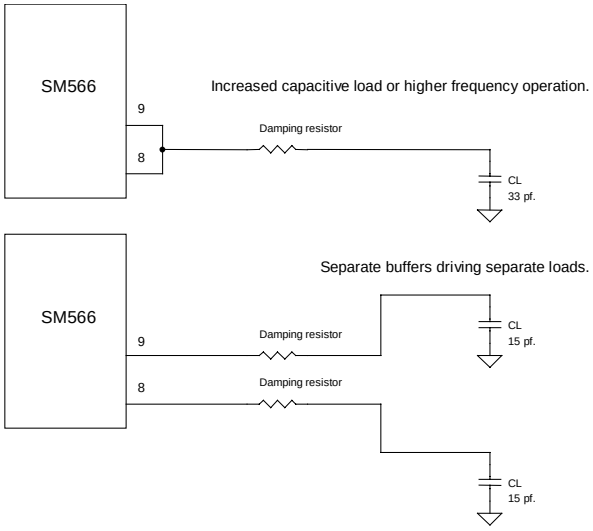


Figure 3. SSCLK1a/b Driver Configurations

SSCLK2
SSCLK2 is a Spread Spectrum Clock with a frequency ½ that of the SSCLK1a clock frequency. When SSCLK1a is programmed to provide a 2.5 % modulated clock at 1X times the reference clock, 40 MHz for example, the frequency of SSCLK2 will be 20 MHz with a BW of 2.5%. Note that by programming the frequency of SSCLK1a to 2X, the frequency of SSCLK2 will be 1X times the reference clock frequency.

Control Logic Structures
The SM566 has 6 input control pins for programming VCO range, BW %, Mod ON/OFF and REFOUT ON/OFF. These programmable control pins are described below.

REFOFF
The output clock REFOUT can be enabled or disabled by controlling the state of REFOFF. When REFOFF is at a logic low (0) state, REFOUT is enabled and the reference clock frequency is present at pin 3. When REFOFF is at a logic high state (1), REFOUT is disabled and is set to a logic high state on pin 3. REFOFF has a 400 K Ω internal pull-up resistor to VDD.

S0 and S1 (Tri-Level Inputs)
S0 and S1 are used to program the frequency range and bandwidth of the modulated output clocks SSCLK1a/b and SSCLK2. S0 and S1 of the SM566 are designed to sense 3 different analog levels. With this Tri-Level structure, the SM566 is able to detect 9 different logic states. Refer to tables 2, 3 and 4 for the results of each of these 9 states. The level of each state is defined as follows;

Logic State “0” is a voltage that is between 0 and 0.15 X VDD volts.
Logic State “M” is a voltage between 0.4 X VDD and 0.6 X VDD volts.
Logic State “1” is a voltage between 0.85 X VDD and VDD

The following diagram illustrates how to implement Tri-Level Logic.

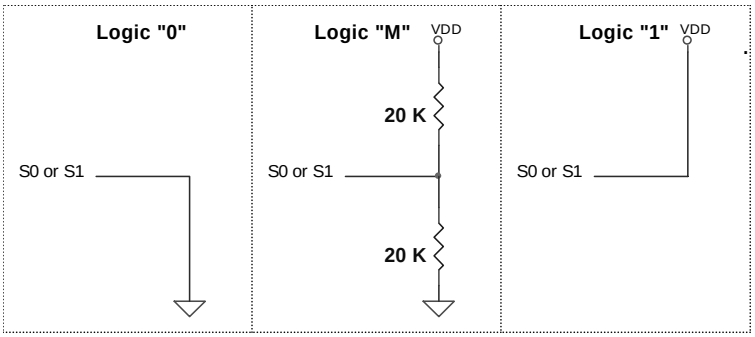


Figure 4.

S2 and S3
S2 and S3 are used to program the SM566 into different frequency ranges and multipliers. The SM566 operates over a frequency range of 25 to 200 MHz and a 1X or 2X multiplication of the reference frequency. S2 and S3 are binary logic inputs and each has a 400 K Ω pull-up resistor to VDD. Refer to tables 2, 3 and 4 for programming details.

SSCC
SSCC is an input control pin that enables or disables SSCG modulation of the output clock at SSCLK1a/b and SSCLK2. Disabling modulation is a method of comparing radiated EMI in a product with SSCG turned on or off.

The SM566 can be used as a conventional low jitter multiple output clock when SSCC is set to low (0). SSCC has a 400 K Ω internal pull-up resistor. Logic high (1) = Modulation ON, logic low (0) = Modulation OFF. Default is modulation to ON.

Modulation Rate

Spectrum Spread Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the Modulation Rate, Tmr. Modulation Rates of SSCG clocks are generally referred to in terms of frequency or Fmod = 1/Tmod.
The input clock frequency, Fin, and the internal divider count, Cdiv, determine the Modulation Rate. The SM566 utilizes 2 different modulation rate dividers, depending on the range selected on S2 and S3 digital control inputs. Refer to the example below;

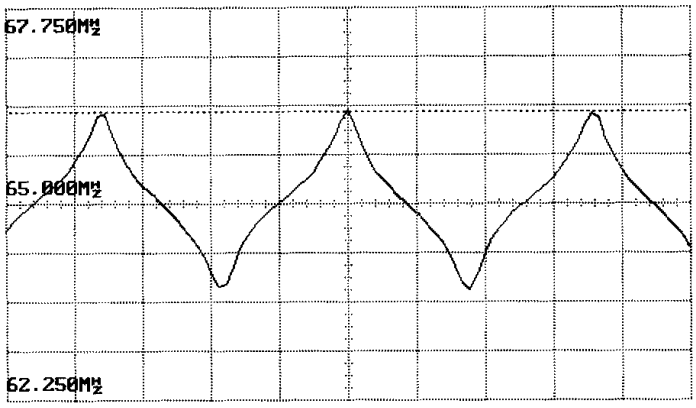
S3, S2	Cdiv	Output Frequency
0, 0	1166	1X
0, 1	1166	2X
1, 0	2332	1X
1,1	N/A	N/A

Example:

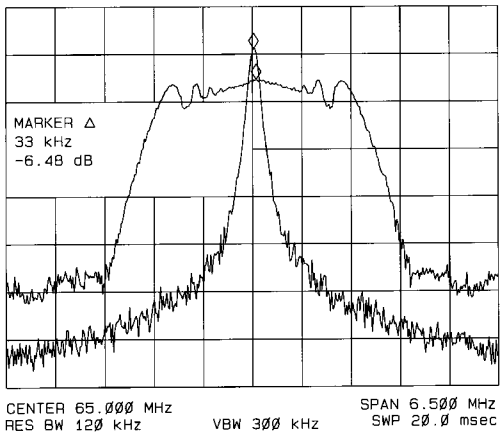
Device = SM566
Fin = 65 MHz
Range = S3 = 0, S2 = 1, S1 = 1, S0 = 0

Then;

Modulation Rate = Fmod = 65 MHz/1166 = 55.7 kHz.



Modulation Profile



Spectrum Analyzer

Figure 5. SSCG Clock, SM566, 65 MHz..

Operating Ranges

The SM566 has 3 frequency groups to select from. Each combination of frequency and bandwidth can be selected by programming the input control lines, S0 – S3, to the proper logic state.

Group 1 is the 1 X low frequency range and operates from 25 to 108 MHz.

Group 2 is the 1 X high frequency range and operates from 50 to 200 MHz.

Group 3 is the 2 X low frequency range and operates from 25 to 54 MHz input and 50 to 108 MHz output.

Group 1: Frequency and Bandwidth Selection Chart.

25 – 54 MHz (Low Range)

XIN/CLK (MHz)	S1=M S0=M	S1=M S0=0	S1=1 S0=0	S1=0 S0=0	S1=0 S0=M
25 – 35	3.8	3.2	2.8	2.3	1.9
35 – 40	3.5	3.0	2.5	2.1	1.7
40 – 45	3.2	2.8	2.4	1.9	1.6
45 – 50	3.0	2.6	2.2	1.8	1.5
50 – 54	2.8	2.4	2.0	1.7	1.4

50 – 108 MHz (High Range)

XIN/CLK (MHz)	S1=1 S0=M	S1=0 S0=1	S1=1 S0=1	S1=M S0=1
50 – 60	2.5	1.9	1.2	1.0
60 – 70	2.4	1.8	1.1	0.9
70 – 80	2.3	1.6	1.1	0.9
80 – 100	2.0	1.4	1.0	0.8
100 – 108	1.8	1.3	0.8	0.6

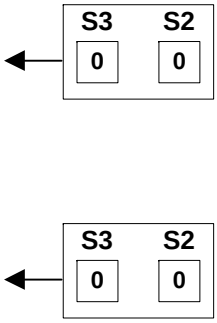


Table 5. Low Frequency (1X) Selection Chart

Group 2: Frequency and Bandwidth Selection Chart

50– 108 MHz (Low Range)

XIN/CLK (MHz)	S1=M S0=M	S1=M S0=0	S1=1 S0=0	S1=0 S0=0	S1=0 S0=M
50– 60	3.6	3.1	2.6	2.1	1.8
60 – 70	3.5	3.0	2.5	2.0	1.7
70 – 80	3.3	2.8	2.4	1.9	1.6
80 - 100	3.0	2.5	2.1	1.7	1.4
100 - 108	2.6	2.3	1.9	1.5	1.3

108 – 200 MHz (High Range)

XIN/CLK (MHz)	S1=1 S0=M	S1=0 S0=1	S1=1 S0=1	S1=M S0=1
108 – 120	2.3	1.7	1.1	0.9
120 – 130	2.3	1.7	1.1	0.9
130 – 140	2.3	1.7	1.1	0.9
140 – 150	2.2	1.6	1.1	0.9
150 - 160	2.1	1.5	1.0	0.8
160 - 170	2.0	1.5	0.9	0.8
170 - 180	1.9	1.4	0.9	0.7
180 – 190	1.8	1.3	0.8	0.7
190 - 200	1.7	1.2	0.7	0.6

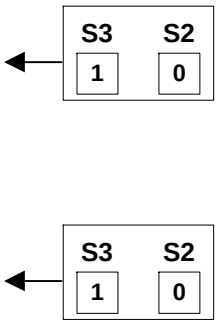


Table 6. High Frequency (1X) Selection Chart

Group 3 Frequency and Bandwidth Selection Chart.

25 – 54 MHz (Low Range, 2X)

XIN/CLK (MHz)	SSCLK1 (MHz)	S1=M S0=M	S1=M S0=0	S1=1 S0=0	S1=0 S0=0	S1=0 S0=M
25 – 35	**50 - 70**	3.8	3.2	2.8	2.3	1.9
35 – 40	**70 - 80**	3.5	3.0	2.5	2.1	1.7
40 – 45	**80 - 90**	3.2	2.8	2.4	1.9	1.6
45 – 50	**90 - 100**	3.0	2.6	2.2	1.8	1.5
50 – 54	**100 - 108**	2.8	2.4	2.0	1.7	1.4

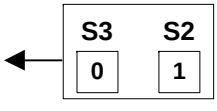


Table 7. Low Frequency (2X) Selection Chart

Application Schematic

In this example, the SM566 is using a 30 MHz 3rd overtone crystal as the reference clock.

S0 = 0 and S1 = 0, are programmed to select a BW of 2.3 %. (Refer to table 4)
S2 = 1 and S3 = 0, are programmed to select the Group 3 range, (2X). (Refer to table 4)

VDD = 3.30 VDC
SSCLK1a = 60 MHz @ 2.3 % center spread modulation.
SSCLK1b = 60 MHz @ 2.3 % center spread modulation.
SSCLK2 = 30 MHz @ 2.3 % center spread modulation.
REFOUT = 30 MHz non-modulated clock

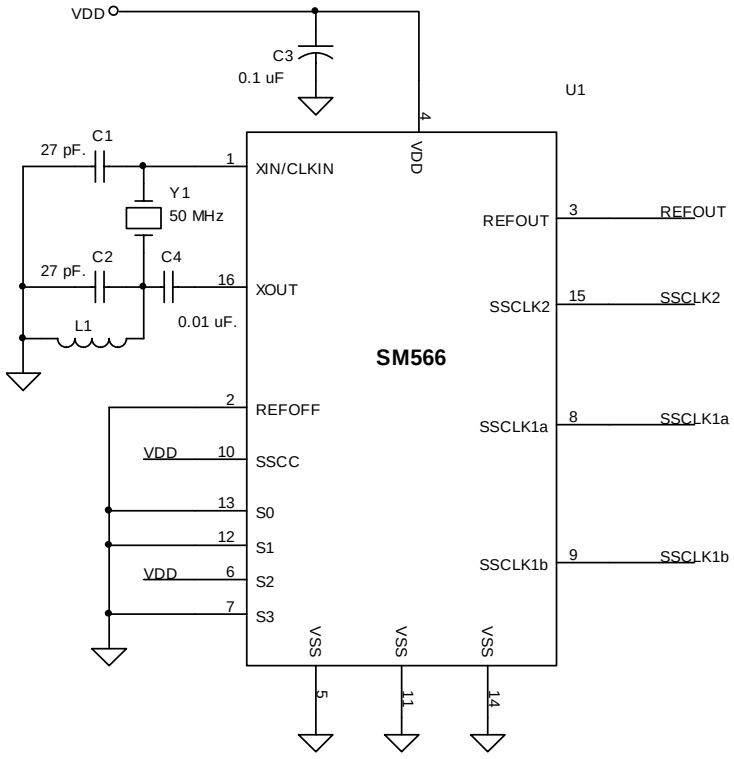


Figure 6. Application Schematic

Note:
L1 is chosen to resonate with C2 at a frequency 30% higher than the fundamental frequency of this crystal. This will insure that the crystal will start up at the 3rd harmonic instead of the fundamental frequency of the crystal. Refer to crystal manufacturer's specifications for recommended values of L1, if a crystal is used.
The above circuit assumes a crystal CL of 18 pF.

16 PIN SOIC PACKAGE DRAWING

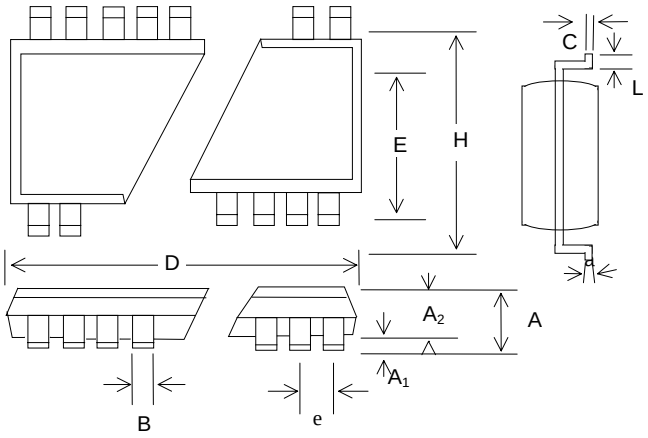


Figure 7. SOIC16 Drawing

16 Pin SOIC Outline Dimensions (150 mil)

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	-	0.069	1.35	-	1.75
A_1	0.004	-	0.010	0.10	-	0.25
A2	0.047	-	0.059	1.20	-	1.50
B	0.013	-	0.020	0.33	-	0.51
C	0.007	-	0.010	0.19	-	0.25
D	0.366	-	0.394	9.80	-	10.00
E	0.150	-	0.157	3.80	-	4.00
e	0.050 BSC			1.27 BSC		
H	0.228	-	0.244	5.80	-	6.20
L	0.016	-	0.050	0.40	-	1.27
a	0º	-	8º	0º	-	8º

Table 8. SOIC16 Outline

Notes:

NOTICE

Cypress Semiconductor Corporation reserves the right to make changes to its products in order to improve design, performance or reliability. Cypress Semiconductor Corporation assumes no responsibility for the use of its products in life supporting and medical applications where the failure or malfunction of the product could cause failure of the life supporting and medical systems. Products are not authorized for use in such applications unless a written approval is requested by the manufacturer and an approval is given in writing Cypress Semiconductor Corporation for the use of its products in the life supporting and medical applications.

Document Title: SM566 Spread Spectrum Clock Generator **Document Number:** 38-07023				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106951	06/05/01	IKA	Convert from IMI to Cypress
*A	122678	12/14/02	RBI	Added power up requirements to operating conditions information.