FAIRCHILD SEMICONDUCTOR®

August 2010

SG6741A
Highly Integrated Green-Mode PWM Controller

Features

- High-Voltage Startup
- Low Operating Current: 4mA
- Linearly Decreasing PWM Frequency to 18kHz
- Frequency Hopping to Reduce EMI Emissions
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- GATE Output Maximum Voltage Clamp: 18V
- V_{DD} Over-Voltage Protection (Auto Restart)
- V_{DD} Under-Voltage Lockout (UVLO)
- Internal Open-Loop Protection
- Constant Power Limit (Full AC Input Range)

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS

Description

The highly integrated SG6741A series of PWM controllers provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 18KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is eliminated. To further reduce power consumption, SG6741A is manufactured using the BiCMOS process, which allows an operating current of only 4mA.

SG6741A integrates a frequency-hopping function internally to reduce EMI emission of a power supply with minimum line filters. A built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit over a wide AC input voltages, from $90V_{AC}$ to 264 V_{AC}.

SG6741A provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety when an open-loop or output short-circuit failure occurs. PWM output is disabled until V_{DD} drops below the UVLO lower limit, when the controller starts up again. As long as V_{DD} exceeds ~26V, the internal OVP circuit is triggered.

SG6741A is available in an 8-pin SOP package.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
SG6741ASY	-40 to +105°C	8-Lead Small Outline Package (SOP)	Tape & Reel

Application Diagram

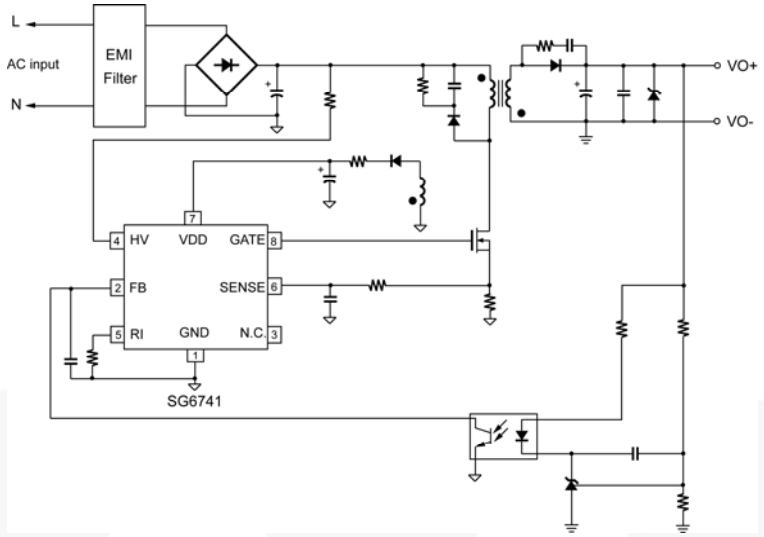


Figure 1. Typical Application

Block Diagram

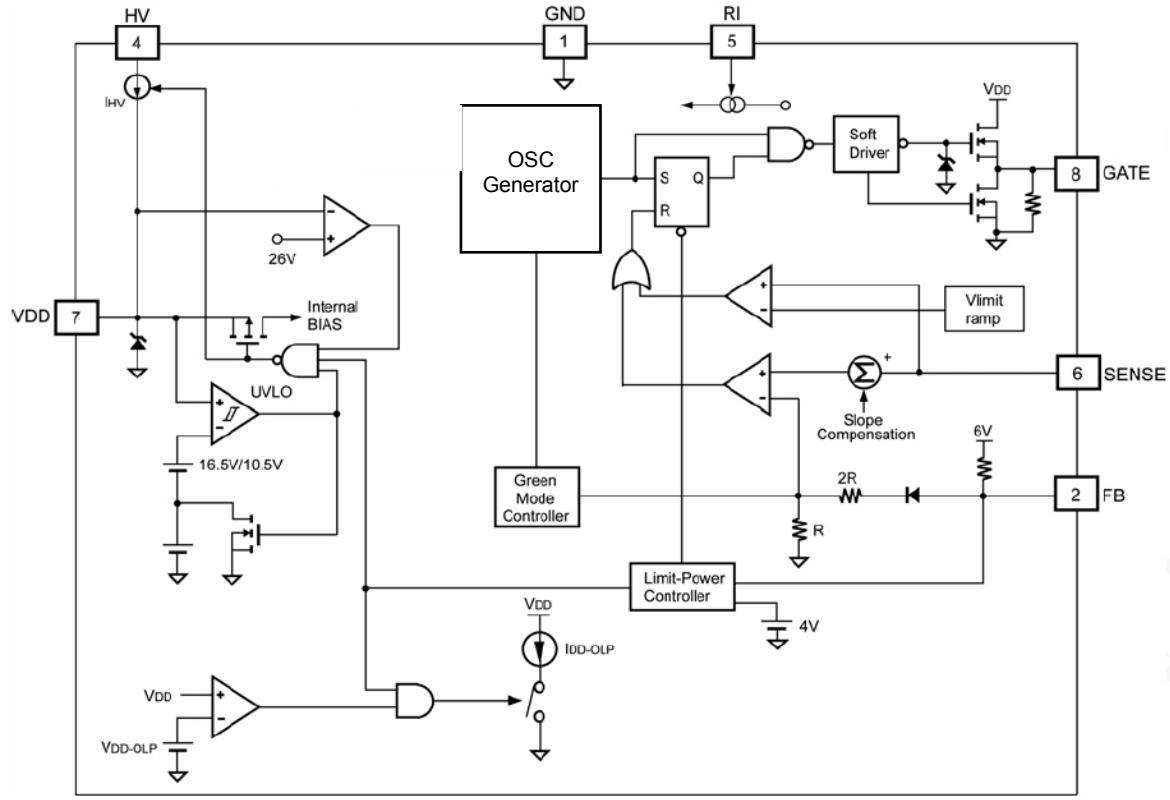
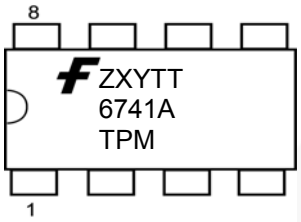


Figure 2. Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (S = SOP)
P: Y=Green Package
M: Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

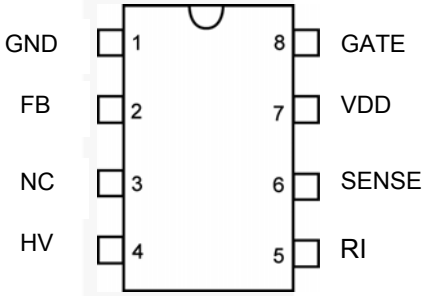


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	Ground.
2	FB	Feedback. The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the current-sense signal on SENSE pin.
3	NC	No Connection.
4	HV	Startup Input. For startup, this pin is pulled HIGH to the line input or bulk capacitor via resistors.
5	RI	Reference Setting. A resistor connected from the RI pin to GND pin provides a constant current source, which determines the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor for R_I results in a 65kHz center PWM frequency.
6	SENSE	Current Sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	VDD	Power Supply. The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.
8	GATE	Driver Output. Totem-pole output driver. Soft driving waveform is implemented for improved EMI.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to the ground pin.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage[1, 2]			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{SENSE}	SENSE Pin Input Voltage		-0.3	7.0	V
V_{RI}	RI Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			500	V
P_D	Power Dissipation (T_A＜50°C)			400	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			141	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114, All Pins Except HV Pin		4	kV
		Machine Model, JESD22-A115, All Pins Except HV Pin		200	V

Notes:
1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Electrical Characteristics

V_{DD}=15V; T_A=25C°, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-OP}	Continuously Operating Voltage				22	V
V_{DD-ON}	Start Threshold Voltage		15.5	16.5	17.5	V
V_{DD-OFF}	Minimum Operating Voltage		9.5	10.5	11.5	V
I_{DD-ST}	Startup Current	V_{DD-ON} – 0.16V			30	µA
I_{DD-OP}	Operating Supply Current	V_{DD}=15V, GATE Open		4	5	mA
I_{DD-OLP}	Internal Sink Current	V_{DD-OLP} +0.1V	50	70	90	µA
V_{DD-OLP}	I_{DD-OLP} off Voltage		6.5	7.5	8.0	V
V_{DD-OVP}	V_{DD} Over-Voltage Protection	Auto Restart	25	26	27	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time	Auto Restart	100	180	260	µs
HV Electrical Characteristics						
I_{HV}	Supply Current Drawn from HV Pin	V_{AC}=90V, (V_{DC}=120V) V_{DD}=10µF		2		mA
I_{HV-LC}	Leakage Current After Startup	HV=500V, V_{DD}=V_{DD-OFF}+1V		1	20	µA
Oscillator Section						
f_{OSC}	Frequency in Nominal Mode	Center Frequency	62	65	68	kHz
		Hopping Range	±3.7	±4.2	±4.7	
t_{HOP}	Hopping Period			4.4		ms
f_{OSC-G}	Green-Mode Frequency		16	18	21	kHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11V to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-20 to 85°C			5	%
Feedback Input Section						
A_V	Input Voltage to Current-Sense Attenuation		1/3.75	1/3.20	1/2.75	V/V
Z_{FB}	Input Impedance		4		7	kΩ
$V_{FB-OPEN}$	FB Output High Voltage	FB Pin Open	5.5			V
V_{FB-OLP}	FB Open-loop Trigger Level		3.7	4.0	4.3	V
t_{D-OLP}	The Delay Time of FB Pin Open-Loop Protection	R_I=26kΩ	50	56	62	ms
V_{FB-N}	Green-Mode Entry FB Voltage		1.9	2.1	2.3	V
V_{FB-G}	Green-Mode Ending FB Voltage			V_{FB-N} - 0.5		V
V_{FB-ZDC}	Zero Duty-Cycle Input Voltage			1		V

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Electrical Characteristics (Continued)

V_{DD}=15V; T_A=25C°, unless otherwise noted.

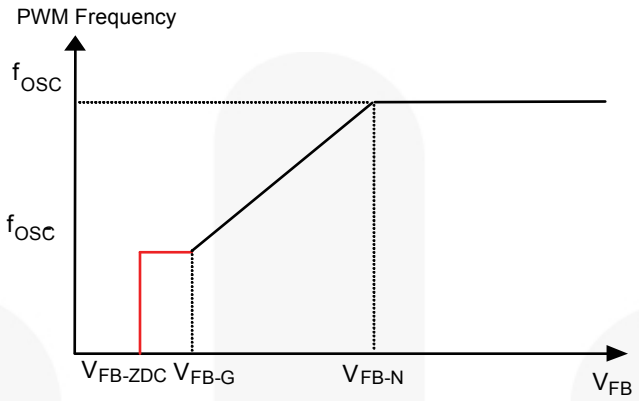

Figure 5. PWM Frequency

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Current Sense Section						
Z_{SENSE}	Input Impedance			12		KΩ
V_{STHFL}	Current Limit Flatten Threshold Voltage		0.87	0.90	0.93	V
V_{STHVA}	Current Limit Valley Threshold Voltage	V_{STHFL}–V_{STHVA}	0.18	0.22	0.26	V
t_{PD}	Delay to Output			100	200	ns
t_{LEB}	Leading-Edge Blanking Time		275	350	425	ns
Gate Section						
DCY_{MAX}	Maximum Duty Cycle		60	65	70	%
V_{GATE-L}	Gate Low Voltage	V_{DD}=15V, I_O=50mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=12.5V, I_O=-50mA	8			V
tr	Gate Rising Time	V_{DD}=15V, C_L=1nF	150	250	350	ns
tf	Gate Falling Time	V_{DD}=15V, C_L=1nF	30	50	90	ns
$I_{GATE-SOURCE}$	Gate Source Current	V_{DD}=15V, GATE=6V	250			mA
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V			18	V
DCY_{MAX}	Maximum Duty Cycle		60	65	70	%

Typical Performance Characteristics

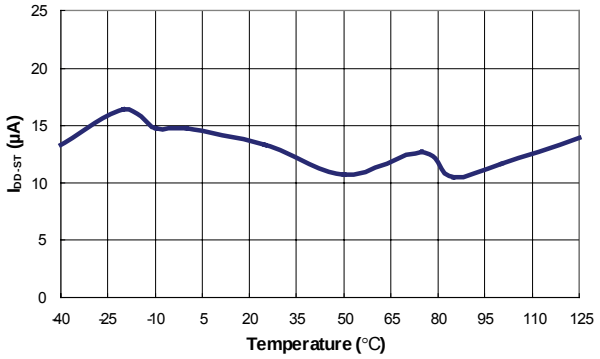

Figure 6. Startup Current (I_{DD-ST}) vs. Temperature

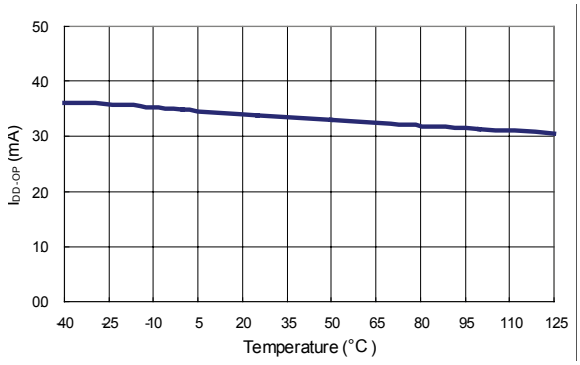

Figure 7. Operating Supply Current (I_{DD-OP}) vs. Temperature

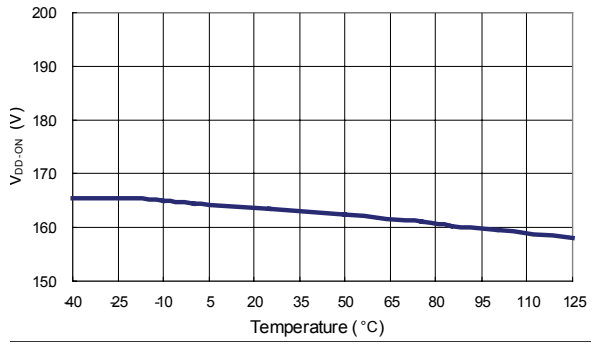

Figure 8. Start Threshold Voltage (V_{DD-ON}) vs. Temperature

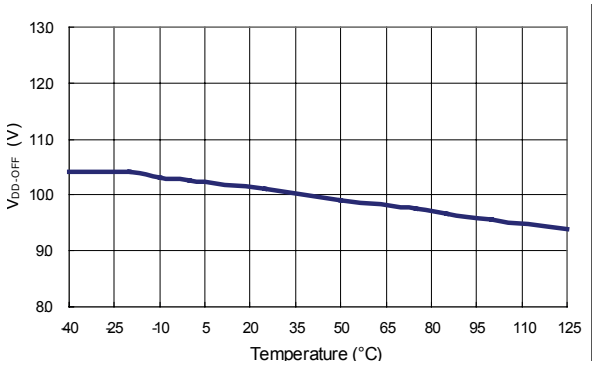

Figure 9. Minimum Operating Voltage (V_{DD-OFF}) vs. Temperature

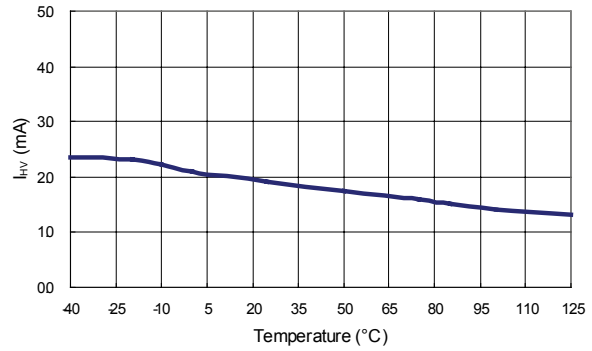

Figure 10. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

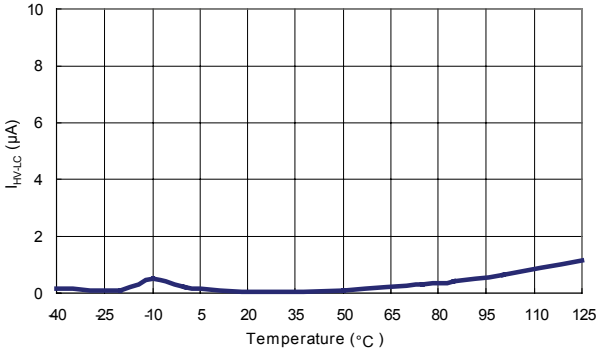

Figure 11. Leakage Current After Startup (I_{HV_LC}) vs. Temperature

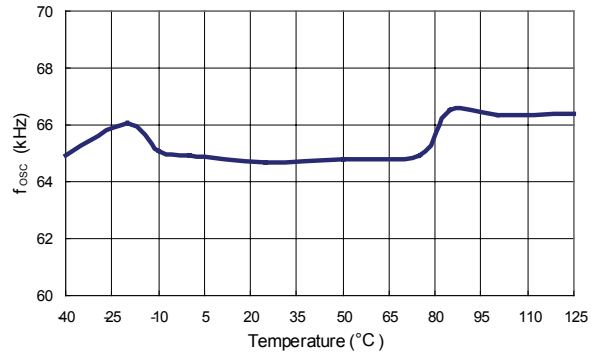

Figure 12. Frequency in Nominal Mode (f_{OSC}) vs. Temperature

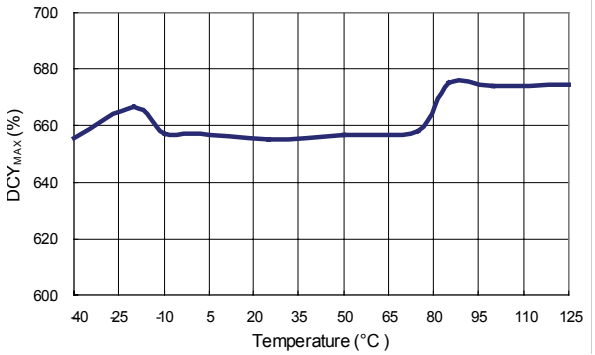

Figure 13. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Functional Description

Startup Current

For startup, the HV pin is connected to the line input or bulk capacitor through an external resistor, R_{HV}, which is recommended as 100KΩ. Typical startup current drawn from pin HV is 2mA and charges the hold-up capacitor through the resistor R_{HV}. When the V_{DD} capacitor level reaches V_{DD-ON}, the startup current switches off. At this moment, the V_{DD} capacitor only supplies the SG6741A to maintain V_{DD} before the auxiliary winding of the main transformer provides the operating current.

Operating Current

Operating current is around 4mA. The low operating current enables a better efficiency and reduces the requirement of V_{DD} hold-up capacitance.

Green-Mode Operation

The proprietary green-mode function provides an off-time modulation to reduce the switching frequency in the light-load and no-load conditions. The on-time is limited for better abnormal or brownout protection. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage, switching frequency is continuously decreased to the minimum green-mode frequency around 18KHz (R_I=26KΩ).

Oscillator Operation

A resistor connected from the RI pin to the GND pin generates a constant current source for the controller. This current is used to determine the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor R_I results in a corresponding 65KHz PWM frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{1690}{R_I\ (K\Omega)} (KHz) \quad (1)$$

The range of the PWM oscillation frequency is designed as 47kHz ~ 109kHz.

Current Sensing and PWM Current Limiting

Peak-current-mode control is utilized in SG6741A to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current sense signal and V_{FB}, the feedback voltage. When the voltage on the SENSE pin reaches around V_{COMP} = (V_{FB}–1.2)/3.2, a switch cycle terminates immediately. V_{COMP} is internally clamped to a variable voltage around 0.85V for output power limit.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.5V and 10.5V. During startup, the hold-up capacitor must be charged to 16.5V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10.5V during startup. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output / Soft Driving

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction is avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

Built-in Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability or prevents sub-harmonic oscillation. SG6741A inserts a synchronized positive-going ramp at every switching cycle.

Constant Output Power Limit

When the SENSE voltage, across the sense resistor R_s, reaches the threshold voltage, around 0.9V, the output GATE drive is turned off after a small delay, t_{PD}. This delay introduces an additional current proportional to t_{PD} • V_{IN} / L_P. Since the delay is nearly constant, regardless of the input voltage $V_{IN,}$ higher input voltage results in a larger additional current and the output power limit is higher than that under low input line voltage. To compensate this variation for wide AC input range, a sawtooth power-limiter is designed to solve the unequal power-limit problem. The power limiter is designed as a positive ramp signal fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs.

V_{DD} Over-voltage Protection (OVP)

V_{DD} over-voltage protection has been built in to prevent damage due to abnormal conditions. Once the V_{DD} voltage is over the V_{DD} over-voltage protection voltage (V_{DD-OVP}) and lasts for $t_{D-VDDOVP}$, the PWM pulses are disabled until the V_{DD} voltage drops below the UVLO, then starts again. Over-voltage conditions are usually caused by open feedback loops.

Limited Power Control

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold for longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned off, the supply voltage V_{DD} begins decreasing.

When V_{DD} goes below the turn-off threshold (~10.5V) the controller is totally shut down. V_{DD} is charged up to the turn-on threshold voltage of 16V through the startup resistor until PWM output is restarted. This protection feature continues as long as the overloading condition persists. This prevents the power supply from overheating due to overloading conditions.

Noise Immunity

Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the SG6741A, and increasing the power MOS gate resistance improve performance.

Reference Circuit

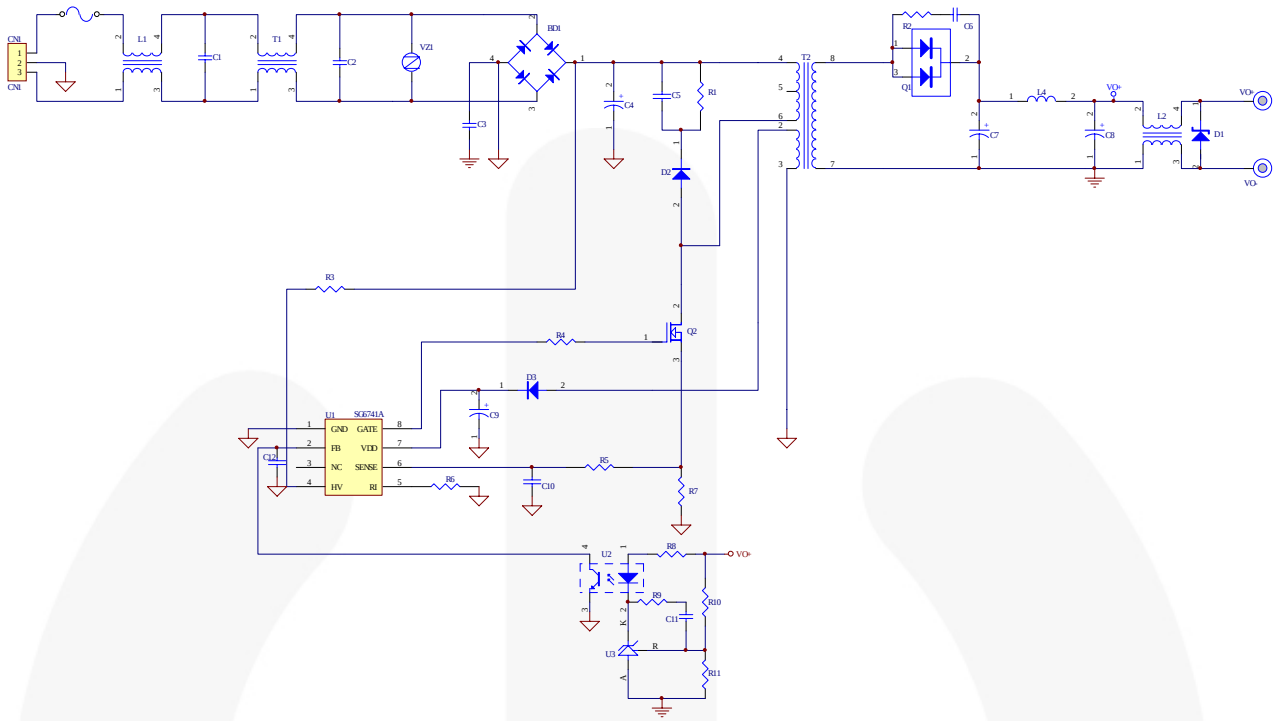

Figure 14. Circuit (12V/5A)

BOM

Reference	Component	Reference	Component
BD1	BD 4A/600V	Q2	MOS 7A/600V
C1	XC 0.68μF/300V	R1	R 100KΩ 1/2W
C2	XC 0.1μF/300V	R2	R 47Ω 1/4W
C3	YC 222pF/Y1	R3	R 100KΩ 1/2W
C4	EC 120μF/400V	R4	R 20Ω 1/8W
C5	CC 0.01μF/500V	R5	R 100Ω 1/8W
C6	CC 102pF/100V	R6	R 33KΩ 1/8W
C7	EC 1000μF/25V	R7	R 0.3Ω 2W
C8	EC 470μF/25V	R8	R 680Ω m 1/8W
C9	EC 22μF/50V	R9	R 4.7KΩ 1/8W
C10	CC 470pF/50V	R10	R 150KΩ m 1/8W
C11	CC 222pF/50V	R11	R 39KΩ 1/8W
C12	CC 103pF/50V	T1	10mH
D1	Zener Diode 15V 1/2W (option)	T2	600μH(PQ2620)
D2	BYV95C	U1	IC SG6741A
D3	FR103	U2	IC PC817
F1	FUSE 4A/250V	U3	IC TL431
L1	900μH	VZ1	VZ 9G
Q1	STP20-100CT		

Physical Dimensions

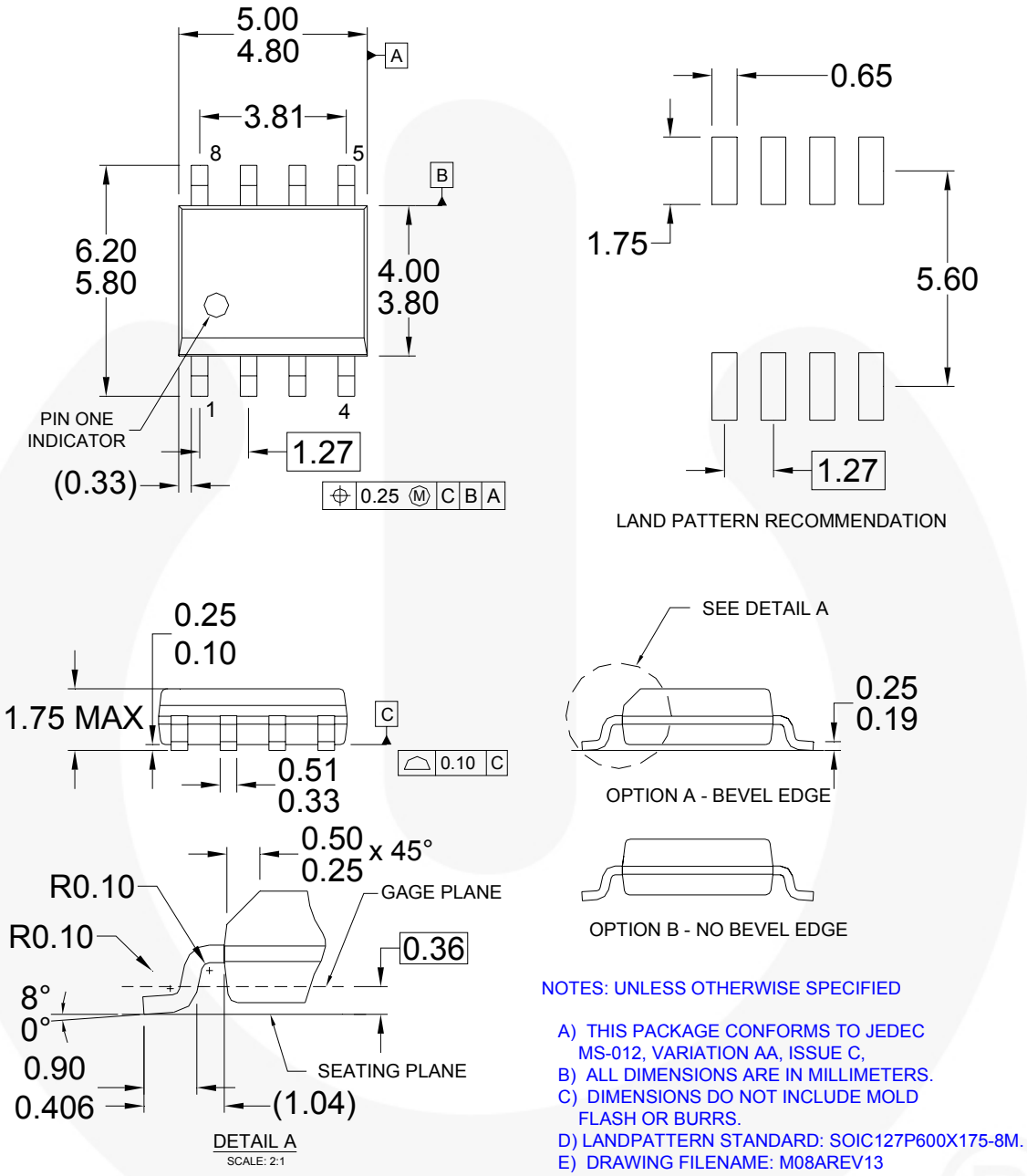

Figure 15. 8-Lead Small Outline Package (SOP)

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ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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