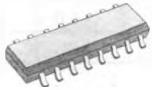
REGULATING PULSE WIDTH MODULATORS

- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT .. 8 mA TYPICAL
- OPERATION UP TO 300 KHz
- 1 % MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE

DESCRIPTION

The SG1524 , SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-ship reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shutdown circuitry.

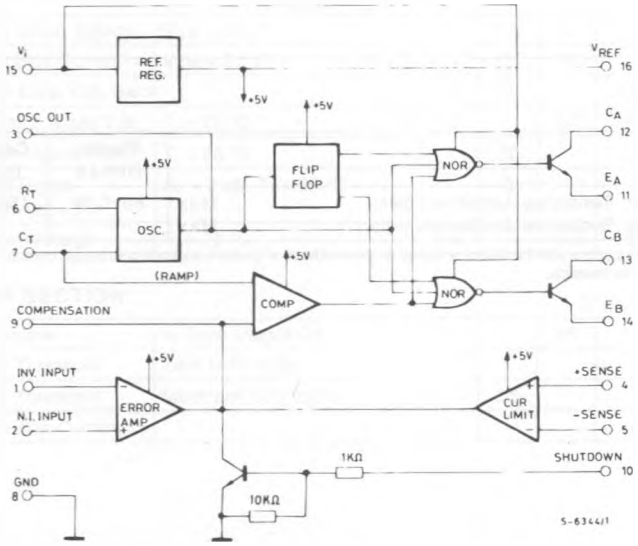
DIP-16
(Plastic –0.25– and Ceramic)



SO16 J

ORDER CODES SG1524J – SG2524J – SG3524J (Ceramic)
SG2524N – SG3524N (Plastic)
SG2524P – SG3524P (SO–16J)

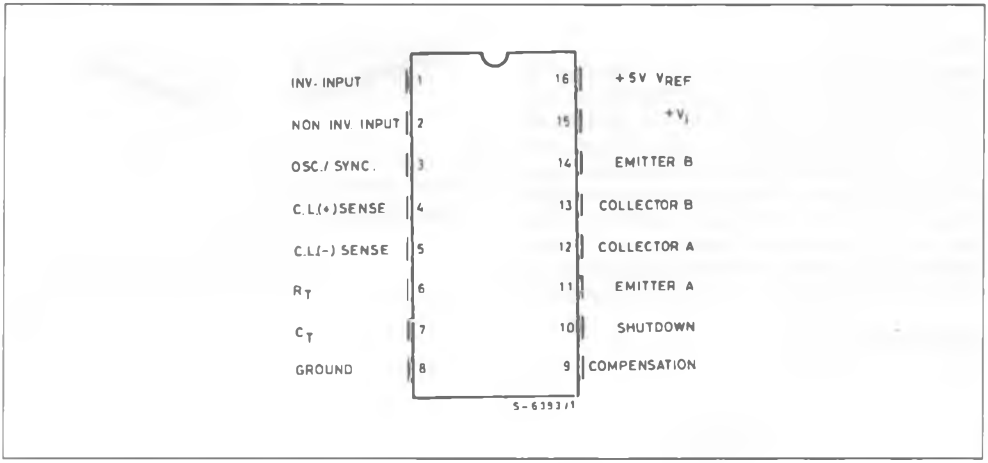
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	Supply Voltage	40	V
I_C	Collector Ouptut Current	100	mA
I_R	Reference Output Current	50	mA
I_T	Current Through C_T Terminal	– 5	mA
P_{tot}	Total Power Dissipation at Tamb = 70 °C	1000	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature Range **SG1524** **SG2524** **SG3524**	– 55 to 125 – 25 to 85 0 to 70	°C °C °C

CONNECTION DIAGRAMS



THERMAL DATA

			Plastic DIP-16	Ceramic DIP-16	SO16J
$R_{th\ j\text{-}amb}$	Themal Resistance Junction-ambient	Max	80 °C/W	150 °C/W	–
$R_{th\ j\text{-}aluminia}$	Themal Resistance Junction-aluminia	Max	–	–	50 °C/W

* Thermal resistance junction–alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness with infinite heatsink.

ELECTRICAL CHARACTERISTICS (unless otherwise stated , these specifications apply for T_j = – 55 °C to+ 125 °C for the SG1524, – 25 °C to + 85 °C for the SG2524, and 0 °C to + 70 °C for the SG3524, V_N = 20 V, and f = 20 KHz).

Symbol	Parameter	Test conditions	SG1524 SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage		4.8	5	5.2	4.6	5	5.4	V
ΔV_{REF}	Line Regulation	V_{IN} = 8 to 40 V		10	20		10	30	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
	Ripple Rejection	f = 120 Hz, T_j = 25 °C		66			66		dB
	Short Circuit Current Limit	V_{REF} = 0, T_j = 25 °C		100			100		mA
$\Delta V_{REF}/\Delta T$	Temp. Stability	Over Operating Temp. Range		0.3	1		0.3	1	%
ΔV_{REF}	Long Term Stability	T_j = 125 °C, t = 1000 Hrs		20			20		mV
OSCILLATOR SECTION									
f_{MAX}	Maximum Frequency	C_T = 0.001 µF, R_T = 2 kΩ		300			300		kHz
	Initial Accuracy	R_T and C_T Constant		5			5		%
	Voltage Stability	V_{IN} = 8 to 40 V, T_j = 25 °C			1			1	%
$\Delta f/\Delta T$	Temperature Stability	Over Operating Temp. Range			2			2	%
	Output Amplitude	Pin 3, T_j = 25 °C		3.5			3.5		V
	Output Pulse Width	C_T = 0.01 µF, T_j = 25 °C		0.5			0..5		µs
ERROR AMPLIFIER SECTION									
V_{OS}	Input Offset Voltage	V_{CM} = 2.5 V		0.5	5		2	10	mV
I_b	Input Bias Current	V_{CM} = 2.5 V		2	10		2	10	µA
G_V	Open Loop Volt. Gain		72	80		60	80		dB
CMV	Common Mode Volt.	T_j = 25 °C	1.8		3.4	1.8		3.4	V
CMR	Comm. Mode Rejec.	T_j = 25 °C		70			70		dB
B	Small Signal Bandwidth	A_v = 0 dB, T_j = 25 °C		3			3		MHz
V_O	Output Voltage	T_j = 25 °C	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION									
	Duty-cycle	% Each Output On	0		45	0		45	%
V_{IT}	Input Threshold	Zero Duty-cycle		1			1		V
V_{IT}	Input Threshold	Maximum Duty-cycle		3.5			3.5		V
I_b	Input Bias Current			1			1		µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	SG1524 SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT LIMITING SECTION									
	Sense Voltage	Pin 9 = 2 V With Error Amplifier Set for Max. Out, Tj = 25 °C	190	200	210	180	200	220	mV
	Sense Voltage T.C.			0.2			0.2		mV/°C
CMV	Common Mode Volt.		− 1		+ 1	− 1		+ 1	
OUTPUT SECTION (each output)									
	Collector-emitter Volt.		40			40			V
	Collector Leackage Cur.	V_{CE} = 40 V		0.1	50		0.1	50	µA
	Saturation Voltage	I_c = 50 mA		1	2		1	2	V
	Emitter Out. Voltage	V_{IN} = 20 V	17	18		17	18		V
t_r	Rise Time	R_c = 2 KΩ, T_j = 25 °C		0.2			0.2		µs
t_f	Fall Time	R_c = 2 KΩ, T_j = 25 °C		0.1			0.1		µs
I_q*	Total Standby Curr.	V_{IN} = 40 V		8	10		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Figure 1 : Open-loop Voltage Amplification of Error Amplifier vs. Frequency.

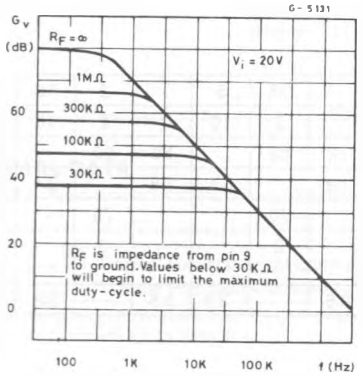


Figure 2 : Oscillator Frequency vs. Timing Components.

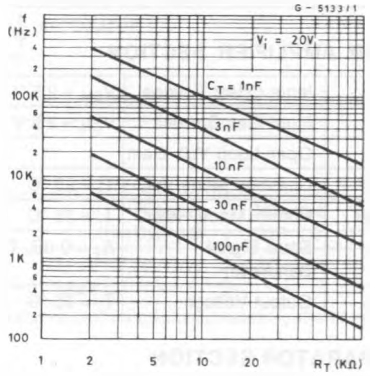


Figure 3 : Output Dead Time vs. Timing Capacitance Value.

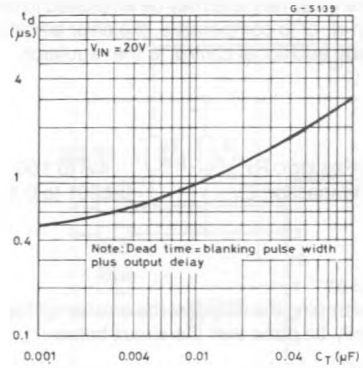


Figure 4 : Output Saturation Voltage vs. Load Current .

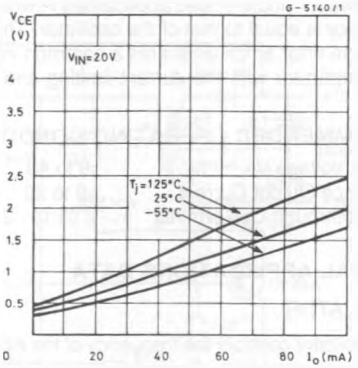
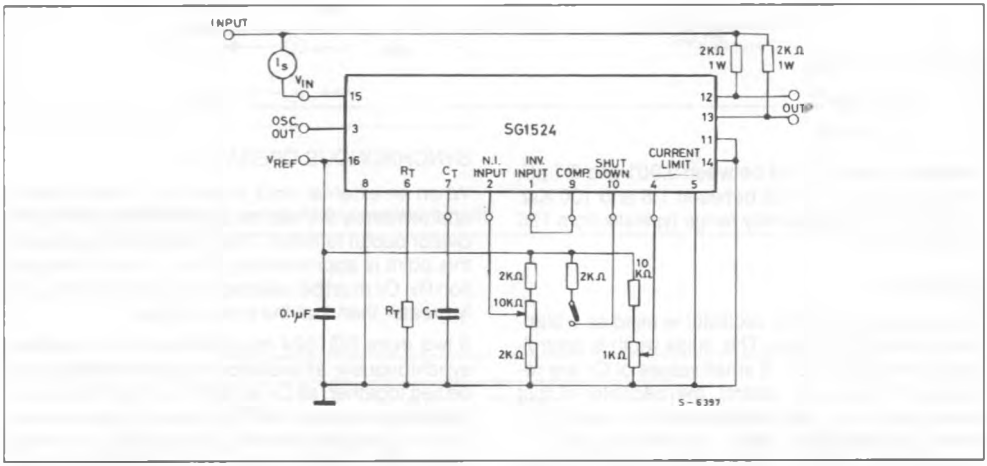


Figure 5 : Open Loop Test Circuit.



PRINCIPLES OF OPERATION

The SG1524 is a fixed-frequency pulse-with-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T established a constant charging current for C_T. This results in a linear voltage ramp at CT, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG1524 contains, an on-board 5 V regulator that serves as a reference as well as powering the SG1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generale a feedback signal to error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (Q_A or Q_B) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both output are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs

may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{IN}	8 to 40	V
Reference Output Current	0 to 20	mA
Current through C_T Terminal	- 0.03 to - 2	mA
Timing Resistor, R_T	1.8 to 100	KΩ
Timing Capacitor, C_T	0.001 to 0.1	µF

TYPICAL APPLICATIONS DATA

OSCILLATOR

The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T according to the approximate formula :

$$f = \frac{1.18}{R_T C_T}$$

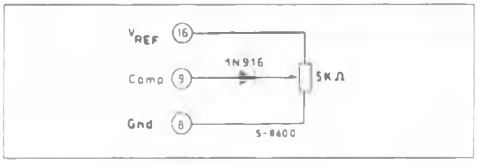
where R_T is in KΩ
C_T is in µF
f is in KHz

Pratical values of C_T fall between 0.001 and 0.1 µF. Pratical values of R_T fall between 1.8 and 100 KΩ. This results in a frequency range typically from 120 Hz to 500 KHz.

BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below :

Figure 6.



SYNCHRONOUS OPERATION

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator ouptut terminal. The impedance to ground at this point is approximately 2 KΩ. In this configuration R_T C_T must be selected for a clock period slightly greater than that the external clock.

If two more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Figure 7: Flyback Converter Circuit.

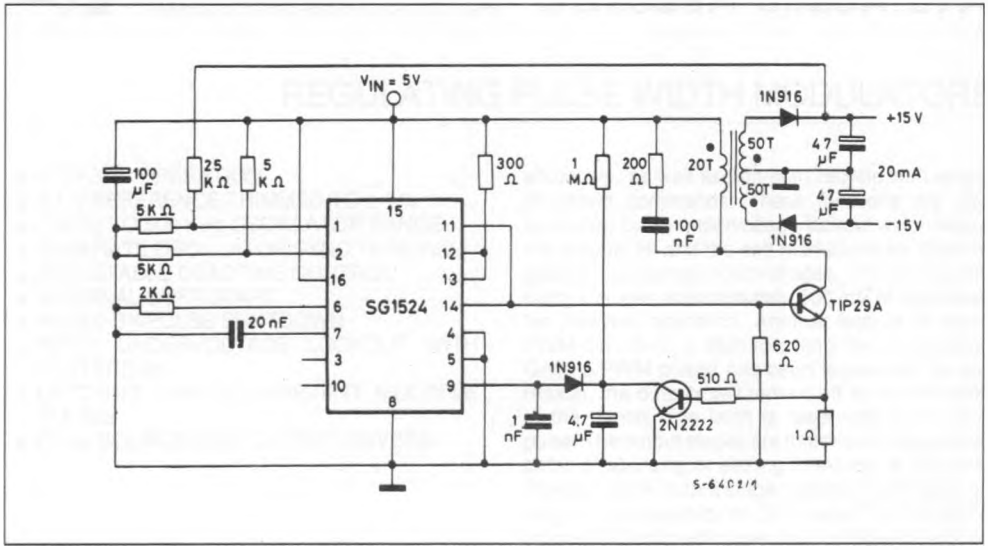


Figure 8: PUSH-PULL transformer-coupled circuit.