Signetics

Linear Products

NE/SE5060
Precision High-Speed Sample-and-Hold Amplifier

Preliminary Specification

DESCRIPTION

The NE/SE5060 is a high-performance, monolithic sample-and-hold amplifier that features high accuracy, low droop rate, and fast acquisition times required in high-speed data acquisition systems.

The circuit consists of two high impedance buffer amplifiers connected by an analog switch. In the sample mode, the device is in a non-inverting unity-gain configuration. The switch (S2) (see Block Diagram) is implemented as a unique switchable output stage of the input buffer which has been optimized for fast charging of the hold capacitor and a low sample-to-hold step size. In the hold mode, the input signal is effectively disconnected from the circuit by switch S1 to give a low feedthrough, and GM2 maintains 0V across the switch S2, ensuring a low droop rate. The device includes a 100pF hold capacitor. If lower droop rates and smaller sample-to-hold step error is desired at the expense of acquisition time, additional hold capacitance may be added externally. The voltage at the hold capacitor is buffered by the output buffer amplifier to drive the external load.

The device utilizes high voltage ion-implanted JFETs to obtain the low droop rates. The circuit has been designed to minimize the initial zero offset error, which is trimmed at the wafer level to be less than 0.5mV. The NE5060 operates from ±9V to ±17V power supplies with little or no change in the specification as long as the peak input voltage is not within 4V of the supplies.

FEATURES

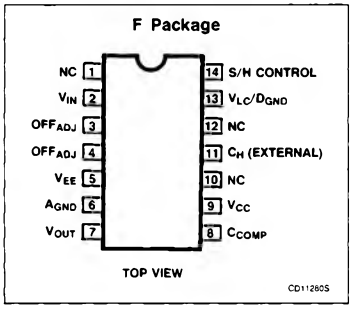
- **Voltage gain** **0.99970**
- **Low signal non-linearity** **0.0035%**
- **Low offset error** **0.5mV**
- **Fast acquisition time** **850ns**
- **Low sample-to-hold step** **1mV**
- **Low droop rate** **0.2μV/μs**
  +25°C (SE/NE5060) **0.2μV/μs**
  +70°C (NE5060) **2.0μV/μs**
  +125°C (SE5060) **150.0μV/μs**
- **Internal 100pF hold capacitor**
- **TTL CMOS Logic compatible**
- **Functional equivalent replacement for HA2420, HA2425, HA5320, AD583 and SMP11**

APPLICATIONS

- **Precision data acquisition systems**
- **D/A converter deglitching**
- **Auto-zero circuits**
- **Peak detectors**

PIN CONFIGURATION

F Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Hermetic Cerdip	0 to +70°C	NE5060F
14-Pin Hermetic Cerdip	−55°C to +125°C	SE5060F

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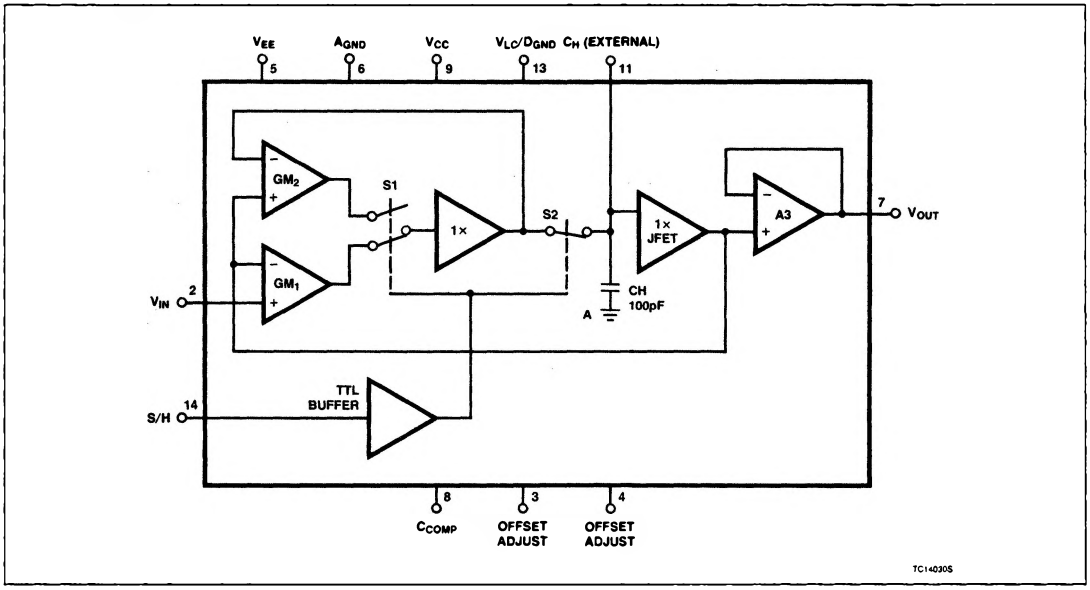
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Voltage between V_{CC} and V_{EE}	36	V
V_{IN}	Analog input voltage	±15	V
$V_{S/H}$	Logic input voltage	±15	V
V_{LC}	Logic reference voltage	±15	V
I_{SC}	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	60	s
P_D	Maximum power dissipation T_A = 25°C (still-air)[1]	1190	mW
T_A	Operating temperature range NE5060 SE5060S[2]	0 to +70 −55 to +125	°C °C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTES:

1. Derate above 25°C at 9.5mW/°C.
2. Operation above 110°C ambient requires that a heat sink be provided so as not to exceed the recommended maximum junction temperature of 150°C.
   θ_{JA} = 110°C/W
   θ_{JC} = 30°C/W
   $T_J = V_{CC} \times I_{CC} \times 0.8 \times \theta_{JA}$
   $= 15\ (15 + 14) \times 0.8 \times 110°C/W$
   = 38.2°C

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DC ELECTRICAL CHARACTERISTICS

Test conditions, unless otherwise noted:
V_{CC} = 15V; V_{EE} = −15V; −10V ≤ V_{IN} ≤ 10V; V_{LC} = 0V; $V_{S/H}$ < 0.8V (for sample mode); $V_{S/H}$ > 2.0V (for hold mode); C_H = Internal; device in sample mode; 0°C ≤ T_A ≤ +70°C for NE5060; −55°C ≤ T_A ≤ +125°C for SE5060.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5060			SE5060			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{ZS}	Zero-scale error	V_{IN} = 0V; T_A = 25°C T_{MIN} to T_{MAX}		0.5 1.0	 2.0		0.5 3.0	 4.0	mV mV
I_{BIAS}	Input bias current	V_{IN} = 0V		70	150		70	250	nA
R_{IN}	Input resistance		150	250		100	250		MΩ
A_V	Voltage gain	V_{IN} = ± 10V T_A = 25°C T_{MIN} to T_{MAX}	 0.99960 0.99950	 0.99975 0.99965		 0.99960 0.99930	 0.99975 0.99955		V/V V/V V/V
E_L	Linearity error	V_{IN} = ± 10V, R_L = 5kΩ		0.0035	0.007		0.0035	0.008	%
V_{INR}	Input voltage range		± 10.5	± 11		± 10.5	± 11		V
R_{OUT}	Output resistance			0.15	0.5		0.15	0.5	Ω
I_{LOAD}	Output load current (@ R_O < 0.5Ω)	V_{IN} = ± 10V; T_A = 25°C T_{MIN} to T_{MAX}	± 10 ± 8	± 15 ± 11		± 10 ± 7	± 15 ± 11		mA mA
V_{IH}	Logic "1" voltage		2.0			2.0			V
V_{IL}	Logic "0" voltage				0.8			0.8	V
I_{IH}	Logic input current high	$V_{S/H}$ = 5V			0.1			0.1	μA
I_{IL}	Logic input current low	$V_{S/H}$ = 0V			−15			−15	μA
$E_{N\ RMS}$	Output noise	DC to 260kHz		250			250		μV
V_{CC}	Positive supply voltage[1]		13.5	15	16.5	13.5	15	16.5	V
V_{EE}	Negative supply[1]		−13.5	−15	−16.5	−13.5	−15	−16.5	V
I_{CC}	Positive supply current			11.5	15		11.5	15	mA
I_{EE}	Negative supply current			−11.5	−14		−11.5	−14	mA
PSRR+	Positive supply rejection ratio	V_{CC} = 15V ± 5% V_{IN} = 0V V_{IN} = ± 10V	 85 80	 100 90		 85 80	 100 90		dB dB dB
PSRR−	Negative supply rejection ratio	V_{EE} = −15V ± 5% V_{IN} = 0V V_{IN} = ± 10V	 65 57	 72 63		 65 57	 72 63		dB dB

NOTE:
1. Recommend operating supply voltage range for V_{IN} = ± 10V; DC specification production tested only at ± 15V.

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AC ELECTRICAL CHARACTERISTICS Test conditions, unless otherwise specified:
V_{CC} = 15V; V_{EE} = −15V; V_{IN} = 0V; V_{LC} = 0V; R_L = 2kΩ; C_L = 50pF; C_H = Internal;
$V_{S/H}$ = 0.4V (for sample mode); $V_{S/H}$ = 3.5V (for hold mode); T_A = +25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
SR	Slew rate[1]		16	20		V/μs
	Overshoot[1]			6		%
BW	Full power bandwidth	V_{IN} = 20V_{P-P}		260		kHz
t_{AQ}	Acquisition time,[1, 2]			850	1250	ns
t_{APD}	Aperture delay			30		ns
t_{AP}	Aperture time			25		ns
t_{APU}	Aperture uncertainty			1		ns
V_{HT}	Sample – Hold transient (peak to peak)[3]			2	15	mV
t_{HM}	Hold mode settling[2, 3]			35	125	ns
Q_t	Charge transfer[3]			0.1	0.25	pC
	Hold step[3, 4]			1.0	2.5	mV
dV_H/dt	Drop rate	T_A = +25°C 0°C to +70°C −55°C to +125°C		0.2 2 150	 5 200	μV/μs μV/μs μV/μs
I_D	Drop current	T_A = +25°C 0°C to +70°C −55°C to +125°C		2 100 10	 500 20	pA pA nA
	Hold mode feedthrough	V_{IN} = 10V_{P-P}; 100kHz		2		mV

NOTES:
1. V_{IN} = ±10V step.
2. To within 1.0mV of its final value (0.01%).
3. $V_{S/H\ (HIGH)}$ = 3.5V; t_R = 50ns (V_{IL} to V_{IH}).
4. Can be adjusted to zero.

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APPLYING THE NE/SE5060

The NE/SE5060 is a high-performance sample-and-hold amplifier. In the track mode the device behaves as a non-inverting unity gain amplifier. In the hold mode the device holds the value of the output voltage that was present at the instant the sample-to-hold signal goes high.

Hold Capacitor

The NE/SE5060 includes an on-chip hold capacitor and achieves fast acquisition, low hold step, and droop rate which are adequate for most high-speed applications. However, if a smaller hold step and lower droop rate are desired, then an external hold capacitor (C_H) may be added from Pin 11 to ground (Pin 6). The external hold capacitor should have high insulation resistance and low dielectric absorption to minimize droop errors.

If an external hold capacitor is used, then additional compensation capacitance of value $0.03C_H$ should be connected between Pin 8 and ground. Exact value and type are not critical. The additional hold capacitor will reduce the slew rate and increase acquisition time.

Offset Adjustment

The NE/SE5060 hold step error can be adjusted to zero using the offset adjustment pins as shown in the 'Typical Connections'. The error should be adjusted with the device in the hold mode, so that both the initial offset error and the hold-step error are nulled to zero. If desired, the center-tap of the offset adjustment potentiometer may be connected to V_{CC} through a 1MΩ resistor in series with the center-tap of the potentiometer.

Layout and Other Considerations

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01μF to 0.1μF ceramic) should be provided for each power supply terminal to Pin 6 as close to the device as possible.

The ideal ground connections are as follows:

- a wide trace between Pin 6 and Pin 13
- Pin 6 to each power supply ground
- a separate trace from Pin 6 to the signal ground
- Pin 13 to digital ground.

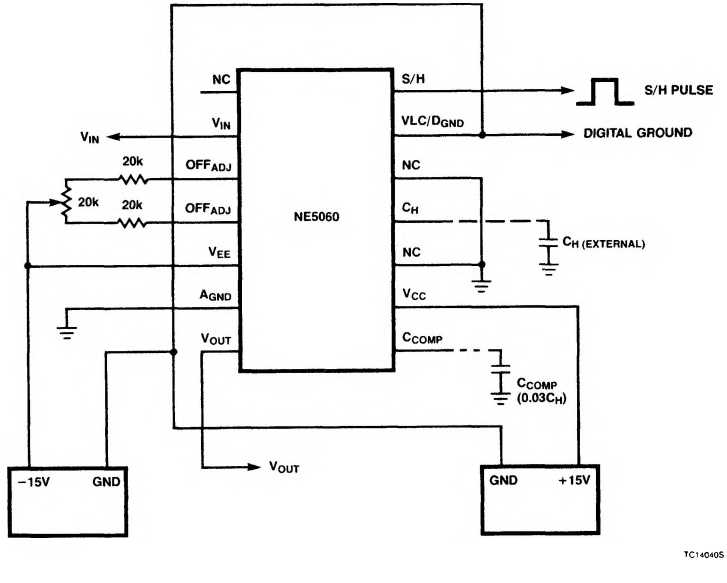
The hold capacitor (Pin 11) is sensitive to stray coupling. Any connection made to this pin should be kept short and guarded by a ground plane since nearby signal lines or power supply voltages will introduce errors in the hold mode.

In unity gain applications requiring no external hold capacitor, the NE/SE5060 can directly replace the HA2420, HA2425, and HA5320. In applications requiring an additional hold capacitor, it should be remembered that the capacitor should be connected from Pin 11 to ground.

Sample/Hold Input

Optimum performance is achieved with a clean (no ringing) sample-to-hold pulse with a rise time between 20ns and 50ns.

NE/SE5060 is compatible with all logic families. For TTL and DTL interface, simply ground Pin 13. The internal threshold voltage is set to 1.4V above the voltage at Pin 13. For CMOS and HTL interface, the appropriate voltage may be applied to Pin 13. For proper operation the voltage applied at Pin 13 must be at least 4V below the positive supply and 3V above the negative supply.



NOTE:
C_H and C_{COMP} required only if external hold capacitance is desired.

Figure 1. NE5060 Typical Connections