TOPAZ SEMICONDUCTOR

SD5200

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET DRIVER ARRAY

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD5200CHP
16-Pin Plastic Dual In-Line Package	SD5200N
Description	30V, 80 ohm

FEATURES

- Normally OFF configuration
- Low Interelectrode capacitance
- High-speed switching

APPLICATIONS

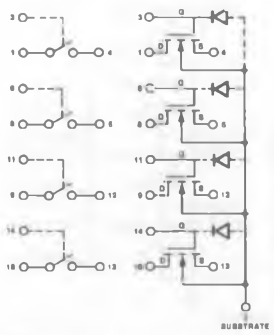
- +30V Analog Switch Drivers
- Wide-Band Dual Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS (per channel, T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage ..... +30Vdc
V_{SD} Source-Drain Voltage ..... +0.5Vdc
V_{DB} Drain-Body Voltage ..... +30Vdc
V_{SB} Source-Body Voltage ..... +15Vdc
V_{GS} Gate-Source Voltage ..... +25Vdc
V_{GB} Gate-Body Voltage ..... +25Vdc
Gate-Body Voltage ..... −0.3Vdc
V_{GD} Gate-Drain Voltage ..... +25Vdc, -30Vdc
I_D Continuous Drain Current 50mA

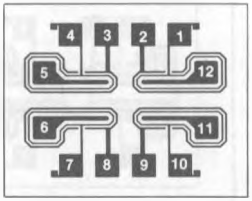
P_D Total Package Power Dissipation
(at or below T_A = +25°C) 640mW
Linear Derating Factor ..... 10.7mW/°C
P_D Single Device Power Dissipation
(at or below T_A = +25°C) 300mW
Linear Derating Factor ..... 5.0mW/°C
T_j Operating Junction Temperature
Range ..... −55 to +85°C
T_S Storage Temperature Range .. −55 to +150°C

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

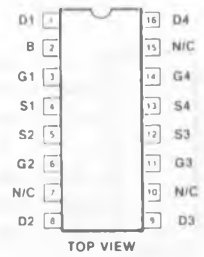
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

Dimensions: .041 × .033 × .020 inches

PIN CONFIGURATION



TOP VIEW

DIMENSIONS
16-Pin Plastic DIP
See Package 10

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD5200 MIN	SD5200 TYP	SD5200 MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	30	35		V	$I_D = 10\mu A, V_{GS} = V_{BS} = 0$
2	STATIC	BV_{SB}	Source-Substrate Breakdown Voltage	15			V	$I_S = 10\mu A$, $V_{GB} = 0$ Drain Open
3	STATIC	I_{GBS}	Gate-Body Leakage Current			1.0	μA	$V_{GB} = 25V, V_{DB} = V_{SB} = 0$
4	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.0	2.0	V	$V_{DS} = V_{GS}, I_D = 1.0\mu A$ $V_{SB} = 0$
5	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		50	80	ohms	$V_{GS} = 5V$
6	STATIC				30		ohms	$V_{GS} = 10V$
7	STATIC				23		ohms	$V_{GS} = 15V$
8	STATIC				19		ohms	$V_{GS} = 20V$
								$I_D = 1mA$ $V_{SB} = 0$
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10	12		mmhos	$V_{DS} = 10V, I_D = 20mA$ $f = 1KHz, V_{SB} = 0$
10	DYNAMIC	$c_{(gs + gd + gb)}$	Gate Node Capacitance		2.4	3.5	pF	
11	DYNAMIC	$c_{(gd + db)}$	Drain Node Capacitance		1.3	1.5	pF	$f = 1MHz$ $V_{DS} = 10V$ $V_{GS} = V_{BS} = -15V$
12	DYNAMIC	$c_{(gs + sb)}$	Source Node Capacitance		3.5	4.0	pF	
13	DYNAMIC	$c_{(dg)}$	Reverse Transfer Capacitance		0.3	0.5	pF	
14	DYNAMIC	C_T	Cross Talk		−107		dB	