TOPAZ SEMICONDUCTOR

SD5100, SD5101

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET ANALOG SWITCH ARRAYS

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD5100CHP	SD5101CHP
14-Pin Plastic Dual In-Line Package	SD5100N	SD5101N
SO-14 Package	SD5100CY	SD5101CY
Description	30V, 70 ohm	15V, 70 ohm

FEATURES

- Common source for 4 channels
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

APPLICATIONS

- +30V Switch Drivers—SD5100
- +15V Switch Drivers—SD5101

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	SD5100	SD5101	UNITS
V_{DS}	+30	+15	Vdc
V_{SD}	+0.5	+0.5	Vdc
V_{DB}	+30	+15	Vdc
V_{SB}	+0.5	+0.5	Vdc
V_{GS}	+20	+20	Vdc
V_{GB}	+20	+20	Vdc
	−0.3	−0.3	Vdc
V_{GD}	+20	+20	Vdc
	−30	−15	Vdc

I_D Continuous Drain Current 50mA

P_D Total Package Power Dissipation (at or below T_A = +25°C) 640mW

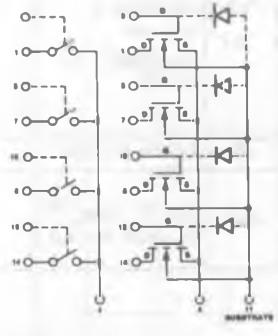
Linear Derating Factor ..... 10.67mW/°C

P_D Single Device Power Dissipation (at or below T_A = +25°C) 300mW

T_j Operating Junction Temperature Range ..... −55 to +85°C

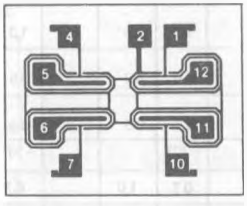
T_S Storage Temperature Range .. −55 to +150°C

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

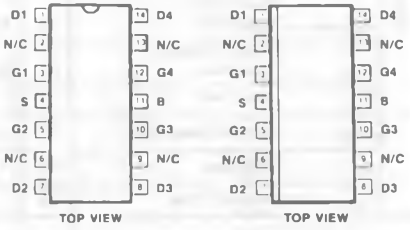
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source	10	Gate No. 4
4	Gate No. 2	11	Drain No. 4
5	Drain No. 2	12	Drain No. 1
6	Drain No. 3		

Dimensions: .041 × .033 × .020 inches

PIN CONFIGURATION



DIMENSIONS

14-Pin Plastic DIP
See Package 9

SO-14 Plastic
See Package 20

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD5100			SD5101			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	30	35		15	30		V	I_D = 1.0μA, V_{GS} = V_{BS} = 0
2		BV_{SD}	Source-Drain Breakdown Voltage	0.5			0.5			V	I_S = 10nA, V_{GD} = V_{BD} = 0
3		BV_{DB}	Drain-Substrate Breakdown Voltage	30			15			V	I_D = 1.0μA, V_{GB} = 0 Source Open
4		BV_{SB}	Source-Substrate Breakdown Voltage	0.5			0.5			V	I_S = 100nA, V_{GB} = 0 Drain Open
5		$I_{D(off)}$	Drain-Source OFF Current		1.0	10		1.0	10	nA	V_{DS} = 10V, V_{GS} = V_{BS} = 0
6		I_{GBS}	Gate-Substrate Leakage Current			10			10	μA	V_{GS} = 20V, V_{DB} = V_{SB} = 0
7		$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.0	2.0	0.5	1.0	2.0	V	I_D = 1.0μA, V_{DS} = V_{GS} V_{SB} = 0
8		$r_{DS(on)}$	Drain-Source ON Resistance		50	70		50	70	ohms	V_{GS} = 5V; I_D = 1mA, V_{SB} = 0
9					30	45		30	45	ohms	V_{GS} = 10V; I_D = 1mA, V_{SB} = 0
10					23			23		ohms	V_{GS} = 15V; I_D = 1mA, V_{SB} = 0
11					19			19		ohms	V_{GS} = 20V; I_D = 1mA, V_{SB} = 0
12		r_{DSM}	ON Resistance Match		1.0	5.0		1.0	5.0	ohms	V_{GS} = 5V; I_D = 1mA, V_{SB} = 0
13	DYNAMIC	g_{fs}	Common-Source Forward Transcond	10	15		10	15		mmhos	V_{DS} = 10V, I_D = 20mA f = 1KHz, V_{SB} = 0
14		$c_{(gs+gd+gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5	pF	V_{DS} = 10V V_{GS} = V_{BS} = −5V f = 1MHZ
15		$c_{(gd+db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		
16		c_{dg}	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		
17		C_T	Cross Talk		−107			−107		dB	f = 3KHz, R_G = 600Ω