

# 5-BIT SHIFT REGISTER | S5496 N7496

S5496-B,F,W • N7496-B, F

DIGITAL 54/74 TTL SERIES

## DESCRIPTION

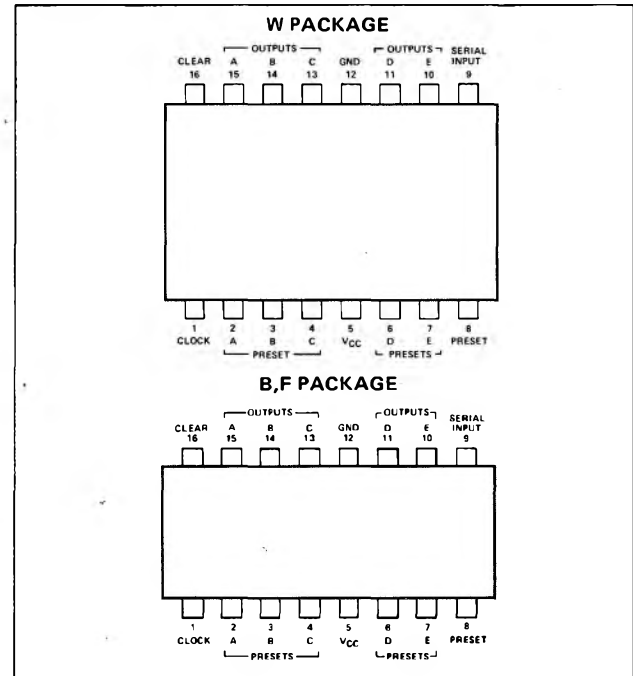
This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

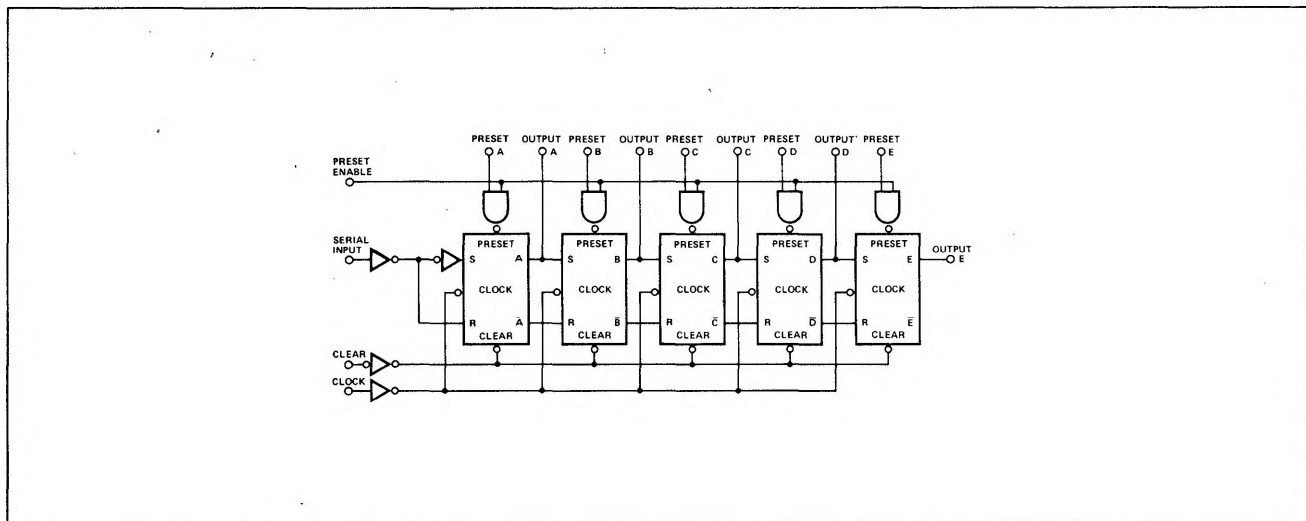
The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

## PIN CONFIGURATIONS



## LOGIC DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Supply Voltage $V_{CC}$ (See Note 1):				
S5496 Circuits	4.5	5	5.5	V
N7496 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output			10	
Width of Clock Pulse, $t_p(\text{clock})$	35			ns
Width of Clear Pulse, $t_p(\text{clear})$	30			ns
Width of Preset Pulse, $t_p(\text{preset})$	30			ns
Serial Input Setup Time, $t_{\text{setup}}$	30			ns
Serial Input Hold Time, $t_{\text{hold}}$	0			ns

NOTE: 1. This voltage value is with respect to network ground terminal.

SIGNETICS DIGITAL 54/74 TTL SERIES - S5496 • N7496

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$				0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}, I_{load} = -400\mu\text{A}$		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}, I_{sink} = 16\text{mA}$			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset (pin 8)	$V_{CC} = \text{MAX}, V_{in} = 2.4\text{V}$				40	$\mu\text{A}$
		$V_{CC} = \text{MAX}, V_{in} = 5.5\text{V}$				1	mA
$I_{in(1)}$	Logical 1 level input current at preset (pin 8)	$V_{CC} = \text{MAX}, V_{in} = 2.4\text{V}$				200	$\mu\text{A}$
		$V_{CC} = \text{MAX}, V_{in} = 5.5\text{V}$				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset (pin 8)	$V_{CC} = \text{MAX}, V_{in} = 0.4\text{V}$				-1.6	mA
		$V_{CC} = \text{MAX}, V_{in} = 0.4\text{V}$				-8	mA
$I_{OS}$	Short-circuit output current†	$V_{CC} = \text{MAX}, V_{out} = 0$		-20		-57	mA
				-18		-57	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$			48	68	mA
					48	79	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{max}$	Maximum clock frequency	$C_L = 15\text{pF}, R_L = 400\Omega$		10			MHz
$t_{pd1}$	Propagation delay time to logical 1 level from clock to output	$C_L = 15\text{pF}, R_L = 400\Omega$			25	40	ns
	Propagation delay time to logical 0 level from clock to output	$C_L = 15\text{pF}, R_L = 400\Omega$			25	40	ns
$t_{pd1}$	Propagation delay time to logical 1 level from preset to output	$C_L = 15\text{pF}, R_L = 400\Omega$				35	ns
$t_{pd0}$	Propagation delay time to logical 0 level from preset to output	$C_L = 15\text{pF}, R_L = 400\Omega$			28	40	ns
$t_{pd0}$	Propagation delay time to logical 0 level from clear to output	$C_L = 15\text{pF}, R_L = 400$				55	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

\*\* All typical values are at  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ .

† Not more than one output should be shorted at a time.