4-BIT BINARY COUNTER

S5493
N7493

S5493–A,F,W • N7493–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5493/N7493 is a high-speed, monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

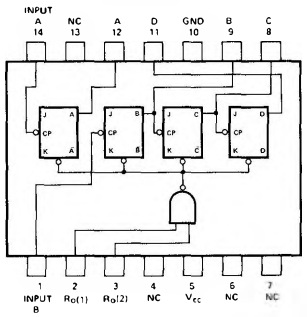
1. When used as a 4-bit ripple-through counter output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

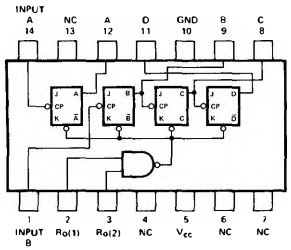
The S5493/N7493 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 32mW per flip-flop (128mW total).

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



TRUTH TABLE (See Notes 1 and 2)

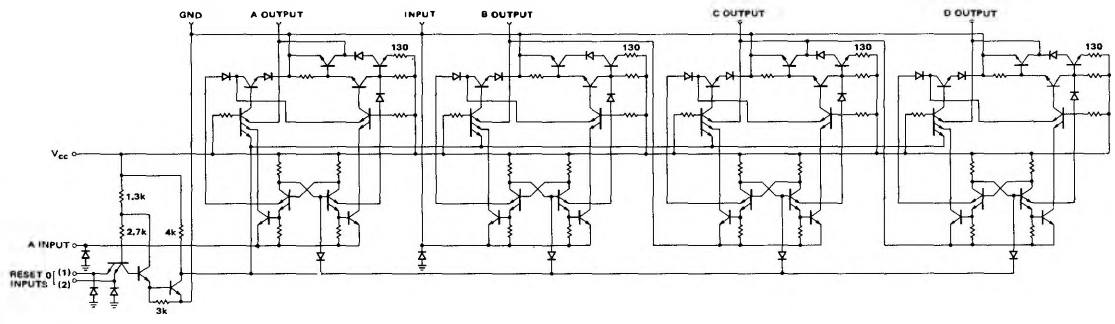
LOGIC

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

COUNT	OUTPUT			
	D	C	B	A
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES:
1. Output A connected to input B.
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5493 Circuits	4.5	5	5.5	V
	N7493 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5493 Circuits	-55	25	125	°C
	N7493 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{out} = 0	S5493 N7493	-20 -18		-57 -57	mA mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5493 N7493		32 32	46 53	mA mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		75	135	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.