# QUADRUPLE BISTABLE LATCH

# S5477
# N7477

S5477W • N7477W

DIGITAL 54/74 TTL SERIES

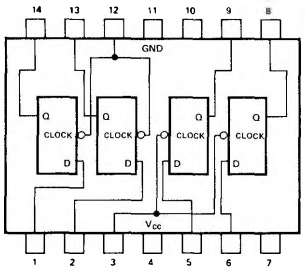
## DESCRIPTION

The S5477Q/N7477Q is a monolithic, quadruple, bistable latch with Q outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

## PIN CONFIGURATIONS

W PACKAGE




## TRUTH TABLE

### LOGIC

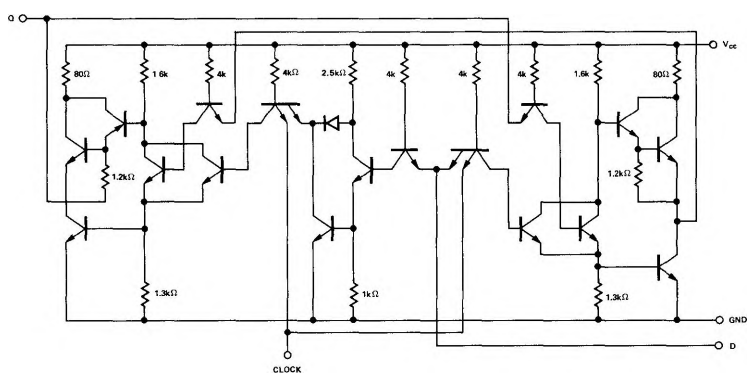
| (Each Latch) | |
|---|---|
| $t_n$ | $t_{n+1}$ |
| D | Q |
| 1 | 1 |
| 0 | 0 |

NOTES:
1. $t_n$ = bit time before clock pulse.
2. $t_{n+1}$ = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 3): | S5477 Circuits | 4.5 | 5 | 5.5 | V |
| | N7477 Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from each Output, N | | | | 10 | |
| Operating Free-Air Temperature Range, $T_A$: | S5477 Circuits | -55 | 25 | 125 | °C |
| | N7477 Circuits | 0 | 25 | 70 | °C |

## SCHEMATIC (each latch)



**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS* | | | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 level at any input terminal | $V_{CC}$ = MIN | | | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 0 level at any input terminal | $V_{CC}$ = MIN | | | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | $V_{CC}$ = MIN, | $I_{load}$ = −400μA | | 2.4 | | | V |
| $V_{out(0)}$ | Logical 0 output voltage | $V_{CC}$ = MIN, | $I_{sink}$ = 16mA | | | | 0.4 | V |
| $I_{in(0)}$ | Logical 0 level input current at D | $V_{CC}$ = MAX, | $V_{in}$ = 0.4V | | | | −3.2 | mA |
| $I_{in(0)}$ | Logical 0 level input current at clock | $V_{CC}$ = MAX, | | | | | −6.4 | mA |
| $I_{in(1)}$ | Logical 1 level input current at D | $V_{CC}$ = MAX,<br>$V_{CC}$ = MAX, | $V_{in}$ = 2.4V<br>$V_{in}$ = 5.5V | | | | 80<br>1 | μA<br>mA |
| $I_{in(1)}$ | Logical 1 level input current at clock | $V_{CC}$ = MAX,<br>$V_{in}$ = 2.4V,<br>$V_{CC}$ = MAX, | <br><br>$V_{in}$ = 5.5V | | | | 160<br><br>1 | μA<br><br>mA |
| $I_{OS}$ | Short circuit output current† | $V_{CC}$ = MAX,<br>$V_{out}$ = 0 | | S5477<br>N7477 | −20<br>−18 | | −75<br>−75 | mA<br>mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, | | S5477<br>N7477 | | 32<br>32 | 46<br>53 | mA<br>mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{setup1}$ | Minimum logical 1 level input setup time at D input | $C_L$ = 15pF, | $R_L$ = 400Ω | | 7 | 20 | ns |
| $t_{setup0}$ | Minimum logical 0 level input setup time at D input | $C_L$ = 15pF, | $R_L$ = 400Ω | | 14 | 20 | ns |
| $t_{hold1}$ | Maximum logical 1 level input hold time required at D input | $C_L$ = 15pF, | $R_L$ = 400Ω | 0 | 15¶ | | ns |
| $t_{hold0}$ | Maximum logical 0 level input hold time required at D input | $C_L$ = 15pF, | $R_L$ = 400Ω | 0 | 6¶ | | ns |
| $t_{pd1(D-Q)}$ | Propagation delay time to logical 1 level from D input to Q output | $C_L$ = 15pF, | $R_L$ = 400Ω | | 16 | 30 | ns |
| $t_{pd0(D-Q)}$ | Propagation delay time to logical 0 level from D input to Q output | $C_L$ = 15pF, | $R_L$ = 400Ω | | 14 | 25 | ns |
| $t_{pd1(C-Q)}$ | Propagation delay time to logical 1 level from clock input to Q output | $C_L$ = 15pF, | $R_L$ = 400Ω | | 16 | 30 | ns |
| $t_{pd0(C-Q)}$ | Propagation delay time to logical 0 level from clock input to Q output | $C_L$ = 15pF, | $R_L$ = 400Ω | | 7 | 15 | ns |

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurring prior to the fall of clock pulse ($t_0$) below 1.5V when data at the D input will still be recognized and stored.