

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S5472 Circuits	4.5	5	5.5	V
N7472 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A : S5472 Circuits	-65	25	125	°C
N7472 Circuits	0	25	70	°C
Normalized Fan-Out From each Output, N			10	
Width of Clock Pulse, $t_p(\text{clock})$	20			ns
Width of Preset Pulse, $t_p(\text{preset})$	25			ns
Width of Clear Pulse, $t_p(\text{clear})$	25			ns
Input Setup Time, t_{setup}	$\geq t_p(\text{clock})$			
Input Hold Time, t_{hold}	0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}$, $I_{\text{load}} = -400\mu\text{A}$	2.4	3.5		V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}$, $I_{\text{sink}} = 16\text{mA}$		0.22	0.4	V
$I_{in(0)}$ Logical 0 level input current at J1, J2, J3, K1, K2, or K3	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at preset, clear, or clock	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J1, J2, J3, K1, K2, or K3	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$.40 1	μA mA
$I_{in(1)}$ Logical 1 level input current at preset, clear, or clock	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			80 1	μA mA
I_{OS} Short circuit output current†	$V_{CC} = \text{MAX}$, $V_{in} = 0$	S5472 N7472	-20 -18	-57 -57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, $V_{in} = 5\text{V}$		10	20	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock} Maximum clock frequency	$C_L = 15\text{pF}$, $R_L = 400\Omega$	15	20		MHz
t_{pd1} Propagation delay time to logical 1 level from clear or preset to output	$C_L = 15\text{pF}$, $R_L = 400\Omega$		16	25	ns
t_{pd0} Propagation delay time to logical 0 level from clear or preset to output	$C_L = 15\text{pF}$, $R_L = 400\Omega$		25	40	ns
t_{pd1} Propagation delay time to logical 1 level from clock to output	$C_L = 15\text{pF}$, $R_L = 400\Omega$	10	16	25	ns
t_{pd0} Propagation delay time to logical 0 level from clock to output	$C_L = 15\text{pF}$, $R_L = 400\Omega$	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$. † Not more than one output should be shorted at a time.