DESCRIPTION

The S5470/N7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The S5470/N7470 flip-flop is ideally suited for medium- and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

TRUTH TABLE

LOGIC

J_n	K_n	Q_{n+1}	PRESET	CLEAR	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	Q

$J = J_1 J_2 J^*$ $\quad K = K_1 K_2 K^*$

n is time prior to clock

n+1 is time following clock

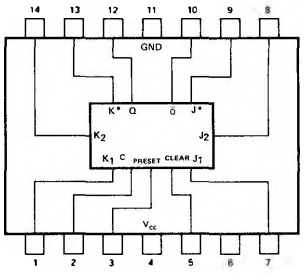
† Both outputs in 0 state

POSITIVE LOGIC

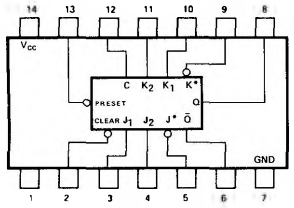
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

PIN CONFIGURATIONS

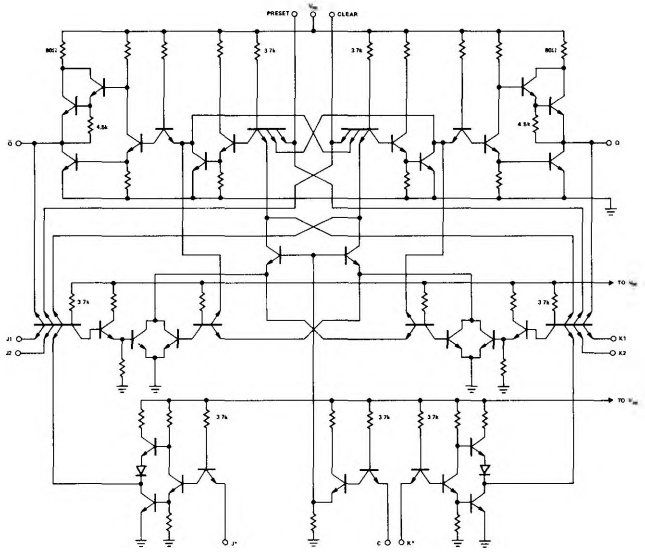
W PACKAGE



A,F PACKAGE



SCHEMATIC DIAGRAM



NOTE: Component values are typical.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5470 Circuits	4.5	5	5.5	V
	N7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5470 Circuits	−55	25	125	°C
	N7470 Circuits	0	25	70	°C
Normalized Fanout from each Output, N				10	
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$		5		150	ns
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Preset Pulse, $t_{p(preset)}$		25			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J*, K1, K2, K*, or clock	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 0.4V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5470 N7470	−20 −18		−75 −75	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			13	26	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	35		MHz
t_{setup}	Minimum Input Setup time	C_L = 15pF,	R_L = 400Ω		10	20	ns
t_{hold}	Minimum input hold time	C_L = 15pF,	R_L = 400Ω		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	18	50	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.