Features

- **Low-noise Low Drop Out Voltage Regulator**
- **2.6V Fixed Output Voltage**
- **3V to 5.5V Supply Operation**
- **160 mA Maximum Load Current**
- **Less Than 46 µA (max) Quiescent Current**
- **Power-down Mode Consumption Less Than 1 µA**
- **More Than 60 dB (Typical) PSRR at 1 kHz**
- **68µ V_{RMS} Output Noise**
- **0.35 µm CMOS Technology**
- **Typical Application: Baseband Section Supply in Mobile Terminals**

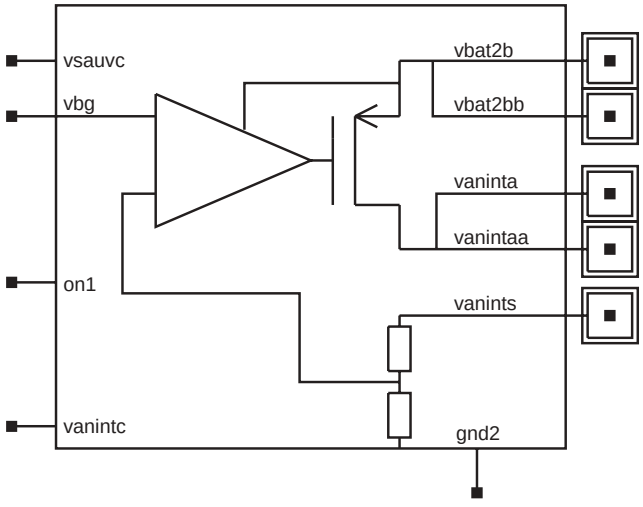
Description

RE023 is a Low Drop Out (LDO) voltage regulator macrocell with a fixed 2.6V output voltage, rated for loads up to 160 mA. It is designed to be integrated with other analog cells, digital logic, microcontrollers, DSP cores and memory blocks into system-on-chip products.

The circuit consists of a PMOS pass device, an error amplifier and a feedback resistive network, sized to achieve the required closed loop gain. These blocks make up the regulating loop. An over-current and short circuit protection circuit has been included to limit the output current delivered by the regulator, thus avoiding destruction in case of a short circuit.

An external reference voltage (bandgap voltage) is necessary for correct functionality. The target reference voltage is 1.231V, delivered, for example, by BG019. Double pads on the supply voltage V_{BAT2B}/V_{BAT2BB} and output voltage V_{ANINTA}/$V_{ANINTAA}$ are used to reduce the total output resistance. Current reference is generated inside the cell through a circuit supplied by a 2.5V ± 0.1V regulated input voltage on V_{SAUVC}. Remote sense terminal V_{ANINTS} provides regulation at the load by connecting it to the output terminal near a critical point to improve performance of the regulator (e.g., connecting them at the package pin by double-bonding, thus avoiding the bonding resistance influence). A ceramic capacitor of 2.2 µF connected from V_{ANINTA}/$V_{ANINTAA}$ to ground is needed as external compensation.

Figure 1. Symbol(1)



Note: 1. Pin names are written as they appear on the user screen when the symbol is opened in the design tool environment.

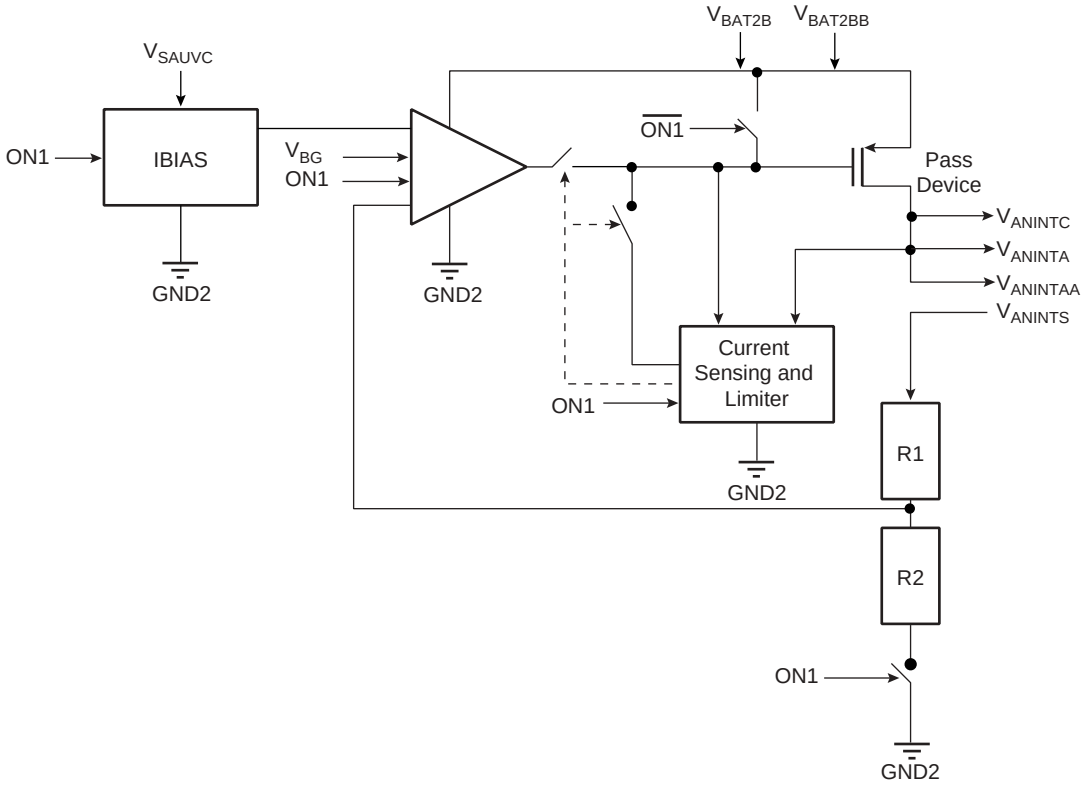
Embedded ASIC Macrocell: Power Management for Mobile Terminals (PM)

RE023 Fixed 2.6V 160 mA LDO Voltage Regulator

Rev. 2702B-PMGMT–02/03

Functional Diagram

Figure 2. Functional Diagram



Pin Description

Pin Name	I/O	Type	Function	Value
V_{BAT2B}	Power supply	External pad	Power supply	3V to 5.5V
V_{BAT2BB}	Power supply	External pad	Power supply	3V to 5.5V
V_{ANINTA}	Analog output	External pad	Output voltage	2.5V to 2.7V
$V_{ANINTAA}$	Analog output	External pad	Output voltage	2.5V to 2.7V
V_{ANINTS}	Analog output	External pad	Sense voltage	2.5V to 2.7V
V_{ANINTC}	Analog output	Internal pin	Output voltage	2.5V to 2.7V
GND2	Ground	Internal pin	Ground	0
V_{SAUVC}	Power supply	Internal pin	Power supply	2.5V ± 0.1V
V_{BG}	Analog input	Internal pin	Voltage reference	1.231V
ON1	Digital input	Internal pin	Enable command	0 or V_{BAT2B}/V_{BAT2BB}

Absolute Maximum Ratings*

V_{IN}	-0.3V to 6.5V
Digital Signals	-0.3V to 5.5V
Output Current	Internally Limited
Junction Temperature	-40°C to 150°C

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications(1)

T_J = -20°C to 125°C, V_{BAT2B}/V_{BAT2BB} = 3V to 5.5V unless otherwise specified, output capacitance = 2.2 µF.

Table 1. Electrical Specifications

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{BAT2B}/V_{BAT2BB}	Operating Supply Voltage			3		5.5	V
V_{SAUVC}	Auxiliary Operating Supply Voltage			2.4	2.5	2.6	V
T_J	Junction Temperature Range			-20		125	°C
V_{ANINTA}/ $V_{ANINTAA}$	Output Voltage			2.5	2.6	2.7	V
I_{ANINTA}/ $I_{ANINTAA}$	Output Current					160	mA
I_{QQ}	Quiescent Current					46	µA
ΔV_{DC}	Line Regulation	$I_{ANINTA}/I_{ANINTAA}$ = 160 mA			2	3	mV
ΔV_{TRAN}	Transient Line Regulation	$I_{ANINTA}/I_{ANINTAA}$ = 160 mA rise time = fall time = 5 µs			4	7	mV
ΔV_{DC}	Load Regulation	10% - 90% of max $I_{ANINTA}/I_{ANINTAA}$			2	3	mV
ΔV_{TRAN}	Transient Load Regulation	10% - 90% of max $I_{ANINTA}/I_{ANINTAA}$ rise time = fall time = 5 µs			5	10	mV
PSRR	Power Supply Rejection Ratio at Full Load	V_{BAT} = 3V	@100 Hz		-65		dB
			@1 kHz		-60		dB
			@20 kHz		-40		dB
			@100 kHz		-30		dB
		V_{BAT} = 4.25V	@100 Hz		-60		dB
			@1 kHz		-60		dB
			@20 kHz		-50		dB
			@100 kHz		-40		dB
		V_{BAT} = 5.5V	@100 Hz		-55		dB
			@1 kHz		-55		dB
			@20 kHz		-48		dB
			@100 kHz		-40		dB

Table 1. Electrical Specifications (Continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_N	Output Noise(2)	Bandwidth: 10 Hz to 100 kHz output current = 160 mA			68	81	μV_{RMS}
T_R	Rise Time	100% of $I_{ANINTA}/I_{ANINTAA}$ 10% - 90% $V_{ANINTA}/V_{ANINTAA}$				70	µs
I_{SD}	Shut Down Current					1	µA
I_{CC}	Short-circuit current					400	mA

Notes: 1. Obtained by considering the parasitics of a TFBGA100 Package.
2. Obtained by using BG019 as reference voltage generator.

Control Modes

All digital signals are referred to the supply voltage $V_{BAT2B/BAT2BB}$.

Table 2. Truth Table

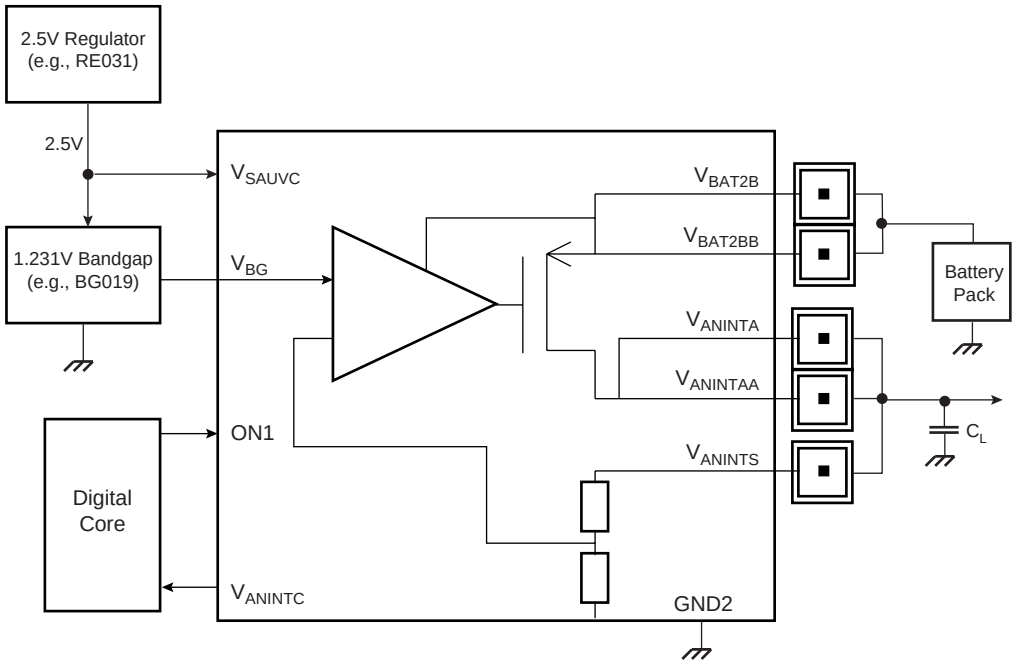
ON1	$V_{ANINTA}/V_{ANINTAA}$
0	Power down (High-Z)
1	Power on, $V_{ANINTA}/V_{ANINTAA}$ = 2.6V

Application Example

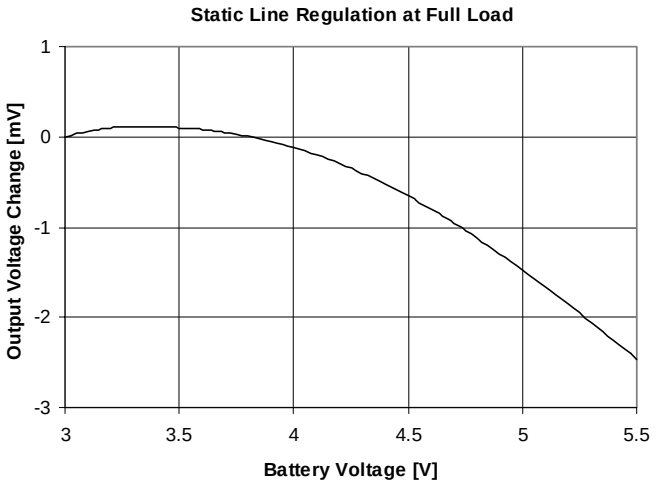
A ceramic capacitor of 2.2 µF with ESR between 20 mΩ and 250 mΩ connected from $V_{ANINTA}/V_{ANINTAA}$ to ground is needed as external compensation.

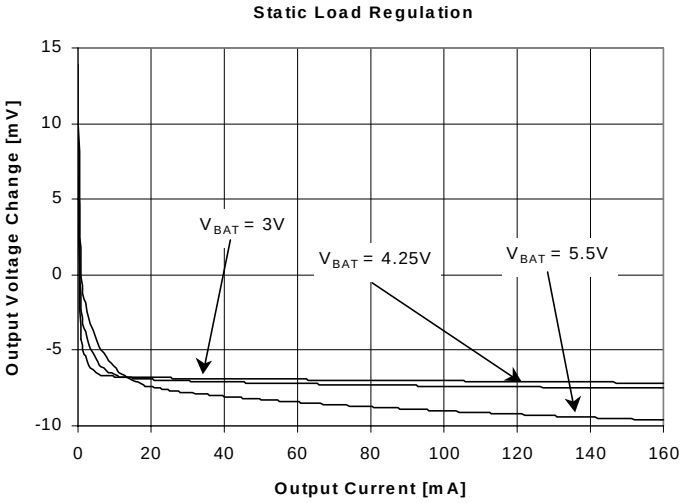
Description	Min	Typ	Max	Units
Capacitor, C_L	1.8	2.2	2.6	µF

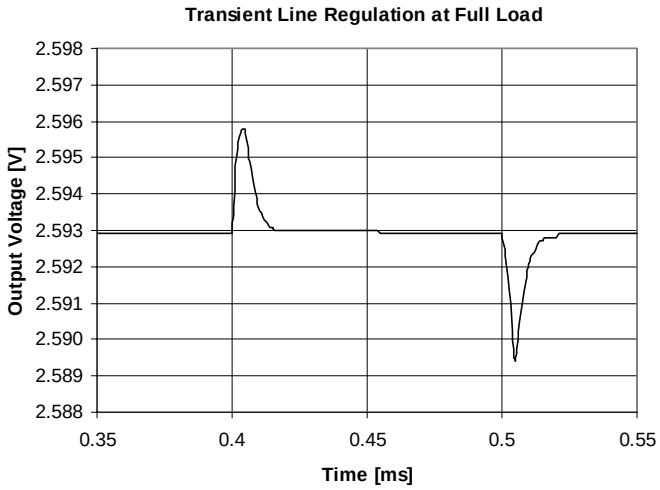
Figure 3. Application Example

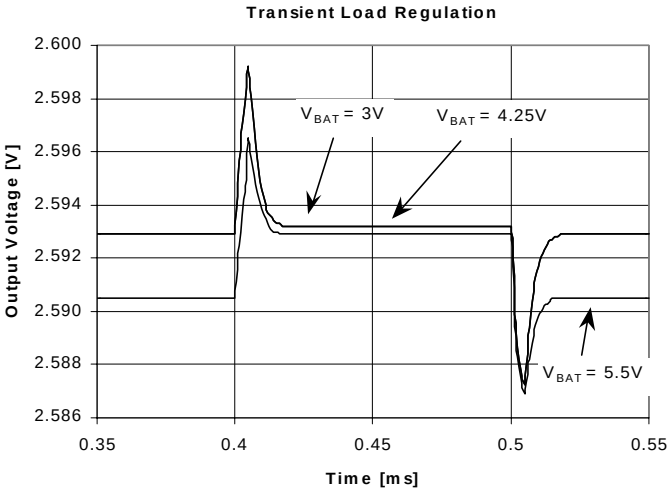


Typical Performance Characteristics (Conditions specified on page 8)









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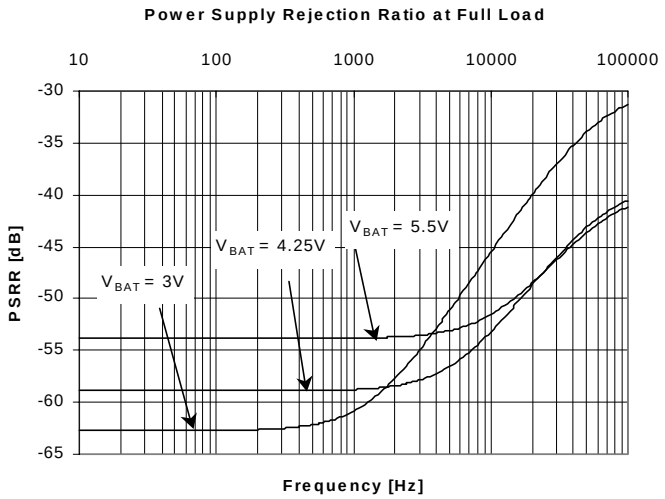
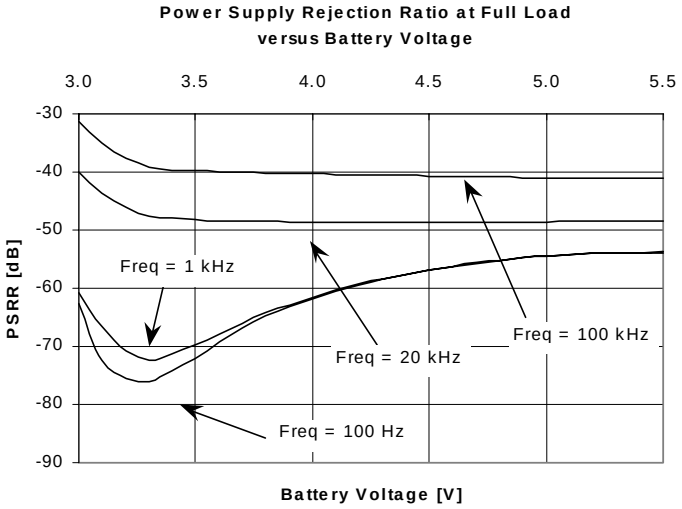
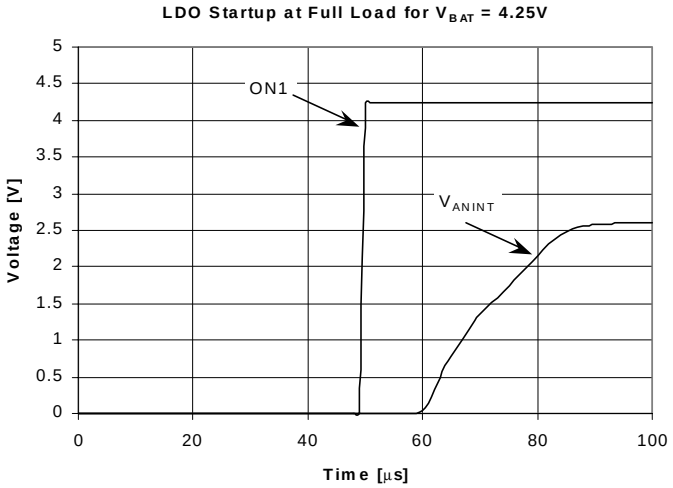
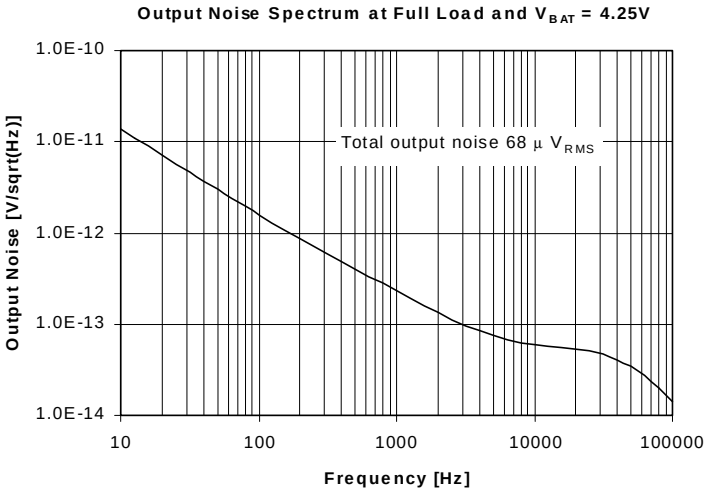






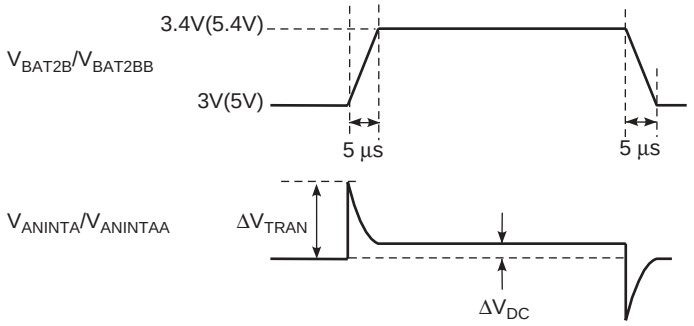


Terminology

Line Regulation

Measures the maximum transient and DC variations of the output voltage of the LDO when the supply changes between two specified values with fixed load current; minimum rise time and fall time is 5 µs.

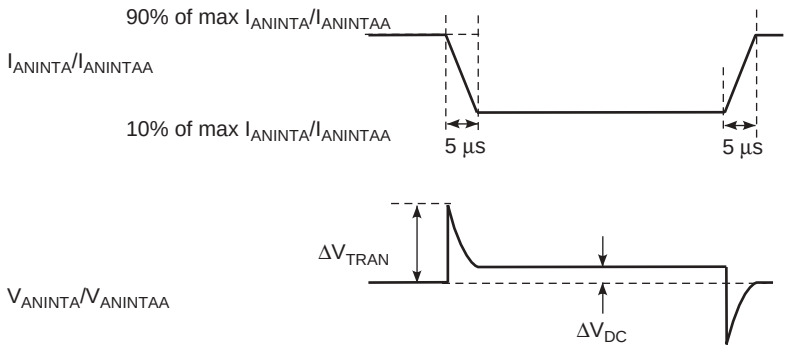
Figure 4. Line Regulation



Load Regulation

Measures the maximum transient and DC variations of the output voltage of the LDO when the load current changes between two specified values with fixed power supply; minimum rise time and fall time is 5 µs.

Figure 5. Load Regulation



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