Signetics

PCF2100
LCD Duplex Driver

Product Specification

Linear Products

DESCRIPTION

The PCF2100 is a single-chip, silicon-gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 40 segments in a duplex manner, especially for low-voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

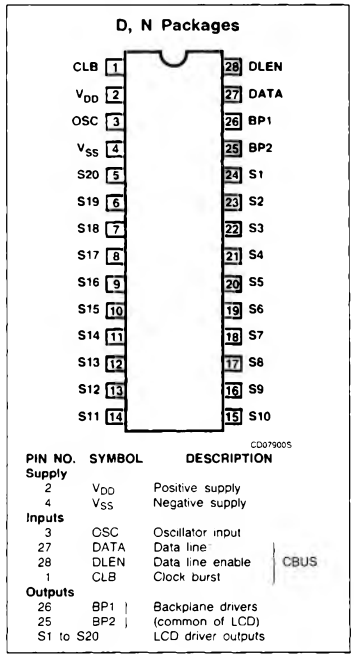
FEATURES

- **40 LCD segment drive capability**
- **Supply voltage 2.25 to 6.5V**
- **Low current consumption**
- **Serial data input**
- **CBUS control**
- **One-point built-in oscillator**
- **Expansion possibility**

APPLICATIONS

- **LCD displays**
- **Gauges**
- **Level/volume indicators**
- **Thermometers**

PIN CONFIGURATION



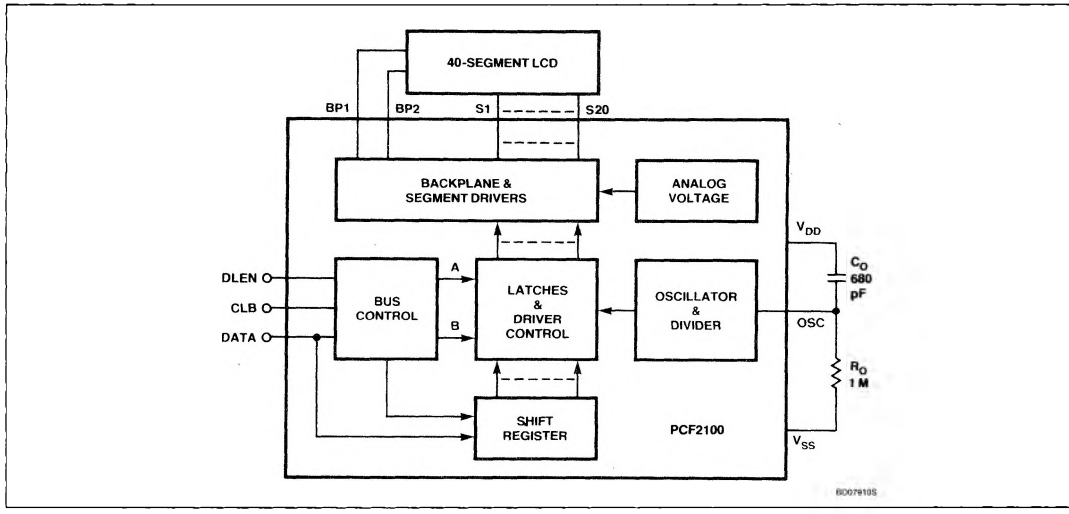
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117D)	−40°C to +85°C	PCF2100PN
28-Pin Plastic SO package (SO-28; SOT-136A)	−40°C to +85°C	PCF2100TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage with respect to V_{SS}	−0.3 to 8	V
V_N	Voltage on any pin	V_{SS} − 0.3 to V_{DD} + 0.3	V
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

DC AND AC ELECTRICAL CHARACTERISTICS V_{DD} = 2.25 to 6.5 V; V_{SS} = 0 V; T_A = −40 to +85°C; R_O = 1MΩ; C_O = 680pF, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{DD}	Supply current	No external load		10	50	μA
I_{DD}	Supply current	No external load; T_A = −25 to +85°C			30	μA
f_{LCD}	Display frequency	See Figure 7; T = 680μs	60	80	100	Hz
V_{BP}	DC component of LCD drive	With respect to V_{SX}		± 10		mV
	Load on each segment driver				10 500	MΩ pF
	Load on each backplane driver				1 5	MΩ nF
V_{IH}	Input voltage HIGH	See Figure 8	2			V
V_{IL}	Input voltage LOW	See Figure 8			0.6	V
t_R	Rise time V_{BP} to V_{SX}	Maximum load		20		μs
Inputs CLB, DATA, DLEN[1]						
t_R, t_F	Rise and fall times	See Figure 1			10	μs
t_{WH}	CLB pulse width HIGH	See Figure 1	1			μs
t_{WL}	CLB pulse width LOW	See Figure 1	9			μs
t_{SUDA}	Data setup time DATA → CLB	See Figure 1	8			μs
t_{HDDA}	Data hold time DATA → CLB	See Figure 1	8			μs
t_{SUEN}	Enable setup time DLEN → CLB	See Figure 1	1			μs
t_{SUDI}	Disable setup time CLB → DLEN	See Figure 1	8			μs
t_{SULD}	Setup time (load pulse) DLEN → CLB	See Figure 1	8			μs
t_{BUSY}	Busy-time from load pulse to next start of transmission	See Figure 1	8			μs
t_{SULZ}	Setup time (leading zero) DATA → CLB	See Figure 1	8			μs

NOTE:

1. All timing values are referred to V_{IHmin} and V_{ILmax} (see Figure 1). If external resistors are used in the bus lines (see Figure 8), the extra time constant has to be added.

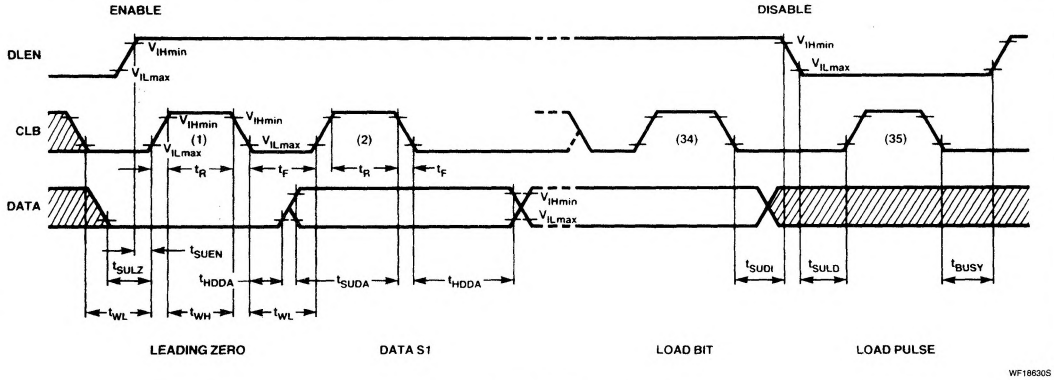
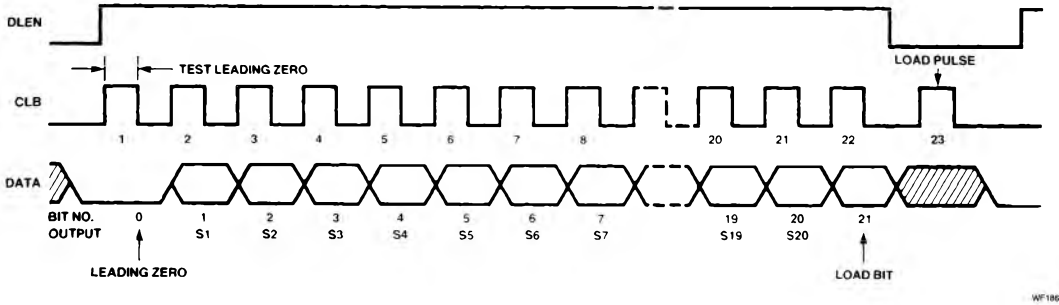


Figure 1. CBUS Timing



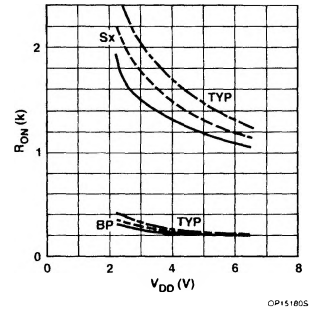
NOTES:
An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded.
When DATA-bit 21 is LOW, the B-latches (BP2) are loaded.
CLB-pulse 23 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

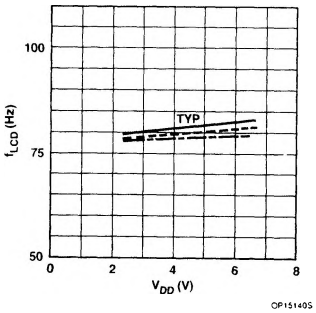
If one of the test conditions is not fulfilled, no action follows the load conditions (load pulse width DLEN is LOW) and the driver is ready to receive new data.

Figure 2. CBUS Data Format



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-· $T_A = +85°C$

Figure 3. Output Resistance of Backplane and Segments



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-· $T_A = +85°C$

Figure 4. Display Frequency as a Function of Supply Voltage; $R_OC_O = 680\mu s$

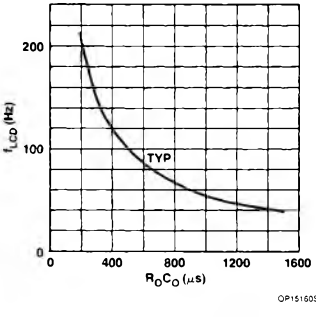
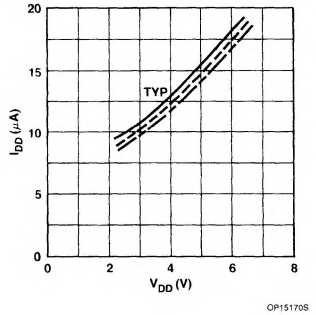


Figure 5. Display Frequency as a Function of $R_O \times C_O$ Time; $T_A = 25°C$



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-· $T_A = +85°C$

Figure 6. Supply Current as a Function of Supply Voltage

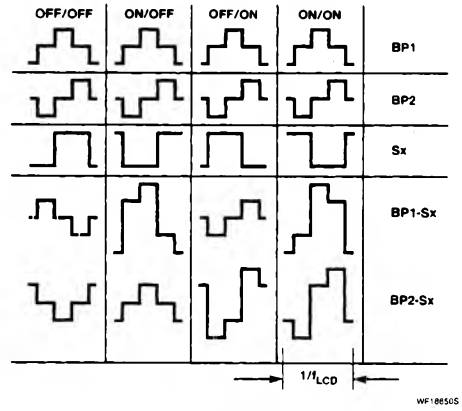
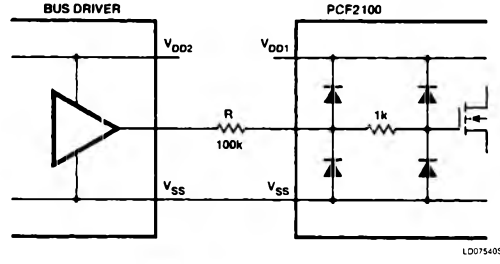
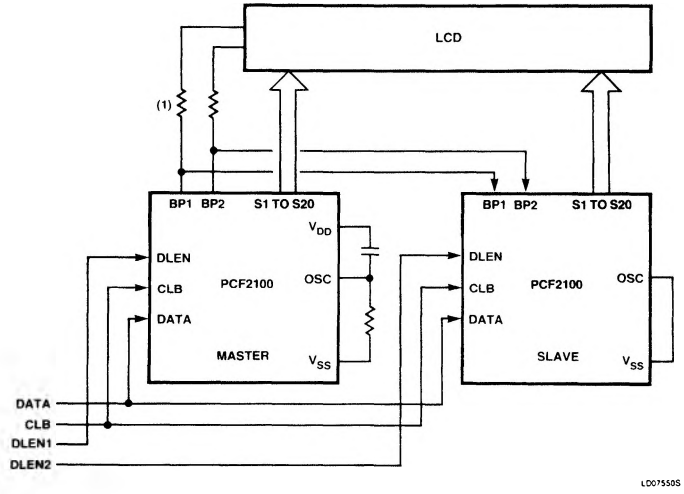


Figure 7. Timing Diagram



NOTES:
V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5V$, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leq 40\ \mu A$.

Figure 8. Input Circuitry



NOTES:

1. In the slave mode, the serial resistors between BP1 and BP2 of the PCF2100 and the backplane of the LCD must be > 2.7kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.
   By connecting the OSC to V_{SS}, the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, and PCF2100 ICs up to the BP drive capability of the master.

PCF2111 is a 64 LCD-segment driver.

Figure 9. Diagram Showing Expansion Possibility