256Mb DDR333 SDRAM

Features

CAS Latency and Frequency

CAS Latency	Maximum Operating Frequency (MHz)
	DDR333 (-6)
2	133
2.5	166

- Double data rate architecture: two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and $\overline{CK}$)
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions.
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Burst lengths: 2, 4, or 8
- CAS Latency: 2, 2.5
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 7.8µs Maximum Average Periodic Refresh Interval
- 2.5V (SSTL_2 compatible) I/O
- V_{DDQ} = 2.5V ± 0.2V
- V_{DD} = 2.5V ± 0.2V
- Package : 66pin TSOP-II / 60 balls 0.8mmx1.0mm pitch CSP.

Description

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a *2n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM effectively consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 256Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going high and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

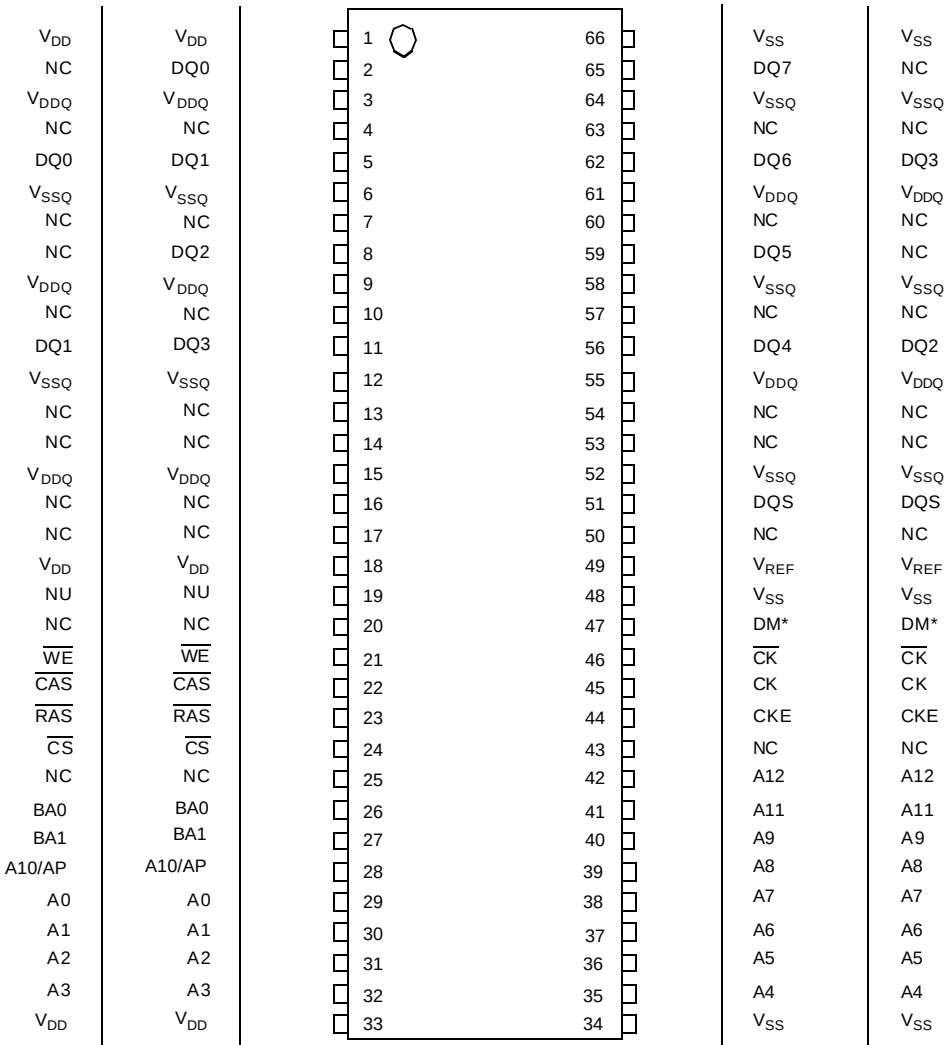
Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Pin Configuration - 400mil TSOP II



66-pin Plastic TSOP-II 400mil

32Mb x 8
NT5DS32M8AT

64Mb x 4
NT5DS64M4AT

Column Address Table

Organization	Column Address
64Mb x 4	A0-A9, A11
32Mb x 8	A0-A9

*DM is internally loaded to match DQ and DQS identically.

Pin Configuration - 60 balls 0.8mmx1.0mm Pitch CSP Package

<Top View >

See the balls through the package.

64 X 4

1	2	3		7	8	9
VSSQ	NC	VSS	A	VDD	NC	VDDQ
NC	VDDQ	DQ3	B	DQ0	VSSQ	NC
NC	VSSQ	NC	C	NC	VDDQ	NC
NC	VDDQ	DQ2	D	DQ1	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DQM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

32 X 8

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VDDQ	NC
NC	VDDQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DQM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

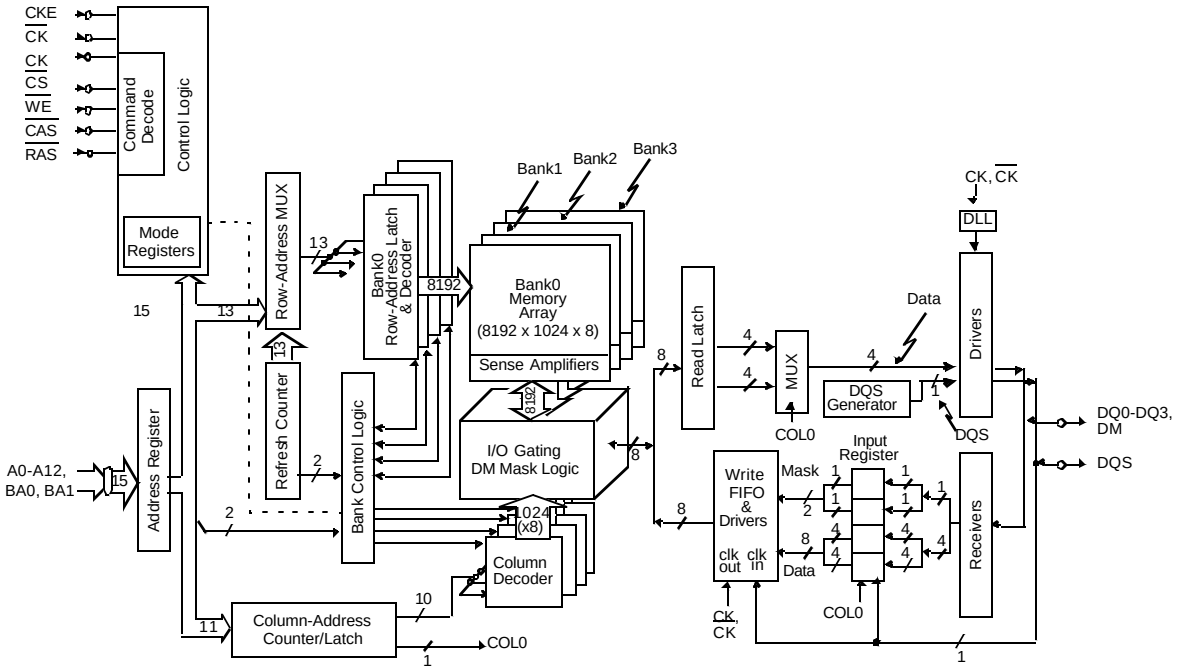
Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE, CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh. The standard pinout includes one CKE pin. Optional pinouts might include CKE1 on a different pin, in addition to CKE0, to facilitate independent power down control of stacked devices.
$\overline{CS}$, $\overline{CS0}$, $\overline{CS1}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin. Optional pinouts might include $\overline{CS1}$ on a different pin, in addition to $\overline{CS0}$, to allow upper or lower deck selection on stacked devices.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. During a Read, DM can be driven high, low, or floated.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A12	Input	**Address Inputs:** Provide the row address for Active commands, and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 low) or all banks (A10 high). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a Mode Register Set command.
DQ	Input/Output	**Data Input/Output:** Data bus.
DQS	Input/Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
NC		**No Connect:** No internal electrical connection is present.
NU		Electrical connection is present. Should not be connected at second level of assembly.
V_{DDQ}	Supply	**DQ Power Supply:** 2.5V ± 0.2V.
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5V ± 0.2V.
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_2 reference voltage:** (V_{DDQ} / 2) ± 1%.

Ordering Information

Part Number	Org.	CAS Latency	Clock (MHz)	CAS Latency	Clock (MHz)	Speed	Package
NT5DS64M4AT-6	x 4	2.5	166	2	133	DDR333	66 pin TSOP-II
NT5DS32M8AT-6	x 8						
NT5DS64M4AW-6	x 4	2.5	166	2	133	DDR333	60 balls CSP
NT5DS32M8AW-6	x 8						

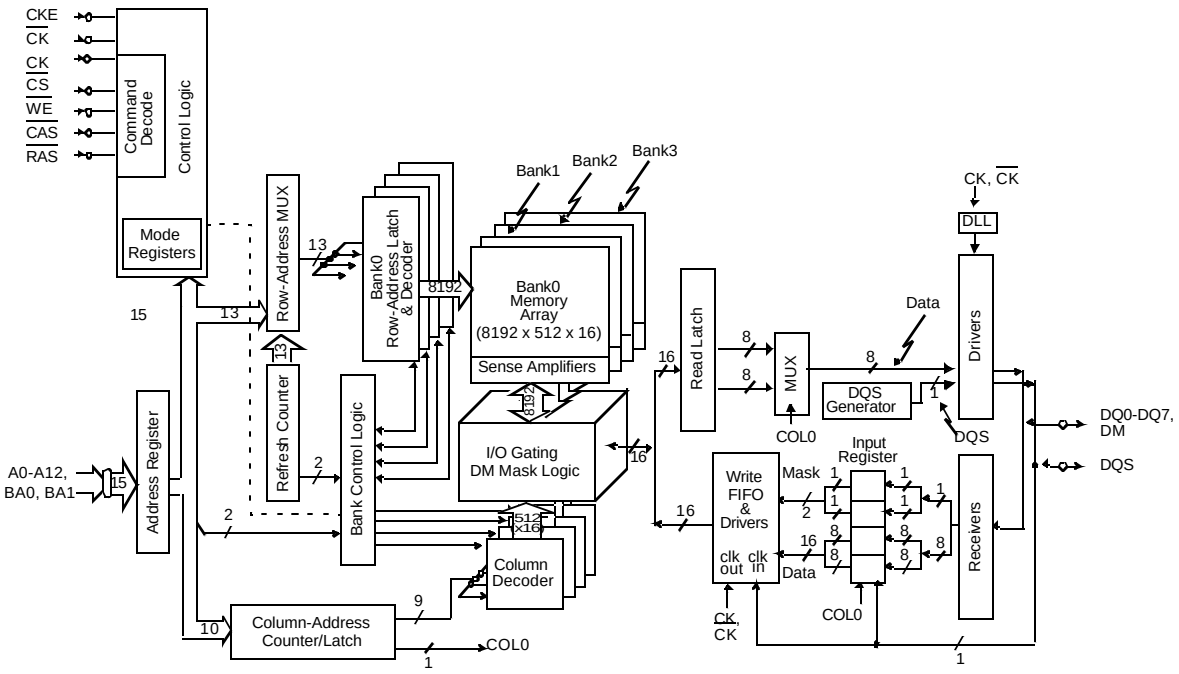
Block Diagram (64Mb x 4)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidi-rectional DQ and DQS signals.

Block Diagram (32Mb x 8)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Mode Register Operation

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus
0*	0*	Operating Mode						CAS Latency			BT	Burst Length			Mode Register

A12 - A9	A8	A7	A6 - A0	Operating Mode
0	0	0	Valid	Normal operation Do not reset DLL
0	1	0	Valid	Normal operation in DLL Reset
0	0	1	VS**	Vendor-Specific Test Mode
–	–	–		Reserved

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

VS** Vendor Specific

* BA0 and BA1 must be 0, 0 to select the Mode Register (vs. the Extended Mode Register).

Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-A i selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A i selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-A i selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in *Burst Definition* on page 9.

Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 or 2.5 clocks.

If a Read command is registered at clock edge *n*, and the latency is *m* clocks, the data is available nominally coincident with clock edge *n* + *m*.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Extended Mode Register Definition

BA1	BA0	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address Bus
0*	1*	Operating Mode										0**	DS	DLL	Extended Mode Register

A12 - A3	A2 - A0	Operating Mode
0	Valid	Normal Operation
–	–	All other states Reserved

Drive Strength

A_1	Drive Strength
0	Normal
1	Reserved

A_2	$\overline{QFC}$
0	Disable

A_0	DLL
0	Enable
1	Disable

* BA0 and BA1 must be 1, 0 to select the Extended Mode Register (vs. the base Mode Register)

Commands

Truth Tables 1a and 1b provide a reference of the commands supported by DDR SDRAM devices. A verbal description of each commands follows.

Truth Table 1a: Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	MNE	Notes
Deselect (Nop)	H	X	X	X	X	NOP	1, 9
No Operation (Nop)	L	H	H	H	X	NOP	1, 9
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1, 3
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1, 4
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1, 4
Burst Terminate	L	H	H	L	X	BST	1, 8
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1, 5
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR / SR	1, 6, 7
Mode Register Set	L	L	L	L	Op-Code	MRS	1, 2

1. CKE is high for all commands shown except Self Refresh.
2. BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register.)
3. BA0-BA1 provide bank address and A0-A12 provide row address.
4. BA0, BA1 provide bank address; A0-A*i* provide column address (where *i* = 9 for x8 and 9, 11 for x4); A10 high enables the Auto Precharge feature (nonpersistent), A10 low disables the Auto Precharge feature.
5. A10 LOW: BA0, BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0, BA1 are "Don't Care."
6. This command is auto refreshif CKE is high; Self Refresh if CKE is low.
7. Internal refresh counter controls row and bank addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts
9. Deselect and NOP are functionally interchangeable.

Truth Table 1b: DM Operation

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

1. Used to mask write data; provided coincident with the corresponding data.

Truth Table 2: Clock Enable (CKE)

1. CKE n is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. Command n is the command registered at clock edge n, and action n is a result of command n.
4. All states and sequences not shown are illegal or reserved.

Current State	CKE n-1	CKEn	Command n	Action n	Notes
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	1
Power Down	L	L	X	Maintain Power-Down	
Power Down	L	H	Deselect or NOP	Exit Power-Down	
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	
All Banks Idle	H	L	Auto Refresh	Self Refresh Entry	
Bank(s) Active	H	L	Deselect or NOP	Active Power-Down Entry	
	H	H	See “Truth Table 3: Current State Bank n - Command to Bank n (Same Bank)” on page 13		

1. Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (t_{XSNR}) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.

Truth Table 3: Current State Bank n - Command to Bank n (Same Bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	1-6
	L	H	H	H	No Operation	NOP. Continue previous operation	1-6
Idle	L	L	H	H	Active	Select and activate row	1-6
	L	L	L	H	Auto Refresh		1-7
	L	L	L	L	Mode Register Set		1-7
Row Active	L	H	L	H	Read	Select column and start Read burst	1-6, 10
	L	H	L	L	Write	Select column and start Write burst	1-6, 10
	L	L	H	L	Precharge	Deactivate row in bank(s)	1-6, 8
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	1-6, 10
	L	L	H	L	Precharge	Truncate Read burst, start Precharge	1-6, 8
	L	H	H	L	Burst Terminate	Burst Terminate	1-6, 9
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	1-6, 10, 11
	L	H	L	L	Write	Select column and start Write burst	1-6, 10
	L	L	H	L	Precharge	Truncate Write burst, start Precharge	1-6, 8, 11

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank.
   - Precharging: Starts with registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the idle state.
   - Row Activating: Starts with registration of an Active command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the "row active" state.
   - Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Deselect or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to Truth Table 4.
5. The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states.
   - Refreshing: Starts with registration of an Auto Refresh command and ends when t_{RFC} is met. Once t_{RFC} is met, the DDR SDRAM is in the "all banks idle" state.
   - Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR SDRAM is in the "all banks idle" state.
   - Precharging All: Starts with registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, all banks is in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.
9. Not bank-specific; Burst terminate affects the most recent Read burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
11. Requires appropriate DM masking.

Truth Table 4: Current State Bank n - Command to Bank m (Different bank)

(Part 1 of 2)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP/continue previous operation	1-6
	L	H	H	H	No Operation	NOP/continue previous operation	1-6
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m		1-6
Row Activating, Active, or Precharging	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-7
	L	H	L	L	Write	Select column and start Write burst	1-7
	L	L	H	L	Precharge		1-6
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start new Read burst	1-7
	L	L	H	L	Precharge		1-6
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-8
	L	H	L	L	Write	Select column and start new Write burst	1-7
	L	L	H	L	Precharge		1-6

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Read with Auto Precharge Enabled: See note 10.
   Write with Auto Precharge Enabled: See note 10.
4. Auto Refresh and Mode Register Set commands may only be issued when all banks are idle.
5. A Burst Terminate command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8. Requires appropriate DM masking.
9. A Write command may be applied after the completion of data output.
10. The Read with Auto Precharge enabled or Write with Auto Precharge enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible Precharge command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, Active, Precharge, Read, and Write commands to the other bank may be applied; during the access period, only Active and Precharge commands to the other bank may be applied. In either case, all other related limitations apply (e.g. contention between Read data and Write data must be avoided).

Truth Table 4: Current State Bank n - Command to Bank m (Different bank)

(Part 2 of 2)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Read (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start new Read burst	1-7,10
	L	H	L	L	Write	Select column and start Write burst	1-7,9,10
	L	L	H	L	Precharge		1-6
Write (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-7,10
	L	H	L	L	Write	Select column and start new Write burst	1-7,10
	L	L	H	L	Precharge		1-6

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Read with Auto Precharge Enabled: See note 10.
   Write with Auto Precharge Enabled: See note 10.
4. Auto Refresh and Mode Register Set commands may only be issued when all banks are idle.
5. A Burst Terminate command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8. Requires appropriate DM masking.
9. A Write command may be applied after the completion of data output.
10. The Read with Auto Precharge enabled or Write with Auto Precharge enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible Precharge command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, Active, Precharge, Read, and Write commands to the other bank may be applied; during the access period, only Active and Precharge commands to the other bank may be applied. In either case, all other related limitations apply (e.g. contention between Read data and Write data must be avoided).

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	−0.5 to V_{DDQ}+ 0.5	V
V_{IN}	Voltage on Inputs relative to V_{SS}	−0.5 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	−0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	−0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to +150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Min.	Max.	Units	Notes
Input Capacitance: CK, $\overline{CK}$	CI_1	2.0	3.0	pF	1
Delta Input Capacitance: CK, $\overline{CK}$	delta CI_1		0.25	pF	1
Input Capacitance: All other input-only pins (except DM)	CI_2	2.0	3.0	pF	1
Delta Input Capacitance: All other input-only pins (except DM)	delta CI_2		0.5	pF	1
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF	1, 2
Delta Input/Output Capacitance: DQ, DQS, DM	delta C_{IO}		0.5	pF	1

1. $V_{DDQ} = V_{DD} = 2.5V \pm 0.2V$ (minimum range to maximum range), f = 100MHz, $T_A = 25°C$, $VO_{DC} = V_{DDQ/2}$, $VO_{Peak\text{-}Peak} = 0.2V$.
2. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match input propagation times of DQ, DQS and DM in the system.

DC Electrical Characteristics and Operating Conditions

($0°C \le T_A \le 70°C$; $V_{DDQ} = 2.5V \pm 0.2V$, $V_{DD} = +2.5V \pm 0.2V$, see AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage	2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)	V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
$V_{IH(DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL(DC)}$	Input Low (Logic0) Voltage	– 0.3	V_{REF} – 0.15	V	1
$V_{IN(DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs	– 0.3	V_{DDQ} + 0.3	V	1
$V_{ID(DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
VI_{Ratio}	V-I Matching Pullup Current to Pulldown Current Ratio	0.71	1.4		5
I_I	Input Leakage Current Any input $0V \le V_{IN} \le V_{DD}$; (All other pins not under test = 0V)	– 5	5	µA	1
I_{OZ}	Output Leakage Current (DQs are disabled; $0V \le V_{out} \le V_{DDQ}$	– 5	5	µA	1
I_{OH}	Output Current: Nominal Strength Driver High current ($V_{OUT} = V_{DDQ}$ -0.373V, min V_{REF}, min V_{TT})	– 16.8		mA	1
I_{OL}	Low current (V_{OUT} = 0.373V, max V_{REF}, max V_{TT})	16.8			

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in tHalf-he DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire tempera-ture and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

DC Electrical Characteristics and Operating Conditions

($0°C \leq T_A \leq 70°C$; $V_{DDQ} = 2.5V \pm 0.2V$, $V_{DD} = +2.5V \pm 0.2V$, see AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
I_{OHW}	Output Current: Half- Strength Driver High current (V_{OUT}= V_{DDQ}-0.763V, min V_{REF}, min V_{TT})	– 9.0		mA	1
I_{OLW}	Low current (V_{OUT}= 0.763V, max V_{REF}, max V_{TT})	9.0			

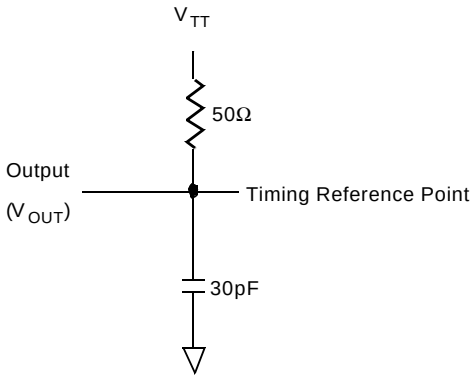
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in tHalf-he DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire tempera-ture and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input low (high) level.

AC Output Load Circuit Diagrams



DQS/DQ/DM Slew Rate

Parameterl	Symbol	DDR333 (-6)		Unit	Notes
		Min	Max		
DCS/DQ/DM input slew rate	DC_{SLEW}	TBD	TBD	V/ns	1,2

1. Measured between V_{IH} (DC), V_{IL} (DC), and V_{IL} (DC), V_{IH} (DC).
2. DQS, DQ, and DM input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal tran-sition through the DC region must be monotonic..

AC Input Operating Conditions ($0\,°C \le T_A \le 70\,°C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$, See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	V_{REF} + 0.31		V	1, 2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals		V_{REF} − 0.31	V	1, 2
$V_{ID(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX(AC)}$	Input Crossing Point Voltage, CK and $\overline{CK}$ Inputs	0.5*V_{DDQ} − 0.2	0.5*V_{DDQ} + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ns .
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

I_{DD} Specifications and Conditions ($0\,°C \le T_A \le 70\,°C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$, See AC Characteristics)

Symbol	Parameter/Condition	DDR333 t_{CK}=6ns	Unit	Notes
I_{DD0}	**Operating Current**: one bank; active / precharge; $t_{RC} = t_{RC}$ (min); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	85	mA	1
I_{DD1}	**Operating Current**: one bank; active / read / precharge; Burst = 2; $t_{RC} = t_{RC}$ (min); CL = 2.5; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	TBD	mA	1
I_{DD2P}	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE ≤ V_{IL} (max)	25	mA	1
I_{DD2N}	**Idle Standby Current:** $\overline{CS}$ ≥ V_{IH} (min); all banks idle; CKE ≥ V_{IH} (min); address and control inputs changing once per clock cycle	35	mA	1
I_{DD3P}	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE ≤ V_{IL} (max)	25	mA	1
I_{DD3N}	**Active Standby Current**: one bank; active / precharge; $\overline{CS}$ ≥ V_{IH} (min); CKE ≥ V_{IH} (min); $t_{RC} = t_{RAS}$ (max); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	60	mA	1
I_{DD4R}	**Operating Current:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; I_{OUT} = 0mA	165	mA	1
I_{DD4W}	**Operating Current**: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2.5	150	mA	1
I_{DD5}	**Auto-Refresh Current**: $t_{RC} = t_{RFC}$ (min)	170	mA	1
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V	3	mA	1, 2
I_{DD7}	**Operating current**: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC}$(min); I_{OUT} = 0mA.	TBD	mA	1

1. I_{DD} specifications are tested after the device is properly initialized.
2. Enables on-chip refresh and address counters.

Electrical Characteristics & AC Timing - Absolute Specifications

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter		DDR333 (-6)		Unit	Notes
			Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		– 0.7	+ 0.7	ns	1-4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		– 0.7	+ 0.7	ns	1-4
t_{CH}	CK high-level width		0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width		0.45	0.55	t_{CK}	1-4
t_{CK}	Clock cycle time	CL = 2.5	6	12	ns	1-4
		CL = 2.0	7.5	12		
t_{DH}	DQ and DM input hold time		0.45		ns	1-4, 15, 16
t_{DS}	DQ and DM input setup time		0.45		ns	1-4, 15, 16
t_{DIPW}	DQ and DM input pulse width (each input)		1.75		ns	1-4
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$		– 0.7	+ 0.7	ns	1-4, 5
t_{LZ}	Data-out low-impedance time from CK/$\overline{CK}$		– 0.7	+ 0.7	ns	1-4, 5
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)			+ 0.4	ns	1-4
t_{HP}	minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time		min (t_{CH}, t_{CL})		t_{CK}	1-4
t_{QHS}	Data Hold Skew Factor		0.55		ns	
t_{QH}	Data output hold time from DQS		t_{HP} - t_{QHS}		t_{CK}	1-4
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	t_{CK}	1-4
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time		2 x t_{CK}		ns	1-4
t_{WPRES}	Write preamble setup time		0		ns	1-4, 7
t_{WPST}	Write postamble		0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble		0.25		t_{CK}	1-4
t_{IH}	Address and control input hold time (fast slew rate)		0.75		ns	2-4, 9, 11, 12
t_{IS}	Address and control input setup time (fast slew rate)		0.75		ns	2-4, 9, 11, 12
t_{IH}	Address and control input hold time (slow slew rate)		0.8		ns	2-4, 10, 11, 12, 14
t_{IS}	Address and control input setup time (slow slew rate)		0.8		ns	2-4, 10, 11, 12, 14
t_{IPW}	Input pulse width		2.2		ns	2-4, 12
t_{RPRE}	Read preamble		0.9	1.1	t_{CK}	1-4
t_{RPST}	Read postamble		0.40	0.60	t_{CK}	1-4
t_{RAS}	Active to Precharge command		42	120,000	ns	1-4

Electrical Characteristics & AC Timing - Absolute Specifications

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	DDR333 (-6)		Unit	Notes
		Min	Max		
t_{RC}	Active to Active/Auto-refresh command period	60		ns	1-4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	72		ns	1-4
t_{RCD}	Active to Read or Write delay	18		ns	1-4
t_{RAP}	Active to Read Command with Autoprecharge	18		ns	1-4
t_{RP}	Precharge command period	18		ns	1-4
t_{RRD}	Active bank A to Active bank B command	12		ns	1-4
t_{WR}	Write recovery time	15		ns	1-4
t_{DAL}	Auto precharge write recovery + precharge time	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}	1-4, 13
t_{WTR}	Internal write to read command delay	1		t_{CK}	1-4
t_{XARD}	Power down exit time	6		ns	1-4
t_{XSNR}	Exit self-refresh to non-read command	75		ns	1-4
t_{XSRD}	Exit self-refresh to read command	200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval		7.8	µs	1-4, 8

Electrical Characteristics & AC Timing - Absolute Specifications

Notes

1. Input slew rate = 1V/ns.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For command/address input slew rate $\geq$ 1.0V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
10. For command/address input slew rate $\geq$ 0.5V/ns and < 1.0V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
11. CK/$\overline{CK}$ slew rates are $\geq$ 1.0V/ns.
12. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
13. For each of the terms in parentheses, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

14. An input setup and hold time derating table is used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	delta (t_{IS})	delta (t_{IH})	Unit	Notes
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+50	0	ps	1,2
0.3 V/ns	+100	0	ps	1,2

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on eachdevice.

15. An input setup and hold time derating table is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	delta (t_{DS})	delta (t_{DH})	Unit	Notes
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+75	+75	ps	1,2
0.3 V/ns	+150	+150	ps	1,2

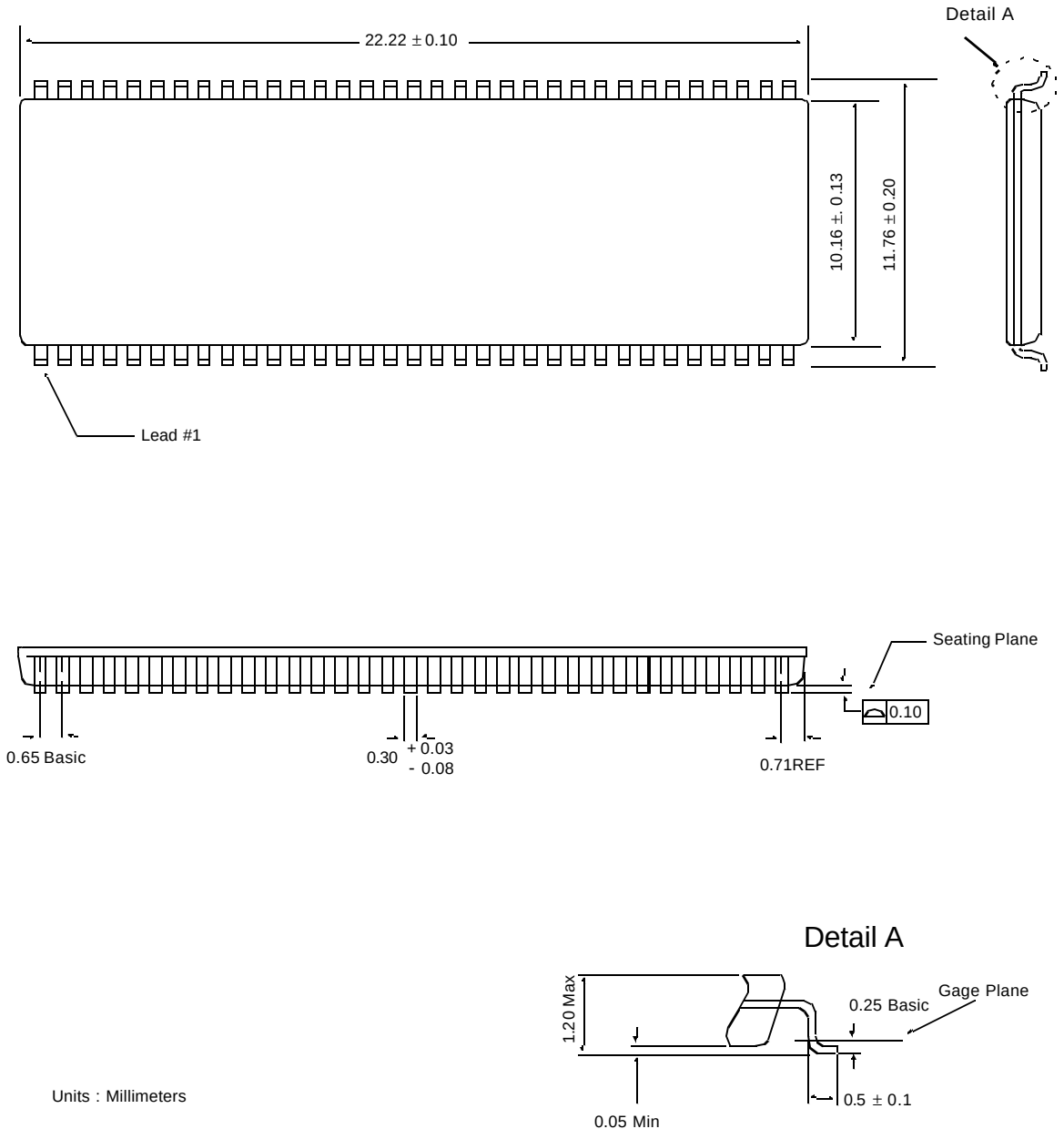
1. I/O slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on eachdevice.

16. An I/O Delta Rise, Fall Derating table is used to increase t_{DS} and t_{DH}) in the case where DQ, DM, and DQS slew rates differ.

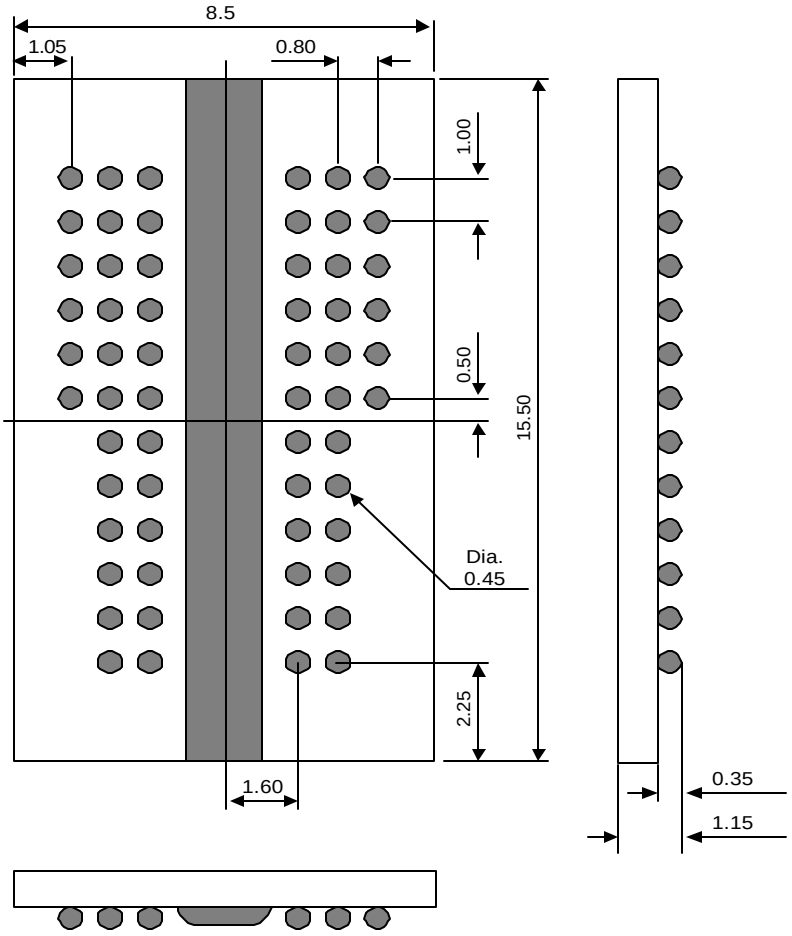
Input Slew Rate	delta (t_{DS})	delta (t_{DH})	Unit	Notes
0.0 V/ns	0	0	ps	1,2,3,4
0.25 V/ns	+50	+50	ps	1,2,3,4
0.5 V/ns	+100	+100	ps	1,2,3,4

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: [1/(slew rate 1)] - [1/(slew rate 2)]
   For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns
   Delta rise, fall = (1/0.5) - (1/0.4) [ns/V]
   = -0.5 ns/V
   Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

Package Dimensions (400mil; 66 lead; Thin Small Outline Package)



Package Dimensions (60 balls; 0.8mmx1.0mm Pitch; CSP Package)



Note : All dimensions are typical unless otherwise stated.
Unit : Millimeters

Revision Log

Rev	Contents of Modification
10/01	Preliminary
	Changed to Revision 1.0
	Modified typo error for CSP package dimension
	Added tQHS on AC timing table
06/02	Changed to Revision 1.1
	Changed I_{DD2P} from 15mA to 25mA
	Changed I_{DD3P} from 15mA to 25mA
	Removed DDR300 speed sort
08/02	Changed to Revision 1.2
	Added t_{XARD} (Power down exit time) to AC Timing Table